

# Sizhe Zhang

Portfolio: [vu-sizhe-zhang.github.io](https://vu-sizhe-zhang.github.io)

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## EDUCATION

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| • <b>Villanova University</b>   | Villanova, PA       |
| • <i>Ph.D. Student in Computer Engineering Advised by Prof. Xun Jiao</i>      | <i>2021-Present</i> |
| • <b>Cornell University</b>   | Ithaca, NY          |
| • <i>Master of Engineering in Electrical Computer Engineering</i>             | <i>2019-2020</i>    |
| • <b>University at Buffalo</b>  | Buffalo, NY         |
| • <i>Bachelor of Science in Electrical Engineering <b>Magna Cum Laude</b></i> | <i>2014-2019</i>    |

## RESEARCH INTEREST

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- **1:** Electronic design automation, Approximate Computing
  - **2:** Machine Learning, Federated Learning
  - **3:** Neuromorphic computing, Hyperdimensional Computing, Vector Symbolic Architectures

## PROJECTS

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- **Hyperdimensional Computing system robustness assessment and enhancement:** Accessing hyperdimensional computing system robustness and explored several approaches to enhance the robustness of hyperdimensional computing. Simulated energy saving through memory voltage scaling
  - **Federated Hyperdimensional Computing:** Explore the different aspects of federated learning based on hyperdimensional computing and deep learning
  - **Vending Machine System Based on Object Detection Neural Networks :** Designed and implemented an embedded system (based on Raspberry Pi 4) to upgrade a basic cooler into a vending machine system. Built a data collection platform to collect goods images and automate label and box the object. Training an object detection neural network by using red cloud services. Combined a custom-trained object detection model with a pre-trained model (running on Google Coral TPU accelerator) and improved the detection accuracy and system performance.
  - **Quad-Core RISC-V Processor Design:** Designed and implemented a five-stage quad-core RISC-V processor. By using special python library Pymtl tested and benchmarked with sorting algorithm based on C.
  - **Neural Network Parallel Computing by CUDA:** Design and implemented a basic neural network for handwritten classification by using CUDA for GPU parallel computing both for inference and training.
  - **Transistor Level Application of Mars Rover Inquire Finite State Machine:** Design and implemented a mars rover control chip on the schematic and gate level by using Cadence Virtuoso. Successfully passed all the test and embedded into a pad frame.

## PUBLICATIONS

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- **1: Sizhe Zhang,** Ruixuan Wang, Dongning Ma, Jeff Jun Zhang, Xunzhao Yin, Xun Jiao, "Energy-Efficient Brain-Inspired Hyperdimensional Computing Using Voltage Scaling". 2022 Design, Automation and Test in Europe Conference (**DATE**), Antwerp, Belgium, 2022
  - **2: Sizhe Zhang,** Ruixuan Wang, Jeff (Jun) Zhang, Abbas Rahimi, Xun Jiao, "Assessing Robustness of Hyperdimensional Computing Against Errors in Associative Memory". The 32nd IEEE International Conference on Application-specific Systems, Architectures and Processors (**ASAP**), Virtual, 2021.
  - **3:** Depeng Wang, Huijuan Zhang, Tri Vu, Ye Zhan, Akash Malhotra, Pei Wang, Upendra Chitgupi, Aliza Rai, **Sizhe Zhang,** Lidai Wang, Jan D Huizinga, Jonathan F Lovell, Jun Xia. "Trans-illumination intestine projection imaging of intestinal motility in mice". **Nature Communications**, 2021.

## HONORS AND AWARDS

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- DAC 2021 Young Fellow Program
  - University at Buffalo Dean's List: Spring 2015, Spring 2018, Fall 2018

## RESEARCH & TEACHING EXPERIENCE

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| • <b>Graduate Assistant</b>  | Villanova University  |
| • <i>Dependable, Efficient, and Intelligent Computing Lab (DETAIL)</i>                   | <i>2021</i>           |
| • <b>Student Assistant</b>   | University at Buffalo |
| • <i>Assistant EE202 Circuit Analysis, EE305 Applied Probability and EE Study lounge</i> | <i>2018</i>           |
| • <b>Research Assistant</b>  | University at Buffalo |
| • <i>University at Buffalo Optical &amp; Ultrasonic Imaging Laboratory</i>               | <i>2017-2018</i>      |