AN4555
Application note

Getting started with STM32L4 series hardware development

Introduction

This application note is intended for system designers who require a hardware implementation overview of the development board features such as the power supply, the clock management, the reset control, the boot mode settings and the debug management. It shows how to use STM32L4 MCUs and describes the minimum hardware resources required to develop an application using STM32L4 series.

Detailed reference design schematics are also contained in this document with descriptions of the main components, interfaces and modes.

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1 Power supplies

1.1 Power supplies

The STM32L4 series devices require a 1.71 V to 3.6 V V_{DD} operating voltage supply. Several independent supplies (V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}), can be provided for specific peripherals:

- V_{DD} = 1.71 V to 3.6 V

  V_{DD} is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD pins.

- V_{DDA} = 1.62 V (ADCs/COMPs) / 1.8 V (DACs/OPAMPs) / 2.4 V (VREFBUF) to 3.6 V

  V_{DDA} is the external analog power supply for A/D converters, D/A converters, voltage reference buffer, operational amplifiers and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage.

- V_{DDUSB} = 3.0 to 3.6 V (USB used)

  V_{DDUSB} is the external independent power supply for USB transceivers. The V_{DDUSB} voltage level is independent from the V_{DD} voltage.

- V_{DDIO2} = 1.08 to 3.6 V

  V_{DDIO2} is the external power supply for 14 I/Os (Port G[15:2]). The V_{DDIO2} voltage level is independent from the V_{DD} voltage.

Note: When the functions supplied by V_{DDA}, V_{DDIO2} or V_{DDUSB} are not used, these supplies should preferably be shorted to V_{DD}.

- V_{LCD} = 2.5 to 3.6 V

  The LCD controller can be powered either externally through VLCD pin, or internally from an internal voltage generated by the embedded step-up converter. VLCD is multiplexed with PC3 which can be used as GPIO when the LCD is not used.

- V_{BAT} = 1.55 to 3.6 V

  V_{BAT} is the power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

- V_{REF-}, V_{REF+}

  V_{REF+} is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.

  When $V_{DDA} < 2$ V V_{REF+} must be equal to V_{DDA}.

  When $V_{DDA} \geq 2$ V V_{REF+} must be between 2 V and V_{DDA}.

  V_{REF+} can be grounded when ADC and DAC are not active.

  The internal voltage reference buffer supports two output voltages, which are configured with VRS bit in the VREF_CSR register:

  - V_{REF+} around 2.048 V. This requires V_{DDA} equal to or higher than 2.4 V.
  - V_{REF+} around 2.5 V. This requires V_{DDA} equal to or higher than 2.8 V.

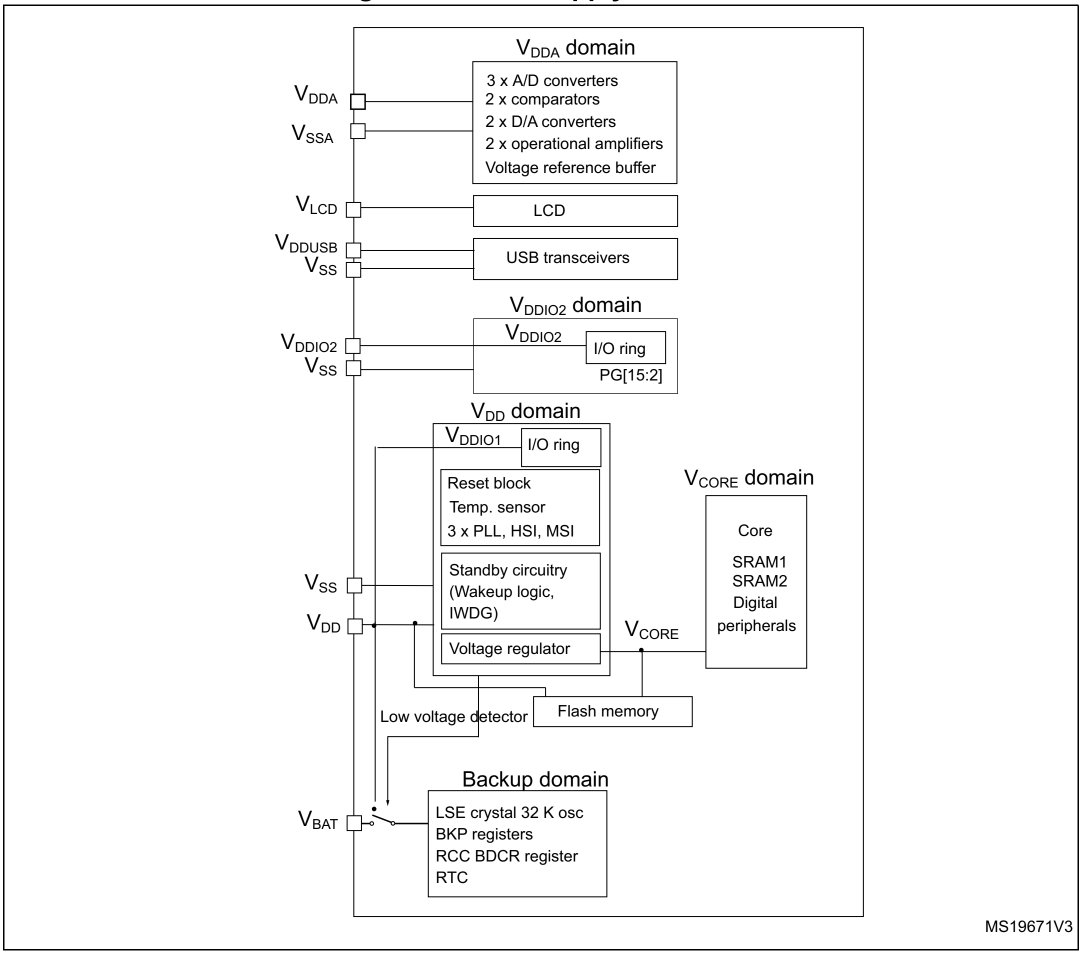
  VREF- and VREF+ pins are not available on all packages. When not available, they are bonded to VSSA and VDDA, respectively.

  When the VREF+ is double-bonded with VDDA in a package, the internal voltage reference buffer is not available and must be kept disable (refer to datasheet for packages pinout description).

  V_{REF-} must always be equal to V_{SSA}.

An embedded linear voltage regulator is used to supply the internal digital power V_{CORE}. V_{CORE} is the power supply for digital peripherals, SRAM1 and SRAM2. The Flash is supplied by V_{CORE} and V_{DD}.

Figure 1. Power supply overview



1.1.1 Independent analog peripherals supply

To improve ADC and DAC conversion accuracy and to extend the supply flexibility, the analog peripherals have an independent power supply which can be separately filtered and shielded from noise on the PCB.

- The analog peripherals voltage supply input is available on a separate V_{DDA} pin.
- An isolated supply ground connection is provided on V_{SSA} pin.

The V_{DDA} supply voltage can be different from V_{DD}. The presence of V_{DDA} must be checked before enabling any of the analog peripherals supplied by V_{DDA} (A/D converter, D/C converter, comparators, operational amplifiers, voltage reference buffer).

The V_{DDA} supply can be monitored by the Peripheral Voltage Monitoring, and compared with two thresholds (1.65 V for PVM3 or 2.2 V for PVM4), refer to reference manual *section: Peripheral Voltage Monitoring (PVM)* for more details.

When a single supply is used, V_{DDA} can be externally connected to V_{DD} through the external filtering circuit in order to ensure a noise-free V_{DDA} reference voltage.

ADC and DAC reference voltage

To ensure a better accuracy on low-voltage inputs and outputs, the user can connect to V_{REF+} a separate reference voltage lower than V_{DDA}. V_{REF+} is the highest voltage, represented by the full scale value, for an analog input (ADC) or output (DAC) signal.

V_{REF+} can be provided either by an external reference of by an internal buffered voltage reference (VREF).

The internal voltage reference is enabled by setting the ENVR bit in the *VREF control and status register (VREF_CSR)*. The voltage reference is set to 2.5 V when the VRS bit is set and to 2.048 V when the VRS bit is cleared. The internal voltage reference can also provide the voltage to external components through V_{REF+} pin. Refer to the device datasheet or reference manual for further information.

1.1.2 Independent I/O supply rail

Some I/Os from Port G (PG[15:2]) are supplied from a separate supply rail. The power supply for this rail can range from 1.08 to 3.6 V and is provided externally through the V_{DDIO2} pin. The V_{DDIO2} voltage level is completely independent from V_{DD} or V_{DDA}. The V_{DDIO2} pin is available only for some packages. Refer to the pinout diagrams or tables in the related device datasheet(s) for I/O list(s).

After reset, the I/Os supplied by V_{DDIO2} are logically and electrically isolated and therefore are not available. The isolation must be removed before using any I/O from PG[15:2], by setting the IOSV bit in the PWR_CR2 register, once the V_{DDIO2} supply is present.

The V_{DDIO2} supply is monitored by the Peripheral Voltage Monitoring (PVM2) and compared with the internal reference voltage (3/4 V_{REFINT}, around 0.9 V), refer to reference manual *section: Peripheral Voltage Monitoring (PVM)* for more details.

1.1.3 Independent USB transceivers supply

The USB transceivers are supplied from a separate V_{DDUSB} power supply pin. V_{DDUSB} range is from 3.0 V to 3.6 V and is completely independent from V_{DD} or V_{DDA}.

After reset, the USB features supplied by V_{DDUSB} are logically and electrically isolated and therefore are not available. The isolation must be removed before using the USB OTG peripheral, by setting the USV bit in the PWR_CR2 register, once the V_{DDUSB} supply is present.

The V_{DDUSB} supply is monitored by the Peripheral Voltage Monitoring (PVM1) and compared with the internal reference voltage (V_{REFINT}, around 1.2 V), refer to reference manual s*ection: Peripheral Voltage Monitoring (PVM)* for more details.

1.1.4 Independent LCD supply

The VLCD pin is provided to control the contrast of the glass LCD. This pin can be used in two ways:

- It can receive from an external circuitry the desired maximum voltage that is provided on segment and common lines to the glass LCD by the microcontroller.
- It can also be used to connect an external capacitor that is used by the microcontroller for its voltage step-up converter. This step-up converter is controlled by software to provide the desired voltage to segment and common lines of the glass LCD.

The voltage provided to segment and common lines defines the contrast of the glass LCD pixels. This contrast can be reduced when you configure the dead time between frames.

- When an external power supply is provided to the VLCD pin, it should range from 2.5 V to 3.6 V. It does not depend on VDD.
- When the LCD is based on the internal step-up converter, the VLCD pin should be connected to a capacitor (see the product datasheet for further information).

1.1.5 Battery backup domain

To retain the content of the Backup registers and supply the RTC function when V_{DD} is turned off, the V_{BAT} pin can be connected to an optional backup voltage supplied by a battery or by another source.

The V_{BAT} pin powers the RTC unit, the LSE oscillator and the PC13 to PC15 I/Os, allowing the RTC to operate even when the main power supply is turned off. The switch to the V_{BAT} supply is controlled by the power-down reset embedded in the Reset block.

Warning: During $t_{RSTTEMPO}$ (temporization at V_{DD} startup) or after a PDR has been detected, the power switch between V_{BAT} and V_{DD} remains connected to V_{BAT}.
During the startup phase, if V_{DD} is established in less than $t_{RSTTEMPO}$ (refer to the datasheet for the value of $t_{RSTTEMPO}$) and V_{DD} > V_{BAT} + 0.6 V, a current may be injected into V_{BAT} through an internal diode connected between V_{DD} and the power switch (V_{BAT}).
If the power supply/battery connected to the V_{BAT} pin cannot support this current injection, it is strongly recommended to connect an external low-drop diode between this power supply and the V_{BAT} pin.

If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD} with a 100 nF external ceramic decoupling capacitor.

When the backup domain is supplied by V_{DD} (analog switch connected to V_{DD}), the PC13, PC14 and PC15 pins, belonging to V_{BAT} domain, can have these functions:

- GPIO pins
- RTC or LSE pins (refer to reference manual *section: RTC functional description*)

Note: Due to the fact that the analog switch can transfer only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is restricted: the speed has to be limited to 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive a LED).

When the backup domain is supplied by V_{BAT} (analog switch connected to V_{BAT} because V_{DD} is not present), the following functions are available:

- PC13, PC14 and PC15 can be controlled only by RTC or LSE refer to reference manual *section: RTC functional description*
- PA0 and PE6 can be used as tamper inputs by the RTC (RTC_TAMP2 and RTC_TAMP3 respectively)

Backup domain access

After a system reset, the backup domain (RTC registers and backup registers) is protected against possible unwanted write accesses. To enable access to the backup domain, proceed as follows:

1. Enable the power interface clock by setting the PWREN bits in the *APB1 peripheral clock enable register 1 (RCC_APB1ENR1)*.
2. Set the DBP bit in the *Power control register 1 (PWR_CR1)* to enable access to the backup domain.
3. Select the RTC clock source in the *Backup domain control register (RCC_BDCR)*.
4. Enable the RTC clock by setting the RTCEN [15] bit in the *Backup domain control register (RCC_BDCR)*.

VBAT battery charging

When VDD is present, It is possible to charge the external battery on VBAT through an internal resistance.

The VBAT charging is done either through a 5 kΩ resistor or through a 1.5 kΩ resistor depending on the VBRS bit value in the PWR_CR4 register.

The battery charging is enabled by setting VBE bit in the PWR_CR4 register. It is automatically disabled in VBAT mode.

1.1.6 Voltage regulator

Two embedded linear voltage regulators supply all the digital circuitries, except for the Standby circuitry and the backup domain. The main regulator output voltage (V_{CORE}) can be programmed by software to two different power ranges (Range 1 and Range 2) in order to optimize the consumption depending on the system's maximum operating frequency (refer to reference manual *Section: Clock source frequency versus voltage scaling* and to *Section: Read access latency*.

The voltage regulators are always enabled after a reset. Depending on the application modes, the V_{CORE} supply is provided either by the main regulator (MR) or by the low-power regulator (LPR).

- In Run, Sleep and Stop 0 modes, both regulators are enabled and the main regulator (MR) supplies full power to the V_{CORE} domain (core, memories and digital peripherals).
- In low-power run and low-power sleep modes, the main regulator is off and the low-power regulator (LPR) supplies low power to the V_{CORE} domain, preserving the contents of the registers and of internal SRAM1 and SRAM2.
- In Stop 1 and Stop 2 modes, the main regulator is off and the low-power regulator (LPR) supplies low power to the V_{CORE} domain, preserving the contents of the registers and internal SRAM1 and SRAM2.
- In Standby mode with SRAM2 content preserved (RRS bit is set in the PWR_CR3 register), the main regulator (MR) is off and the low-power regulator (LPR) provides the supply to SRAM2 only. The core and digital peripherals (except Standby circuitry and backup domain) and SRAM1 are powered off.
- In Standby mode, both regulators are powered off. The contents of the registers and SRAM1 and SRAM2 is lost except for the Standby circuitry and the backup domain.
- In Shutdown mode, both regulators are powered off. When exiting from Shutdown mode, a power-on reset is generated. Consequently, the contents of the registers and

of SRAM1 and SRAM2 is lost, except for the backup domain.

1.1.7 Dynamic voltage scaling management

The dynamic voltage scaling is a power management technique which consists in increasing or decreasing the voltage used for the digital peripherals (V_{CORE}), according to the application performance and power consumption needs.

Dynamic voltage scaling to increase V_{CORE} is known as overvolting. It allows to improve the device performance.

Dynamic voltage scaling to decrease V_{CORE} is known as undervolting. It is performed to save power, particularly in laptop and other mobile devices where the energy comes from a battery and is thus limited.

- Range 1: High-performance range.

The main regulator provides a typical output voltage at 1.2 V. The system clock frequency can be up to 80 MHz. The Flash access time for read access is minimum, write and erase operations are possible.

- Range 2: Low-power range.

The main regulator provides a typical output voltage at 1.0 V. The system clock frequency can be up to 26 MHz.The Flash access time for a read access is increased as compared to Range 1; write and erase operations are possible.

Voltage scaling is selected through the VOS bit in the PWR_CR1 register.

The sequence to go from Range 1 to Range 2 is:

1. Reduce the system frequency to a value lower than 26 MHz.
2. Adjust number of wait states according new frequency target in Range2 (LATENCY bits in the FLASH_ACR).
3. Program the VOS bits to “10” in the PWR_CR1 register.

The sequence to go from Range 2 to Range 1 is:

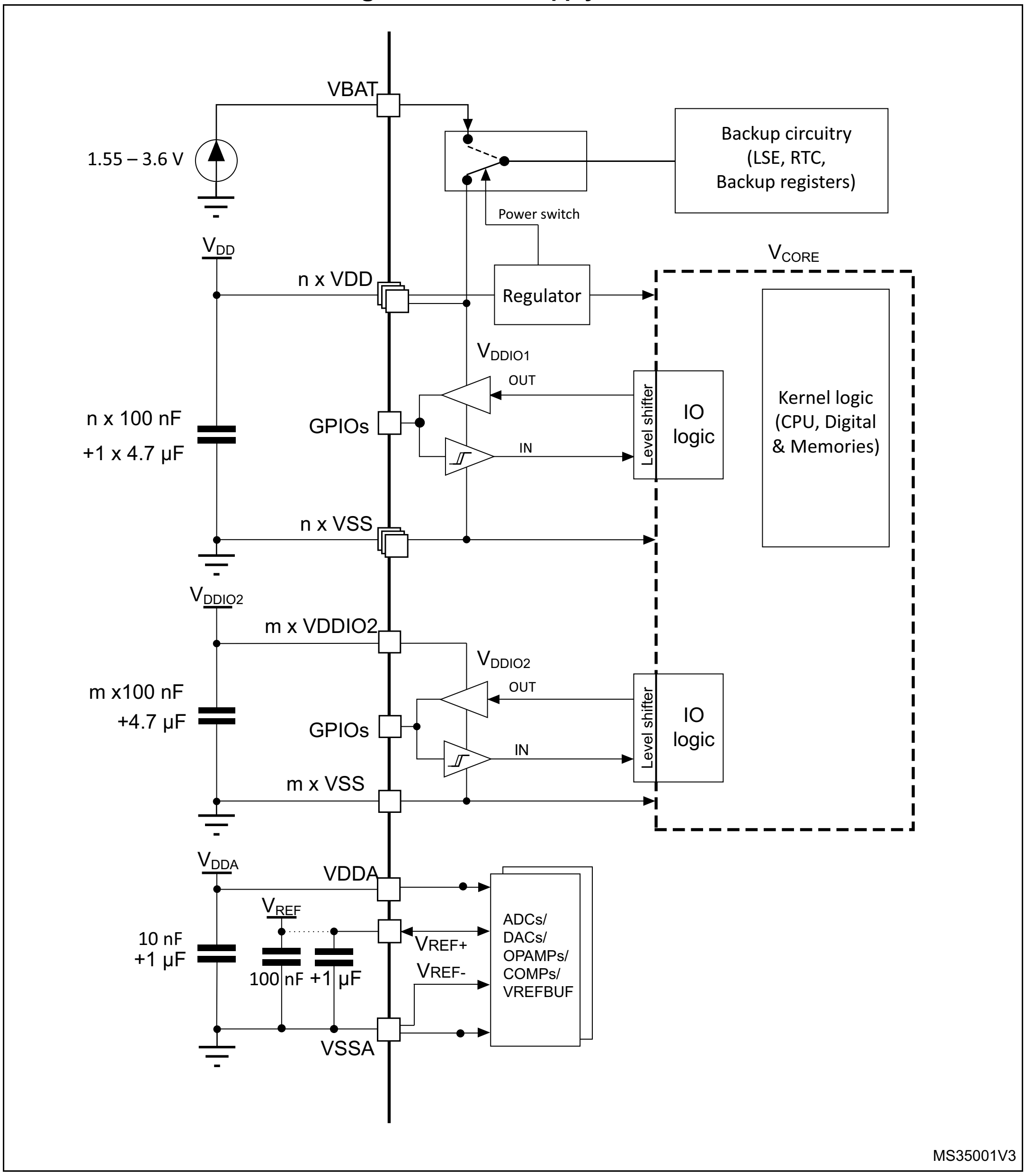
1. Program the VOS bits to “01” in the PWR_CR1 register.
2. Wait until the VOSF flag is cleared in the PWR_SR2 register.
3. Adjust number of wait states according new frequency target in Range1 (LATENCY bits in the FLASH_ACR).
4. Increase the system frequency.

1.2 Power supply schemes

The circuit is powered by a stabilized power supply, V_{DD}.

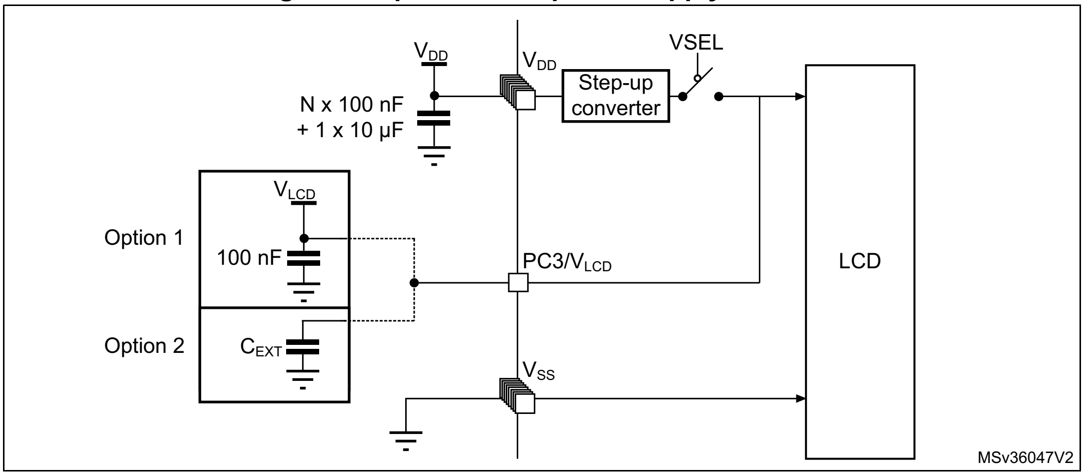
- The VDD pins must be connected to V_{DD} with external decoupling capacitors; one single Tantalum or Ceramic capacitor (minimum 4.7 µF typical 10 µF) for the package + one 100 nF Ceramic capacitor for each V_{DD} pin).
- The VDDA pin must be connected to two external decoupling capacitors (100 nF Ceramic capacitor + 1 µF Tantalum or Ceramic capacitor).
  Additional precautions can be taken to filter digital noise: V_{DDA} can be connected to V_{DD} through a ferrite bead. In this case take care to keep a (V_{DDA} - V_{DD}) difference lower than 300 mV.
- The VREF+ pin can be provided by an external voltage reference in which case an external capacitor of 100 and a 1 µF capacitor must be connected on this pin.
  It can also be provided internally by the Voltage Reference Buffer in which case an external capacitor of 1 µF (typical) must be connected on this pin.
- The VBAT pin can be connected to an external battery to preserve backup domain content.
  When V_{DD} is present, it is possible to charge the external battery on VBAT through a 5 kΩ or 1.5 kΩ internal resistor.
  If no external battery is used in the application, it is recommended to connect VBAT externally to V_{DD} with a 100 nF external ceramic decoupling capacitor.
- The VLCD pin can be provided by an external voltage reference in which case an external capacitor of 100 nF and a 1 µF capacitor must be connected on this pin.
  It can also be provided internally by the Step-up Converter in which case an external capacitor of 1 µF (typical) must be connected on this pin.

Figure 2. Power supply scheme



1. V_{REF}+ is either connected to V_{DDA} or to V_{REF}.
2. N is the number of V_{DD} and V_{SS} inputs.

Figure 3. Optional LCD power supply scheme



- **Option 1**: LCD power supply is provided by a dedicated VLCD supply source, VSEL switch is open.
- **Option 2**: LCD power supply is provided by the internal step-up converter, VSEL switch is closed, an external capacitance is needed for correct behavior of this converter.

Note: VLCD is multiplexed on PC3 GPIO that needs to be configured as VLCD alternate function.

1.3 Reset and power supply supervisor

1.3.1 Power-on reset (POR) / power-down reset (PDR) / brown-out reset (BOR)

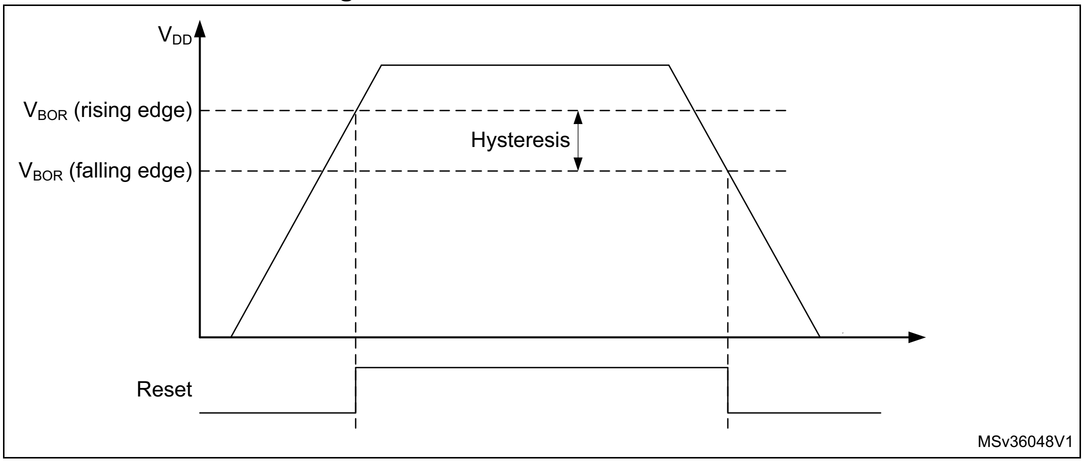
The device has an integrated power-on reset (POR) / power-down reset (PDR), coupled with a brown-out reset (BOR) circuitry. The BOR is active in all power modes except Shutdown mode, and cannot be disabled.

Five BOR thresholds can be selected through option bytes.

During power-on, the BOR keeps the device under reset until the supply voltage V_{DD} reaches the specified V_{BORx} threshold. When V_{DD} drops below the selected threshold, a device reset is generated. When V_{DD} is above the V_{BORx} upper limit, the device reset is released and the system can start.

For more details on the brown-out reset thresholds, refer to the electrical characteristics section in the datasheet.

Figure 4. Brown-out reset waveform



1.3.2 Power reset

A power reset is generated when one of the following events occurs:

1. a Brown-out reset (BOR).
2. when exiting from Standby or Shutdown mode.

A Brown-out reset, including power-on or power-down reset (POR/PDR), sets all registers to their reset values except the Backup domain.

When exiting Standby or Shutdown mode, all registers in the V_{CORE} domain are set to their reset value. Registers outside the V_{CORE} domain (RTC, WKUP, IWDG, and Standby/Shutdown modes control) are not impacted.

1.3.3 System reset

A system reset sets all registers to their reset values except the reset flags in the clock control/status register (RCC_CSR) and the registers in the Backup domain.

A system reset is generated when one of the following events occurs:

1. A low level on the NRST pin (external reset)
2. Window watchdog event (WWDG reset)
3. Independent watchdog event (IWDG reset)
4. A firewall event (FIREWALL reset)
5. A software reset (SW reset)
6. Low-power management reset
7. Option byte loader reset
8. A Brown-out reset

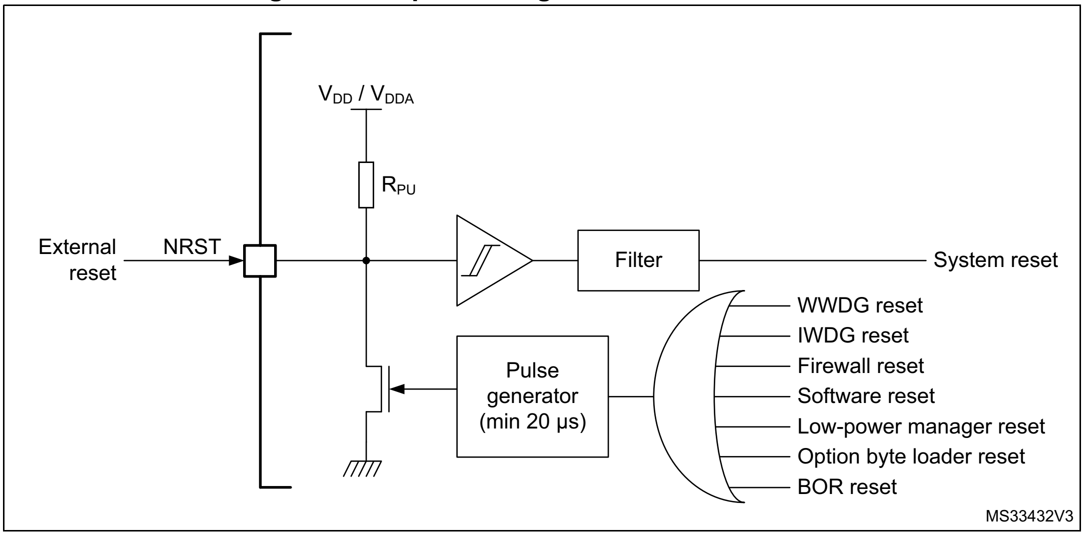
The reset source can be identified by checking the reset flags in the Control/Status register, RCC_CSR.

These sources act on the NRST pin and it is always kept low during the delay phase. The RESET service routine vector is fixed at address 0x0000_0004 in the memory map.

The system reset signal provided to the device is output on the NRST pin. The pulse generator guarantees a minimum reset pulse duration of 20 µs for each internal reset source. In case of an external reset, the reset pulse is generated while the NRST pin is asserted low.

In case on an internal reset, the internal pull-up R_{PU} is deactivated in order to save the power consumption through the pull-up resistor.

Figure 5. Simplified diagram of the reset circuit



Software reset

The SYSRESETREQ bit in Cortex®-M4 Application Interrupt and Reset Control Register must be set to force a software reset on the device (refer to the STM32F3xx/F4xx/L4xx Cortex®-M4 programming manual (PM0214)).

Low-power mode security reset

To prevent that critical applications mistakenly enter a low-power mode, two low-power mode security resets are available. If enabled in option bytes, the resets are generated in the following conditions:

1. Entering Standby mode: this type of reset is enabled by resetting nRST_STDBY bit in User option Bytes. In this case, whenever a Standby mode entry sequence is successfully executed, the device is reset instead of entering Standby mode.
2. Entering Stop mode: this type of reset is enabled by resetting nRST_STOP bit in User option bytes. In this case, whenever a Stop mode entry sequence is successfully executed, the device is reset instead of entering Stop mode.
3. Entering Shutdown mode: this type of reset is enabled by resetting nRST_SHDW bit in User option bytes. In this case, whenever a Shutdown mode entry sequence is successfully executed, the device is reset instead of entering Shutdown mode.

For further information on the User Option Bytes, refer to reference manual *section: Option bytes description*.

Option byte loader reset

The option byte loader reset is generated when the OBL_LAUNCH bit (bit 27) is set in the FLASH_CR register. This bit is used to launch the option byte loading by software.

Charging/discharging the pull-down capacitor through the internal resistor adds to the device power consumption. The recommended value of 100 nF for the capacitor can be reduced to 10 nF to limit power consumption.

1.3.4 Backup domain reset

The backup domain has two specific resets.

A backup domain reset is generated when one of the following events occurs:

1. Software reset, triggered by setting the BDRST bit in the *Backup domain control register (RCC_BDCR)*.
2. V_{DD} or V_{BAT} power on, if both supplies have previously been powered off.

A backup domain reset only affects the LSE oscillator, the RTC, the Backup registers and the RCC Backup domain control register.

2 Package

2.1 Package selection

Package should be selected by taking into account the constraints that are strongly dependent upon the application.

The list below summarizes the more frequent ones:

- Amount of interfaces required. Some interfaces might not be available on some packages. Some interfaces combinations might not be possible on some packages
- PCB technology constrains. Small pitch and high ball density could require more PCB layers and higher class PCB
- Package height
- PCB available area
- Noise emission or signal integrity of high speed interfaces.

  Smaller packages usually provide better signal integrity. This is further enhanced as Small pitch and high ball density requires multilayer PCBs which allow better supply/ground distribution.
- Compatibility with other devices.

Table 1. Package summary (excluding WCSP)

Package type	LQFP64	LQFP100	LQFP144	UFBGA132
Size (mm)(1)	10 x 10	14 x 14	20 x 20	7 x 7
Pitch (mm)	0.5	0.5	0.5	0.5
Height (mm)	1.6	1.6	1.6	0.6
Reference products	STM32L486xx / 476xx			

1. Body size, excluding pins

Table 2. WCSP package summary

Package type	WCSP
Number of balls	72
Size (mm)	4.4284 x 3.7784
Pitch (mm)	0.4
Height (mm)	0.585
Reference products	STM32L486xx / 476xx

2.2 Pinout compatibility

Table 3 below allows to select the right package depending on required signals.

Table 3. Pinout summary

Pin name	Packages and pin number				
	LQFP			UFBGA	WCSP
	64	100	144	132	72
Specific IOs availability					
PC14/OSC32_IN	X	X	X	X	X
PC15/OSC32_OUT	X	X	X	X	X
PH0/OSC_IN	X	X	X	X	X
PH1/OSC_OUT	X	X	X	X	X
PC3/VLCD	X	X	X	X	X
System related pins					
BOOT0	X	X	X	X	X
NRST	X	X	X	X	X
Supplies pins					
VBAT	X	X	X	X	X
VDDUSB	X	X	X	X	X
VSSA	X	X	X	X	X
VREF-	-	X	X	X	-
VREF+	-	X	X	X	X
VDDA	X	X	X	X	X
VDDIO2	-	-	X	X	X
number of VDD(1)	3	5	9	6	3
number of VSS	4	5	11	7	4

1. One single tantalum or ceramic capacitor (min. 4.7 µF, typ.10 µF) for the package + one 100 nF ceramic capacitor for each V_{DD} pin.

3 Clocks

Four different clock sources can be used to drive the system clock (SYSCLK):

- HSI (high speed internal)16 MHz RC oscillator clock
- MSI (multispeed internal) RC oscillator clock
- HSE oscillator clock, from 4 to 48 MHz
- PLL clock

The MSI is used as system clock source after startup from Reset, configured at 4 MHz.

The devices have the following additional clock sources:

- 32 kHz low speed internal RC (LSI RC) which drives the independent watchdog and optionally the RTC used for Auto-wakeup from Stop and Standby modes.
- 32.768 kHz low speed external crystal (LSE crystal) which optionally drives the real-time clock (RTCCLK).

Each clock source can be switched on or off independently when it is not used, to optimize power consumption.

Several prescalers can be used to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB, the APB1 and the APB2 domains is 80 MHz.

All the peripheral clocks are derived from their bus clock (HCLK, PCLK1 or PCLK2) except:

- The 48 MHz clock, used for USB OTG FS, SDMMC and RNG. This clock is derived (selected by software) from one of the three following sources:
  - main PLL VCO (PLLUSB1CLK)
  - PLLSAI1 VCO (PLLUSB2CLK)
  - MSI clock.

  When the MSI clock is auto-trimmed with the LSE, it can be used by the USB OTG FS device.
- The ADCs clock which is derived (selected by software) from one of the three following sources:
  - system clock (SYSCLK)
  - PLLSAI1 VCO (PLLADC1CLK)
  - PLLSAI2 VCO (PLLADC2CLK).
- The U(S)ARTs clocks which are derived (selected by software) from one of the four following sources:
  - system clock (SYSCLK)
  - HSI clock
  - LSE clock
  - APB1 or APB2 clock (PCLK1 or PCLK2 depending on which APB is mapped the U(S)ART)

  The wakeup from Stop mode is supported only when the clock is HSI or LSE.
- The I^2Cs clocks which are derived (selected by software) from one of the three following sources:
  - system clock (SYSCLK)
  - HSI clock
  - APB1 clock (PCLK1)

  The wakeup from Stop mode is supported only when the clock is HSI.
- The SAI1 and SAI2 clocks which are derived (selected by software) from one of the four following sources:
  - an external clock mapped on SAI1_EXTCLK for SAI1 and SAI2_EXTCLK for SAI2.
  - PLLSAI1 VCO (PLLSAI1CLK)
  - PLLSAI2 VCO (PLLSAI2CLK)
  - main PLL VCO (PLLSAI3CLK)
- The SWPMI1 clock which is derived (selected by software) from one of the two following sources:
  - HSI clock
  - APB1 clock (PCLK1)

  The wakeup from Stop mode is supported only when the clock is HSI.
- The low-power timers (LPTIMx) clock which are derived (selected by software) from one of the five following sources:
  - LSI clock
  - LSE clock
  - HSI clock

- APB1 clock (PCLK1)
- External clock mapped on LPTIMx_IN1

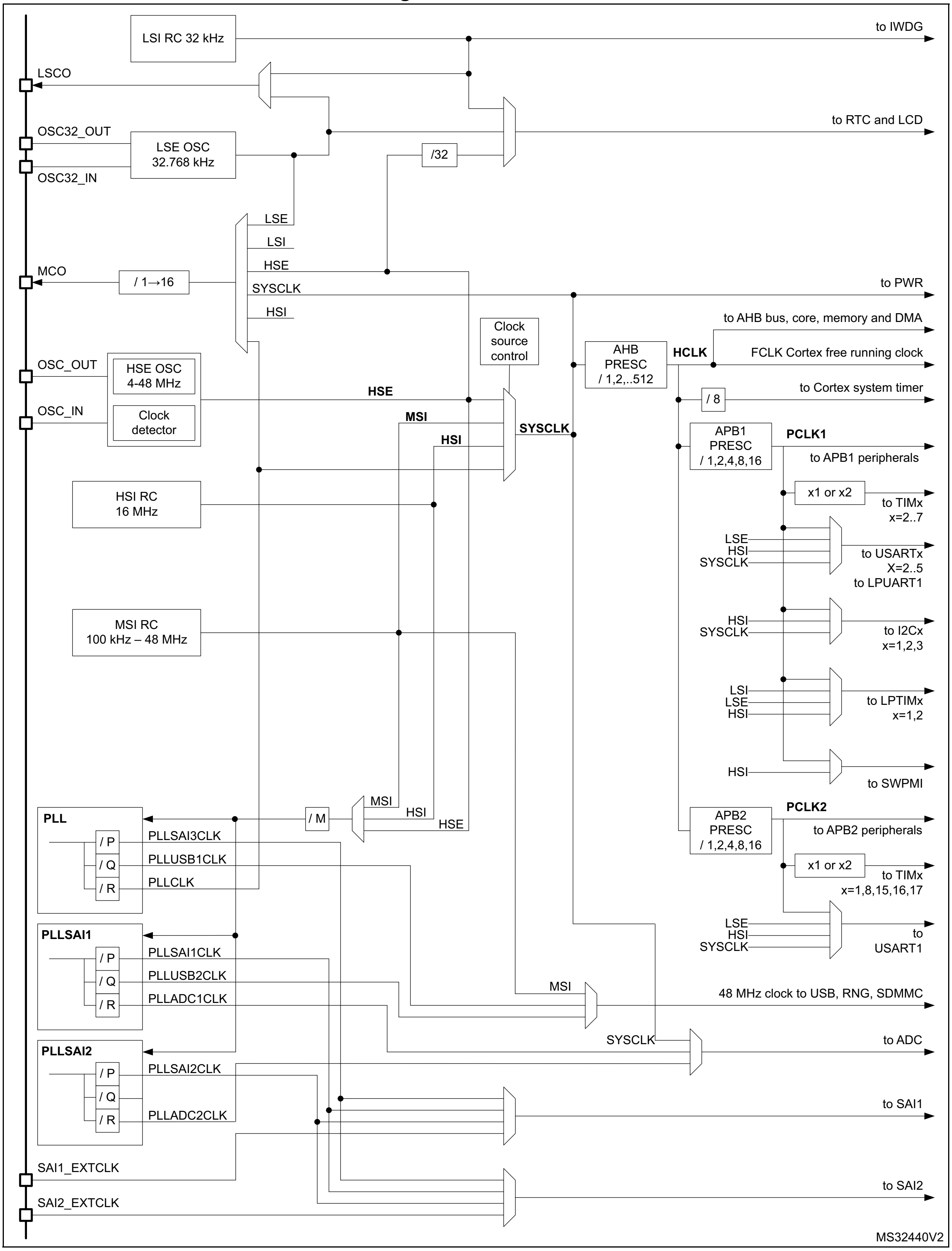
The functionality in Stop mode (including wakeup) is supported only when the clock is LSI or LSE, or in external clock mode.

- The RTC and LCD clock which is derived (selected by software) from one of the three following sources:
  - LSE clock
  - LSI clock
  - HSE clock divided by 32

  The functionality in Stop mode (including wakeup) is supported only when the clock is LSI or LSE.
- The IWDG clock which is always the LSI clock.

The RCC feeds the Cortex® System Timer (SysTick) external clock with the AHB clock (HCLK) divided by 8. The SysTick can work either with this clock or directly with the Cortex® clock (HCLK), configurable in the SysTick Control and Status Register.

Figure 6. Clock tree



1. For full details about the internal and external clock source characteristics, please refer to the “Electrical

characteristics” section in your device datasheet.

2. The ADC clock can be derived from the AHB clock of the ADC bus interface, divided by a programmable factor (1, 2 or 4). When the programmable factor is ‘1’, the AHB prescaler must be equal to ‘1’.

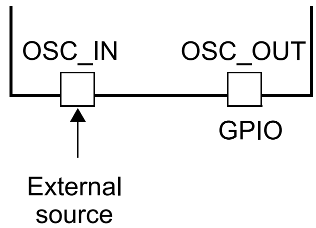
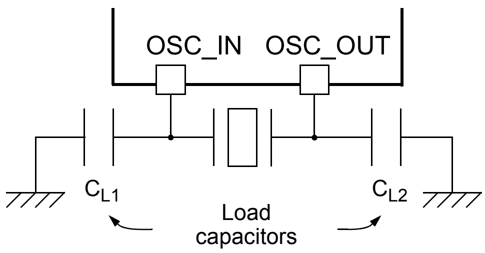
3.1 HSE clock

The high speed external clock signal (HSE) can be generated from two possible clock sources:

- HSE external crystal/ceramic resonator
- HSE user external clock

The resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

Figure 7. HSE/ LSE clock sources

Clock source	Hardware configuration
External clock	
Crystal/Ceramic resonators	

1. The value of R_{EXT} depends on the crystal characteristics. A typical value is in the range of 5 to 6 R_S (resonator series resistance).To fine tune the REXT value, refer to AN2867(Oscillator design guide for ST microcontrollers)
2. Load capacitance, C_L, has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where: C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF. Please refer to *Section 6.4: Decoupling* to minimize its value.

3.1.1 External crystal/ceramic resonator (HSE crystal)

The 4- to 48-MHz external oscillator has the advantage of producing a very accurate rate on the main clock.

The associated hardware configuration is shown in *Figure 7*. Refer to the electrical characteristics section of the *datasheet* for more details.

The HSERDY flag in the *Clock control register (RCC_CR)* indicates if the HSE oscillator is stable or not. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the *Clock interrupt enable register (RCC_CIER)*.

The HSE Crystal can be switched on and off using the HSEON bit in the *Clock control register (RCC_CR)*.

3.1.2 External source (HSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 48 MHz. You select this mode by setting the HSEBYP and HSEON bits in the *Clock control register (RCC_CR)*. The external clock signal (square, sinus or triangle) with ~40-60 % duty cycle depending on the frequency (refer to the datasheet) has to drive the OSC_IN pin while the OSC_OUT pin can be used a GPIO. See *Figure 7*.

3.2 HSI clock

The HSI clock signal is generated from an internal 16 MHz RC Oscillator.

The HSI RC oscillator has the advantage of providing a clock source at low cost (no external components). It also has a faster startup time than the HSE crystal oscillator however, even with calibration the frequency is less accurate than an external crystal oscillator or ceramic resonator.

The HSI clock can be selected as system clock after wakeup from Stop modes (Stop 0, Stop 1 or Stop 2). Refer to reference manual *section: Low-power modes*. It can also be used as a backup clock source (auxiliary clock) if the HSE crystal oscillator fails. Refer to reference manual *section: Clock security system (CSS)*.

3.2.1 Calibration

RC oscillator frequencies can vary from one chip to another due to manufacturing process variations, this is why each device is factory calibrated by ST for 1 % accuracy at T_A=25°C.

After reset, the factory calibration value is loaded in the HSICAL[7:0] bits in the *Internal clock sources calibration register (RCC_ICSCR)*.

If the application is subject to voltage or temperature variations this may affect the RC oscillator speed. You can trim the HSI frequency in the application using the HSITRIM[4:0] bits in the *Internal clock sources calibration register (RCC_ICSCR)*.

For more details on how to measure the HSI frequency variation, refer to reference manual *section: Internal/external clock measurement with TIM15/TIM16/TIM17*.

The HSIRDY flag in the *Clock control register (RCC_CR)* indicates if the HSI RC is stable or not. At startup, the HSI RC output clock is not released until this bit is set by hardware.

The HSI RC can be switched on and off using the HSION bit in the *Clock control register (RCC_CR)*.

The HSI signal can also be used as a backup source (Auxiliary clock) if the HSE crystal oscillator fails. Refer to reference manual *section: Clock security system (CSS)*.

3.3 MSI clock

The MSI clock signal is generated from an internal RC oscillator. Its frequency range can be adjusted by software by using the MSIRANGE[3:0] bits in the *Clock control register (RCC_CR)*. Twelve frequency ranges are available: 100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz and 48 MHz.

The MSI clock is used as system clock after restart from Reset, wakeup from Standby and Shutdown low-power modes. After restart from Reset, the MSI frequency is set to its default value 4 MHz. Refer to reference manual *section: Low-power modes*.

The MSI clock can be selected as system clock after a wakeup from Stop mode (Stop0, Stop 1 or Stop 2). Refer to reference manual s*ection: Low-power modes*. It can also be used as a backup clock source (auxiliary clock) if the HSE crystal oscillator fails. Refer to reference manual *section: Clock security system (CSS)*.

The MSI RC oscillator has the advantage of providing a low-cost (no external components) low-power clock source. In addition, when used in PLL-mode with the LSE, it provides a very accurate clock source which can be used by the USB OTG FS device, and feed the main PLL to run the system at the maximum speed 80 MHz.

The MSIRDY flag in the *Clock control register (RCC_CR)* indicates whether the MSI RC is stable or not. At startup, the MSI RC output clock is not released until this bit is set by hardware. The MSI RC can be switched on and off by using the MSION bit in the *Clock control register (RCC_CR)*.

3.3.1 Hardware auto calibration with LSE (PLL-mode)

When a 32.768 kHz crystal is present in the application, it is possible to configure the MSI in a PLL-mode by setting the MSIPLLEN bit in the *Clock control register (RCC_CR)*. When configured in PLL-mode, the MSI automatically calibrates itself thanks to the LSE. This mode is available for all MSI frequency ranges. At 48 MHz, the MSI in PLL-mode can be used for the USB OTG FS device, saving the need of an external high-speed crystal.

3.3.2 Software calibration

The MSI RC oscillator frequency can vary from one chip to another due to manufacturing process variations, this is why each device is factory calibrated by ST for 1 % accuracy at an ambient temperature, TA, of 25 °C. After reset, the factory calibration value is loaded in the MSICAL[7:0] bits in the *Internal clock sources calibration register (RCC_ICSCR)*. If the application is subject to voltage or temperature variations, this may affect the RC oscillator speed. You can trim the MSI frequency in the application by using the MSITRIM[7:0] bits in the RCC_ICSCR register. For more details on how to measure the MSI frequency variation please refer to reference manual *section: Internal/external clock measurement with TIM15/TIM16/TIM17*.

3.4 PLL

The device embeds 3 PLLs: PLL, PLLSAI1, PLLSAI2. Each PLL provides up to three independent outputs. The internal PLLs can be used to multiply the HSI, HSE or MSI output clock frequency. The PLLs input frequency must be between 4 and 8 MHz. The selected clock source is divided by a programmable factor PLLM from 1 to 8 to provide a clock frequency in the requested input range. Refer to *Figure 6: Clock tree* and *PLL configuration register (RCC_PLLCFGR)*.

The PLLs configuration (selection of the input clock and multiplication factor) must be done before enabling the PLL. Once the PLL is enabled, these parameters cannot be changed.

To modify the PLL configuration, proceed as follows:

1. Disable the PLL by setting PLLON to 0 in *Clock control register (RCC_CR)*.
2. Wait until PLLRDY is cleared. The PLL is now fully stopped.
3. Change the desired parameter.
4. Enable the PLL again by setting PLLON to 1.
5. Enable the desired PLL outputs by configuring PLLPEN, PLLQEN, PLLREN in *PLL configuration register (RCC_PLLCFGR)*.

An interrupt can be generated when the PLL is ready, if enabled in the *Clock interrupt enable register (RCC_CIER)*.

The same procedure is applied for changing the configuration of the PLLSAI1 or PLLSAI2:

1. Disable the PLLSAI1/PLLSAI2 by setting PLLSAI1ON/PLLSAI2ON to 0 in *Clock control register (RCC_CR)*.
2. Wait until PLLSAI1RDY/PLLSAI2RDY is cleared. The PLLSAI1/PLLSAI2 is now fully stopped.
3. Change the desired parameter.
4. Enable the PLLSAI1/PLLSAI2 again by setting PLLSAI1ON/PLLSAI2ON to 1.
5. Enable the desired PLL outputs by configuring PLLSAI1PEN/PLLSAI2PEN, PLLSAI1QEN/PLLSAI2QEN, PLLSAI1REN/PLLSAI2REN in *PLLSAI1 configuration register (RCC_PLLSAI1CFGR)* and *PLLSAI2 configuration register (RCC_PLLSAI2CFGR)*.

The PLL output frequency must not exceed 80 MHz.

The enable bit of each PLL output clock (PLLPEN, PLLQEN, PLLREN, PLLSAI1PEN, PLLSAI1QEN, PLLSAI1REN, PLLSAI2PEN and PLLSAI2REN) can be modified at any time without stopping the corresponding PLL. PLLREN cannot be cleared if PLLCLK is used as system clock.

3.5 LSE clock

The LSE crystal is a 32.768 kHz Low Speed External crystal or ceramic resonator. It has the advantage of providing a low-power but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The LSE crystal is switched on and off using the LSEON bit in *Backup domain control register (RCC_BDCR)*. The crystal oscillator driving strength can be changed at runtime using the LSEDRV[1:0] bits in the *Backup domain control register (RCC_BDCR)* to obtain the best compromise between robustness and short start-up time on one side and low-power-consumption on the other side. The LSE drive can be decreased to the lower drive capability (LSEDRV=00) when the LSE is ON. However, once LSEDRV is selected, the drive capability can not be increased if LSEON=1.

The LSERDY flag in the *AHB1 peripheral clocks enable in Sleep and Stop modes register (RCC_AHB1SMENR)* indicates whether the LSE crystal is stable or not. At startup, the LSE crystal output clock signal is not released until this bit is set by hardware. An interrupt can be generated if enabled in the *Clock interrupt enable register (RCC_CIER)*.

3.5.1 External source (LSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 1 MHz. You select this mode by setting the LSEBYP and LSEON bits in the *AHB1 peripheral clocks enable in Sleep and Stop modes register (RCC_AHB1SMENR)*. The external clock signal (square, sinus or triangle) with ~50 % duty cycle has to drive the OSC32_IN pin while the OSC32_OUT pin can be used as GPIO. See *Figure 7*.

3.6 LSI clock

The LSI RC acts as a low-power clock source that can be kept running in Stop and Standby mode for the independent watchdog (IWDG), RTC and LCD. The clock frequency is 32 kHz. For more details, refer to the electrical characteristics section of the datasheets.

The LSI RC can be switched on and off using the LSION bit in the *Control/status register (RCC_CSR)*.

The LSIRDY flag in the *Control/status register (RCC_CSR)* indicates if the LSI oscillator is stable or not. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the *Clock interrupt enable register (RCC_CIER)*.

3.7 System clock (SYSCLK) selection

Four different clock sources can be used to drive the system clock (SYSCLK):

- MSI oscillator
- HSI oscillator
- HSE oscillator
- PLL

The system clock maximum frequency is 80 MHz. After a system reset, the MSI oscillator, at 4 MHz, is selected as system clock. When a clock source is used directly or through the PLL as a system clock, it is not possible to stop it.

A switch from one clock source to another occurs only if the target clock source is ready (clock stable after startup delay or PLL locked). If a clock source which is not yet ready is selected, the switch will occur when the clock source becomes ready. Status bits in the *Internal clock sources calibration register (RCC_ICSCR)* indicate which clock(s) is (are) ready and which clock is currently used as a system clock.

4 Boot configuration

In the STM32L4x6, three different boot modes can be selected through the BOOT0 pin and nBOOT1 bit in the User option byte, as shown in the following table.

Table 4. Boot modes

Boot mode selection		Boot mode	Aliasing
BOOT1[(1)]	BOOT0		
x	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM1	Embedded SRAM1 is selected as boot space

1. The BOOT1 value is the opposite of the nBOOT1 Option Bit.

The values on both BOOT0 pin and nBOOT1 bit are latched after a reset. It is up to the user to set nBOOT1 and BOOT0 to select the required boot mode.

The BOOT0 pin and nBOOT1 bit are also re-sampled when exiting from Standby mode. Consequently they must be kept in the required Boot mode configuration in Standby mode. After this startup delay has elapsed, the CPU fetches the top-of-stack value from address 0x0000 0000, then starts code execution from the boot memory at 0x0000 0004.

Depending on the selected boot mode, main Flash memory, system memory or SRAM1 is accessible as follows:

- Boot from main Flash memory: the main Flash memory is aliased in the boot memory space (0x0000 0000), but still accessible from its original memory space (0x0800 0000). In other words, the Flash memory contents can be accessed starting from address 0x0000 0000 or 0x0800 0000.
- Boot from system memory: the system memory is aliased in the boot memory space (0x0000 0000), but still accessible from its original memory space (0x1FFF 0000).
- Boot from the embedded SRAM1: the SRAM1 is aliased in the boot memory space (0x0000 0000), but it is still accessible from its original memory space (0x2000 0000).

Note: When the device boots from SRAM, in the application initialization code, you have to relocate the vector table in SRAM using the NVIC exception table and the offset register.

When booting from the main Flash memory, the application software can either boot from bank 1 or from bank 2. By default, boot from bank 1 is selected.
To select boot from Flash memory bank 2, set the BFB2 bit in the user option bytes. When this bit is set and the boot pins are in the boot from main Flash memory configuration, the device boots from system memory, and the boot loader jumps to execute the user application programmed in Flash memory bank 2. For further details, please refer to AN2606.

Note: When booting from bank 2, in the application initialization code, you have to relocate the vector table to bank 2 base address. (0x0808 0000) using the NVIC exception table and offset register.

4.1 Physical remap

Once the boot pins are selected, the application software can modify the memory accessible in the code area (in this way the code can be executed through the ICode bus in place of the System bus). This modification is performed by programming the *SYSCFG memory remap register (SYSCFG_MEMRMP)* in the SYSCFG controller.

The following memories can thus be remapped:

- Main Flash memory
- System memory
- Embedded SRAM1 (112 KB)
- FSMC bank 1 (NOR/PSRAM 1 and 2)
- Quad SPI memory

4.2 Embedded boot loader

The embedded boot loader is located in the System memory, programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces:

- USART1 on pins PA9/PA10, USART2 on pins PA2/PA3, USART3 on pins PC10/PC11
- I2C1 on pins PB6/PB7, I2C2 on pins PB10/PB11, I2C3 on pins PC0/PC1
- SPI1 on pins PA4/PA5/PA6/PA7, SPI2 on pins PB12/PB13/PB14/PB15, SPI3 on pins PA15/PC10/PC11/PC12
- USB DFU interface on pins PA11/PA12

4.3 BOOT0 pin connection

The BOOT0 pin of the STM32L4 series has a lower VIL than the other GPIO, (for details see datasheet I/O static characteristics), thus as it does not fit CMOS requirement, when driven by another CMOS circuit the signal level must be verified.

5 Debug management

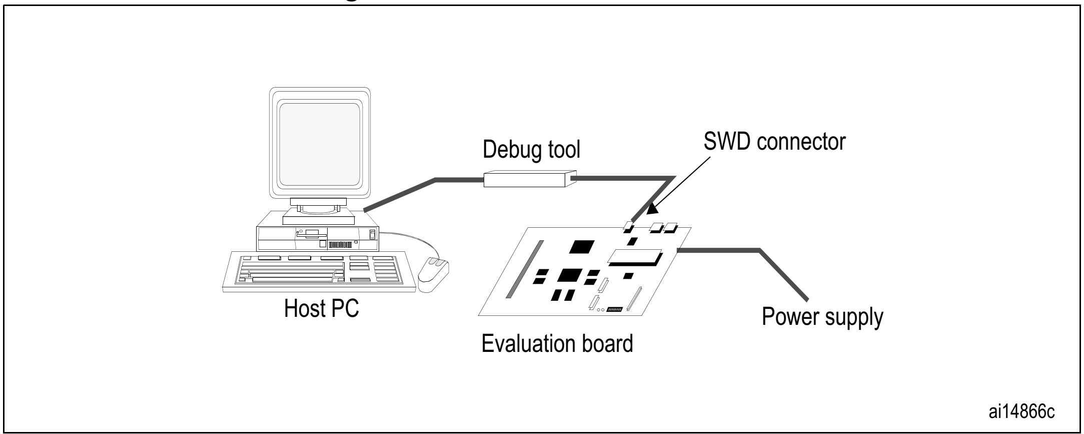
5.1 Introduction

In the SWJ-DP, the two JTAG pins of the SW-DP are multiplexed with some of the five JTAG pins of the JTAG-DP.

The host/target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a SW connector and a cable connecting the host to the debug tool.

Figure 8 shows the connection of the host to a development board.

Figure 8. Host-to-board connection



The Nucleo demonstration board embeds the debug tools (ST-LINK) so it can be directly connected to the PC through an USB cable. The ST-LINK requires by default to have an enumeration with a host that is able to supply 100 mA to power the STM32L4 MCU, hence user shall use jumper JP1 on the Nucleo board which can be set in case maximum current consumption on U5V does not exceed 100 mA.

5.2 SWJ debug port (JTAG and serial wire)

The STM32L4 series core integrates the serial wire / JTAG debug port (SWJ-DP). It is an ARM® standard CoreSight™ debug port that combines a JTAG-DP (5-pin) interface and a SW-DP (2-pin) interface.

- The JTAG debug port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port
- The serial wire debug port (SW-DP) provides a 2-pin (clock + data) interface to the AHP-AP port

5.3 Pinout and debug port pins

The STM32L4 MCU is offered in various packages with different numbers of available pins. As a result, some functionality related to the pin availability may differ from one package to another.

5.3.1 SWJ debug port pins

Five pins are used as outputs for the SWJ-DP as *alternate functions* of general-purpose I/Os (GPIOs). These pins, shown in *Table 5*, are available on all packages.

Table 5. Debug port pin assignment

SWJ-DP pin name	JTAG debug port		SW debug port		Pin assignment
	Type	Description	Type	Debug assignment	
JTMS/SWDIO	I	JTAG test mode selection	I/O	Serial wire data input/output	PA13
JTCK/SWCLK	I	JTAG test clock	I	Serial wire clock	PA14
JTDI	I	JTAG test data input	-	-	PA15
JTDO/TRACESWO	O	JTAG test data output	-	TRACESWO if async trace is enabled	PB3
JNTRST	I	JTAG test nReset	-	-	PB4

5.3.2 Flexible SWJ-DP pin assignment

After reset (SYSRESETn or PORESETn), all five pins used for the SWJ-DP are assigned as dedicated pins which are immediately usable by the debugger host (note that the trace outputs are not assigned except if explicitly programmed by the debugger host).

However, the STM32L4 MCU implements a register to disable all or part of the SWJ-DP port, and so releases the associated pins for general-purpose I/O usage. This register is mapped on an APB bridge connected to the Cortex®-M4 system bus. It is programmed by the user software program and not by the debugger host.

Table 6 shows the different possibilities for releasing some pins. For more details, see the STM32L4x6 advanced ARM®-based 32-bit MCUs reference manual (RM0351).

Table 6. SWJ I/O pin availability

Available debug ports	SWJ I/O pin assigned				
	PA13 / JTMS/ SWDIO	PA14 / JTCK/ SWCLK	PA15 / JTDI	PB3 / JTDO	PB4/ JNTRST
Full SWJ (JTAG-DP + SW-DP) - reset state	X	X	X	X	X
Full SWJ (JTAG-DP + SW-DP) but without JNTRST	X	X	X	X	
JTAG-DP disabled and SW-DP enabled	X	X			
JTAG-DP disabled and SW-DP disabled	Released				

5.3.3 Internal pull-up and pull-down resistors on JTAG pins

The JTAG input pins must *not* be floating since they are directly connected to flip-flops which control the debug mode features. Special care must be taken with the SWCLK/TCK pin that is directly connected to the clock of some of these flip-flops.

To avoid any uncontrolled I/O levels, the STM32L4 series embeds internal pull-up and pull-down resistors on the JTAG input pins:

- JNTRST: internal pull-up
- JTDI: internal pull-up
- JTMS/SWDIO: internal pull-up
- TCK/SWCLK: internal pull-down

Once a JTAG I/O is released by the user software, the GPIO controller takes control again. The reset states of the GPIO control registers put the I/Os in the following equivalent states:

- JNTRST: input pull-up
- JTDI: input pull-up
- JTMS/SWDIO: input pull-up
- JTCK/SWCLK: input pull-down
- JTDO: input floating

The software can then use these I/Os as standard GPIOs.

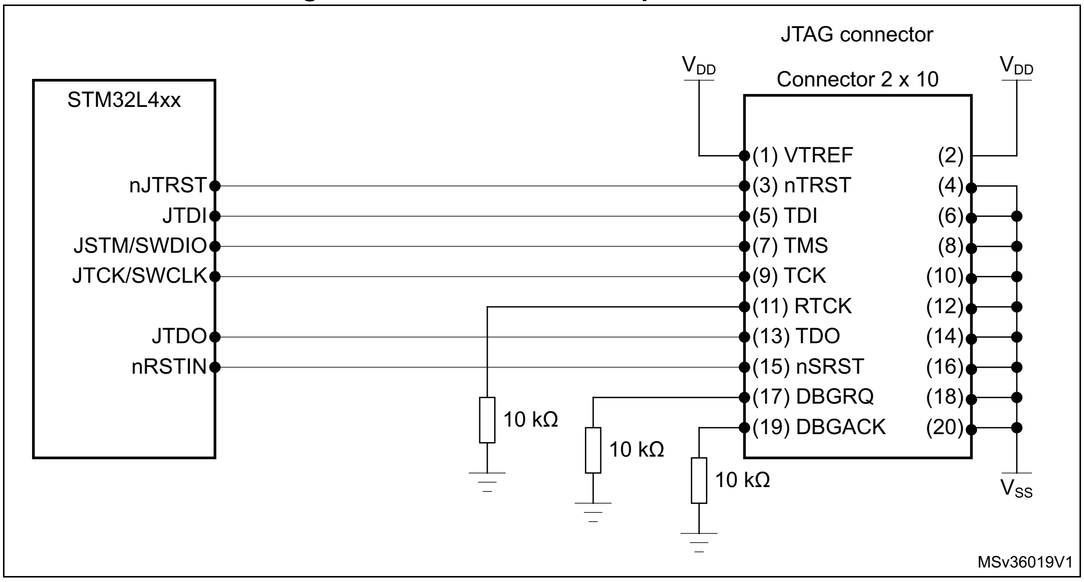
Note: *The JTAG IEEE standard recommends to add pull-up resistors on TDI, TMS and nTRST but, there is no special recommendation for TCK. However, for the* STM32L4 *series, an integrated pull-down resistor is used for JTCK.*

Having embedded pull-up and pull-down resistors removes the need to add external resistors.

5.3.4 SWJ debug port connection with standard JTAG connector

Figure 9 shows the connection between the STM32L4 MCU and a standard JTAG connector.

Figure 9. JTAG connector implementation



5.4 Serial wire debug (SWD) pin assignment

The same SWD pin assignment is available on all STM32L4 series packages.

Table 7. SWD port pins

SWD pin name	SWD port		Pin assignment
	Type	Debug assignment	
SWDIO	I/O	Serial wire data input/output	PA13
SWCLK	I	Serial wire clock	PA14

5.4.1 SWD pin assignment

After reset (SYSRESETn or PORESETn), the pins used for the SWD are assigned as dedicated pins which are immediately usable by the debugger host.

However, the MCU offers the possibility to disable the SWD, therefore releasing the associated pins for general-purpose I/O (GPIO) usage. For more details on how to disable SWD port, refer to the RM0351 reference manual section on I/O pin alternate function multiplexer and mapping.

5.4.2 Internal pull-up and pull-down on SWD pins

Once the SWD I/O is released by the user software, the GPIO controller takes control of these pins. The reset states of the GPIO control registers put the I/Os in the equivalent states:

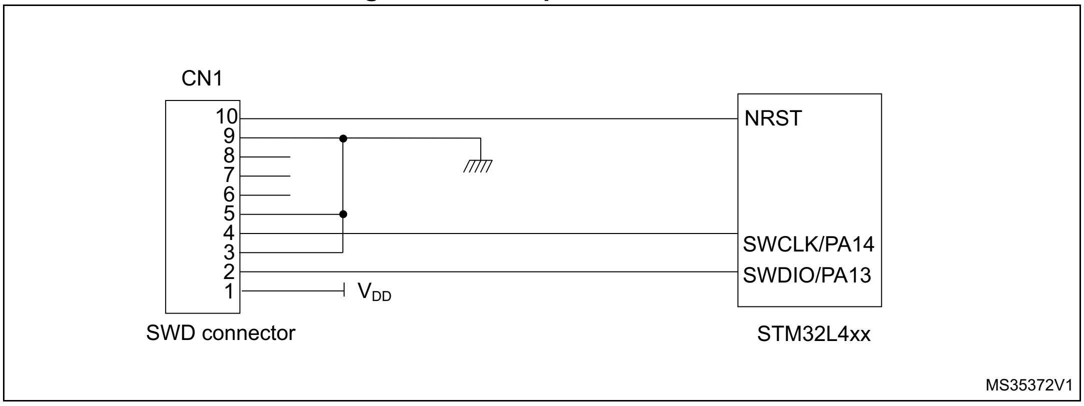
- SWDIO: alternate function pull-up
- SWCLK: alternate function pull-down

Having embedded pull-up and pull-down resistors removes the need to add external resistors.

5.4.3 SWD port connection with standard SWD connector

Figure 10 shows the connection between the STM32L4 MCU and a standard SWD connector.

Figure 10. SWD port connection



6 Recommendations

6.1 Printed circuit board

For technical reasons, it is best to use a multilayer printed circuit board (PCB) with a separate layer dedicated to ground (V_{SS}) and another dedicated to the V_{DD} supply. This provides good decoupling and a good shielding effect. For many applications, economical reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for ground and for the power supply.

6.2 Component position

A preliminary layout of the PCB must make separate circuits:

- High-current circuits
- Low-voltage circuits
- Digital component circuits
- Circuits separated according to their EMI contribution. This will reduce cross-coupling on the PCB that introduces noise.

6.3 Ground and power supply (V_{SS}, V_{DD}, V_{SSA}, V_{DDA}, V_{DDUSB}, V_{DDIO2})

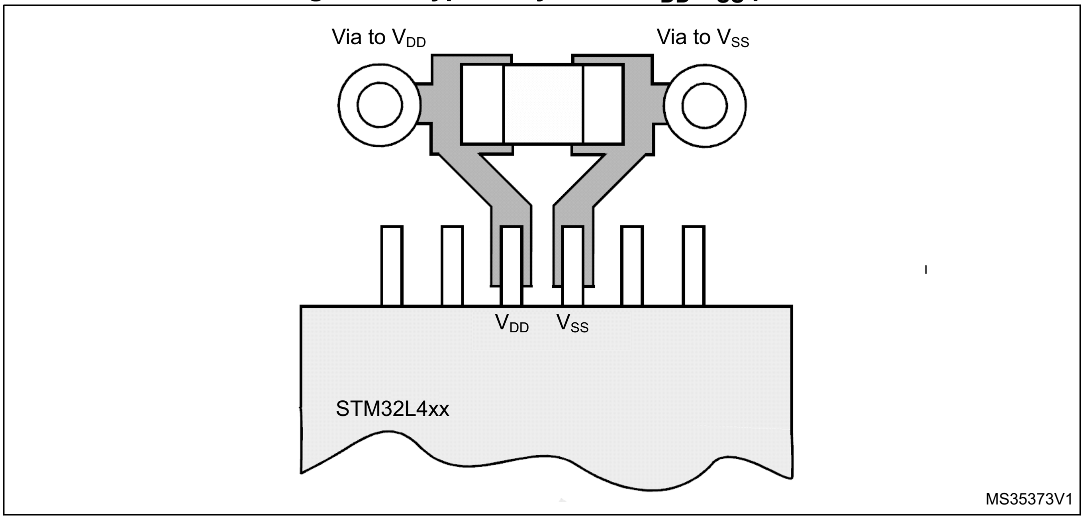
Every block (noisy, low-level sensitive, digital, etc.) should be grounded individually, and all ground returns should be to a single point. Loops must be avoided or have a minimum area. In order to improve analog performance, you must use separate supply sources for V_{DD} and V_{DDA}, and place the decoupling capacitors as close as possible to the device. The power supplies should be implemented close to the ground line to minimize the area of the supplies loop. This is due to the fact that the supply loop acts as an antenna, and acts as the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a kind of shielding (especially when using single-layer PCBs).

6.4 Decoupling

All power supply and ground pins must be properly connected to the power supplies. These connections, including pads, tracks and vias should have as low an impedance as possible. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair should be decoupled with filtering ceramic capacitors (100 nF) and a Tantalum or Ceramic capacitor of about 10 µF connected in parallel on the STM32L4 series device. Some package use a common VSS for several VDD instead of a pair of power supply (one VSS for each VDD), in that case the capacitors must be between each VDD and the common VSS.These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10 nF to 100 nF, but exact values depend on the application needs. *Figure 11* shows the typical layout of such a V_{DD}/V_{SS} pair.

Figure 11. Typical layout for V_{DD}/V_{SS} pair



6.5 Other signals

When designing an application, the EMC performance can be improved by closely studying the following:

- Signals for which a temporary disturbance affects the running process permanently (which is the case for interrupts and handshaking strobe signals but, not the case for LED commands).
  For these signals, a surrounding ground trace, shorter lengths, and the absence of noisy and sensitive traces nearby (crosstalk effect) improve EMC performance.
  For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (example, clock)
- Sensitive signals (example, high impedance)

6.6 Unused I/Os and features

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

To increase EMC performance and avoid extra power consumption, unused clocks, counters or I/Os, should not be left free. Unused I/O pins should be configured as analog input by software. The other options are to connect them to a fixed logic level 0 or 1 by an external or internal pull-up or pull-down or configure them as output mode using software.

7 Reference design

7.1 Description

The reference design shown in *Figure 12*, is based on the STM32L4 series LQFP144.

This reference design can be tailored to any STM32L4 series device with a different package, using the pin correspondence given in *Table 10: Reference connection for all packages*.

7.1.1 Clock

Two clock sources are used for the microcontroller:

- LSE: X2– 32.768 kHz crystal for the embedded RTC
- HSE: X1– 8 MHz crystal for the STM32L4 series microcontroller

Refer to *Section 3: Clocks*.

7.1.2 Reset

The reset signal in *Figure 12* is active low. The reset sources include:

- Reset button (B1)
- Debugging tools via the connector CN1

Refer to *Section 1.3: Reset and power supply supervisor*.

7.1.3 Boot mode

The boot option is configured by setting switches SW1 (Boot 0). Refer to *Section 4: Boot configuration*.

Note: When waking up from Standby mode, the Boot pin is sampled. In this situation, you need to pay attention to its value.

7.1.4 SWD interface

The reference design shows the connection between the STM32L4 MCU and a standard SWD connector. Refer to *Section 5: Debug management*.

Note: It is recommended to connect the reset pins so as to be able to reset the application from the tools.

7.1.5 Power supply

Refer to *Section 1: Power supplies*.

7.2 Component references

Table 8. Mandatory components

Reference	Component name	Value	Quantity	Comments
U1A	Microcontroller	STM32L4 series LQFP144	1	144-pin package
C8, C11, C13	Capacitor	100 nF	9 + 2	Ceramic capacitors (decoupling capacitors)
C9	Capacitor	4.7 µF	1	Tantalum / chemical / ceramic capacitor (decoupling capacitor)
C12	Capacitor	1 µF	1	Ceramic capacitor (LCD booster) only needed if LCD is used
C6, C10, C16	Capacitor	1 µF	3	Ceramic capacitor (decoupling capacitor)
C14, C15	Capacitor	1 µF	1	Ceramic capacitor (decoupling capacitor) used for Internal Voltage Reference buffer

Table 9. Optional components

Reference	Component name	Value	Quantity	Comments
R1	Resistor	390 Ω	1	Used for HSE: the value depends on the crystal characteristics, refer to application note AN2687
R3, R4, R5	Resistor	10 kΩ	3	Used for ST Link interface
C5	Capacitor	100 nF	1	Ceramic capacitor
C1, C2	Capacitor	6.8 pF	2	Used for LSE: the value depends on the crystal characteristics. Fits for MC-306 32.768K-E3, which has a load capacitance of 6 pF.
C3, C4	Capacitor	20 pF	2	Used for HSE: the value depends on the crystal characteristics, refer to application note AN2687
X1	Quartz	8 MHz	1	Used for HSE
X2	Quartz	32.764 kHz	1	Used for LSE
SW1	Switch	-	1	Used to select the right boot mode
B1	Push-button	-	1	-
L1	Ferrite bead	-	1	For EMC reduction on V_{DDA} supply, can be replaced by a direct connection between V_{DD} and V_{DDA}

Figure 12. Reference design STM32L4 series

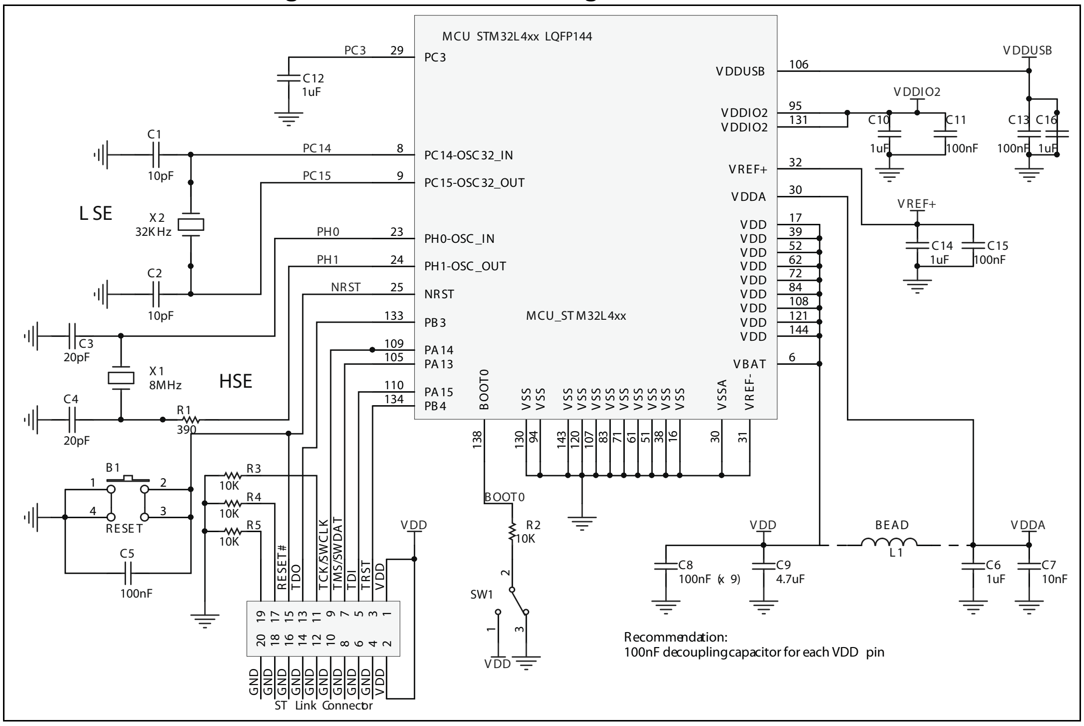


Table 10. Reference connection for all packages

Pin Name	Pin Number per Package				
	LQFP 64 pins	LQFP 100 pins	LQFP 144 pins	BGA 132 pins	CSP 72 pins
VBAT	1	6	6	E2	B9
PC14/OSC32_IN	3	8	8	D1	C9
PC15/OSC32_OUT	4	9	9	E1	C8
VSS	-	10	16	F2	-
VDD	-	11	17	G2	-
PH0/OSC_IN	5	12	23	F1	D9
PH1/OSC_OUT	6	13	24	G1	D8
NRST	7	14	25	H2	E9
PC3/VLCD	11	18	29	K2	G7
VSSA_ADC	12	19	30	J1	G9
VREF-		20	31		
VREF+	13	21	32	L1	G8
VDDA_ADC		22	33	M1	H9
VSS	18	27	38	E3	J9
VDD	19	28	39	H3	J8

Table 10. Reference connection for all packages (continued)

Pin Name	Pin Number per Package				
	LQFP 64 pins	LQFP 100 pins	LQFP 144 pins	BGA 132 pins	CSP 72 pins
VSS	-	-	51	-	-
VDD	-	-	52	-	-
VSS	-	-	61	F6	-
VDD	-	-	62	G6	-
VSS	31	49	71	F12	J2
VDD	32	50	72	G12	J1
VSS	-	-	83	-	-
VDD	-	-	84	-	-
VSS	-	-	94	-	-
VDD	-	-	95	-	-
PA13	46	72	105	A11	C2
VSS	47	-	-	-	B1
VDDUSB	48	73	106	C11	A1
VSS	-	74	107	F11	
VDD	-	75	108	G11	
PA14	49	76	109	A10	B2
VSS	-	-	120	-	-
VDD	-	-	121	-	-
VSS	-	-	130	F7	-
VDDIO_2	-	-	131	G7	B6
BOOT0	60	94	138	A4	D7
VSS	63	99	143	D3	A8
VDD	64	100	144	C4	A9

8 Revision history

Table 11. Document revision history

Date	Revision	Changes
16-Jul-2015	1	Initial release.
05-Jan-2016	2	*Section 3.2: HSI clock* updated: Stop 0 mode added *Section 3.3: MSI clock* updated: Stop 0 mode added