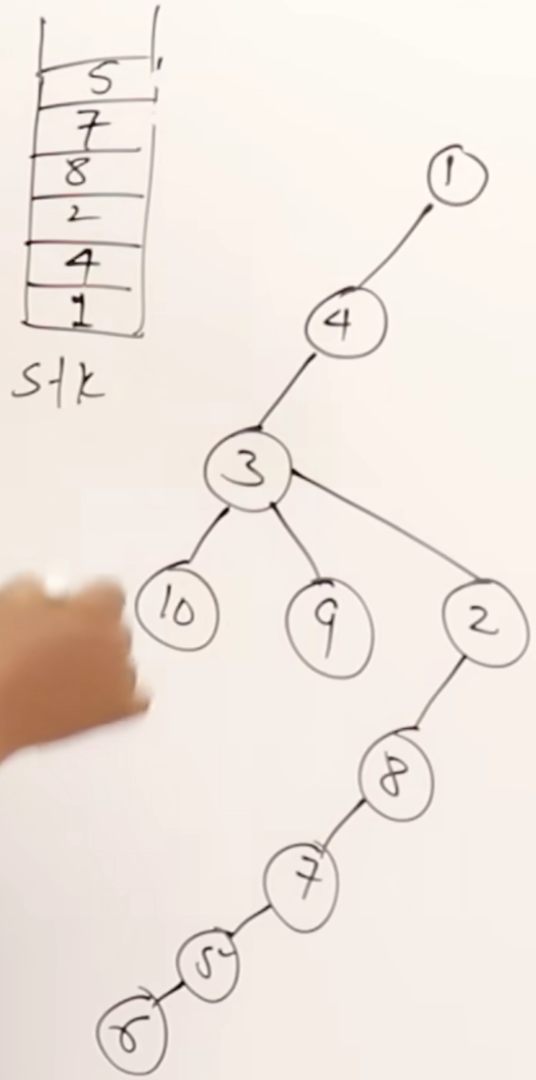
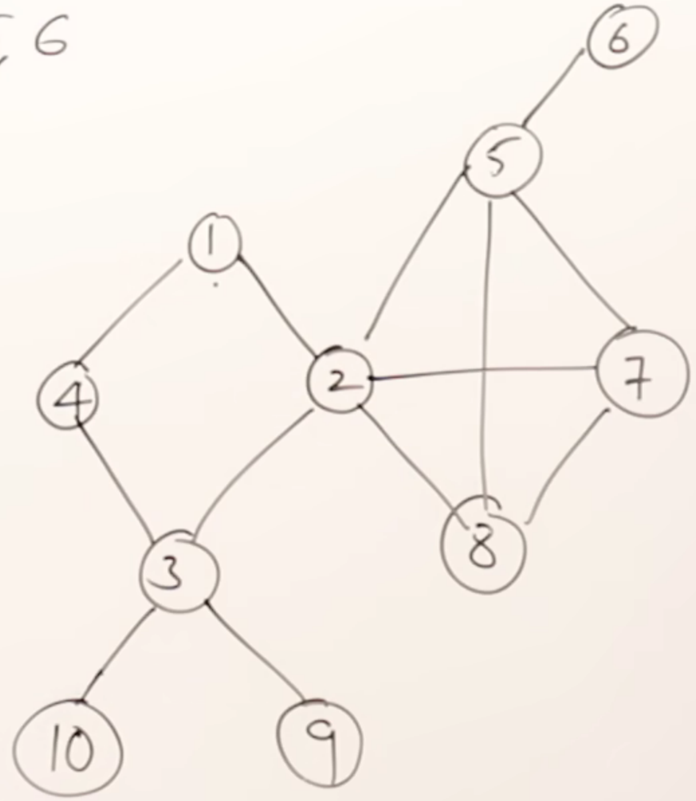
BFS & DFS

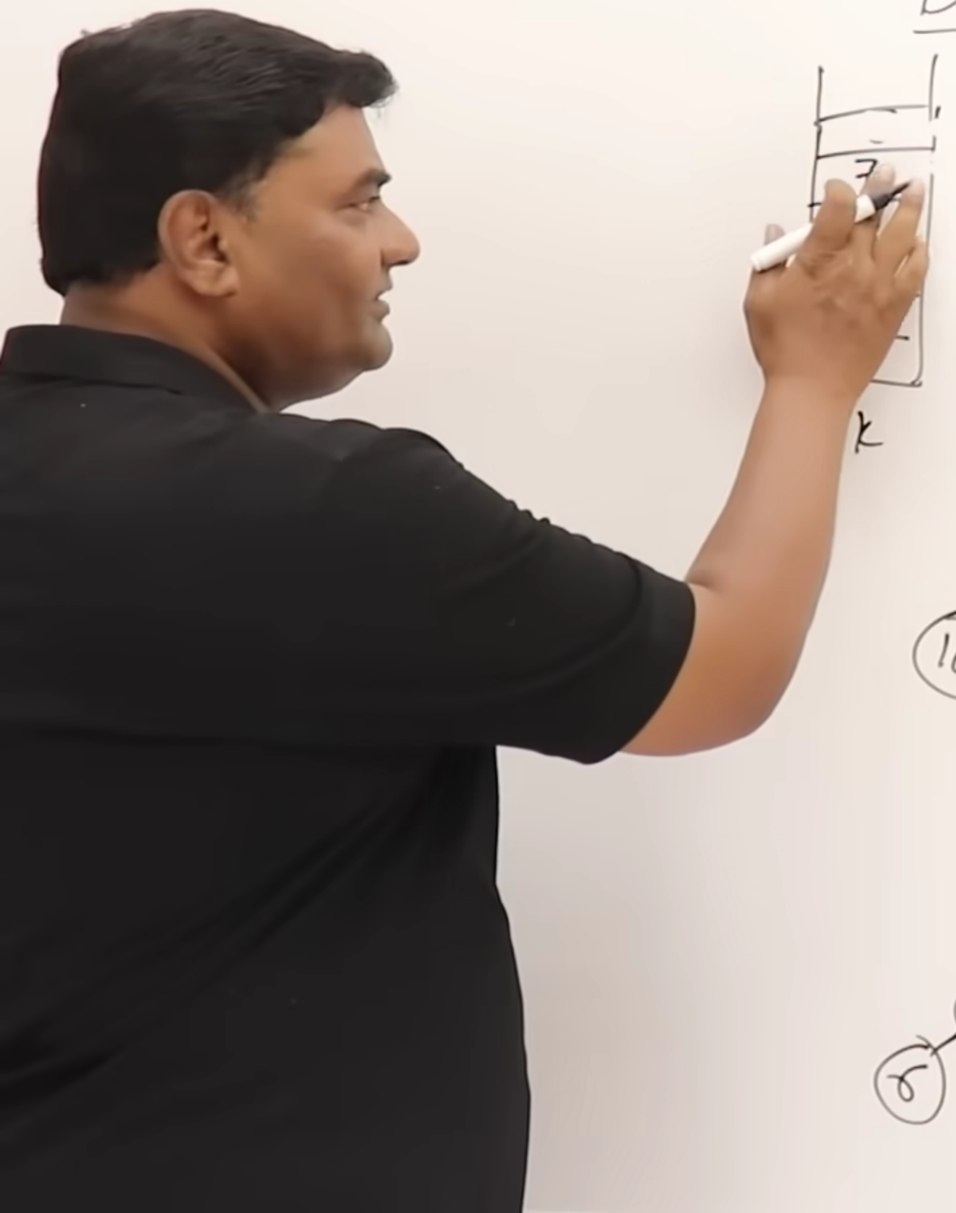
DFS: 1, 4, 3, 10, 9, 2, 8, 7, 5, 6

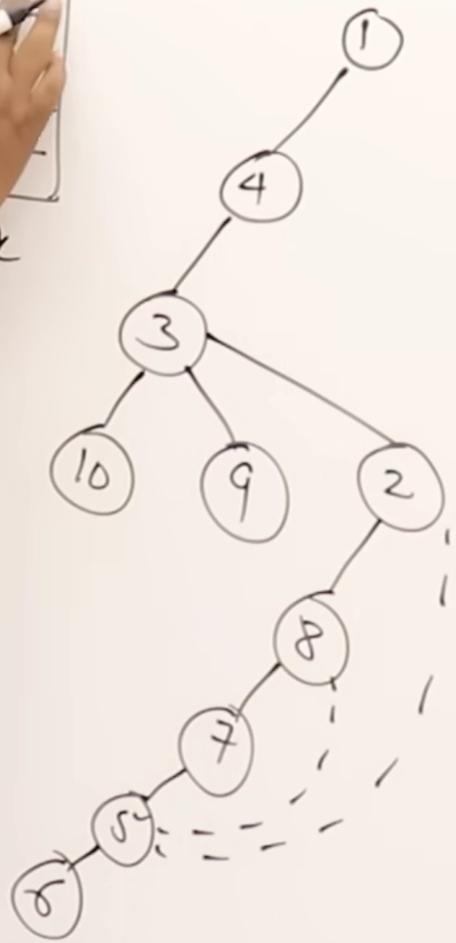


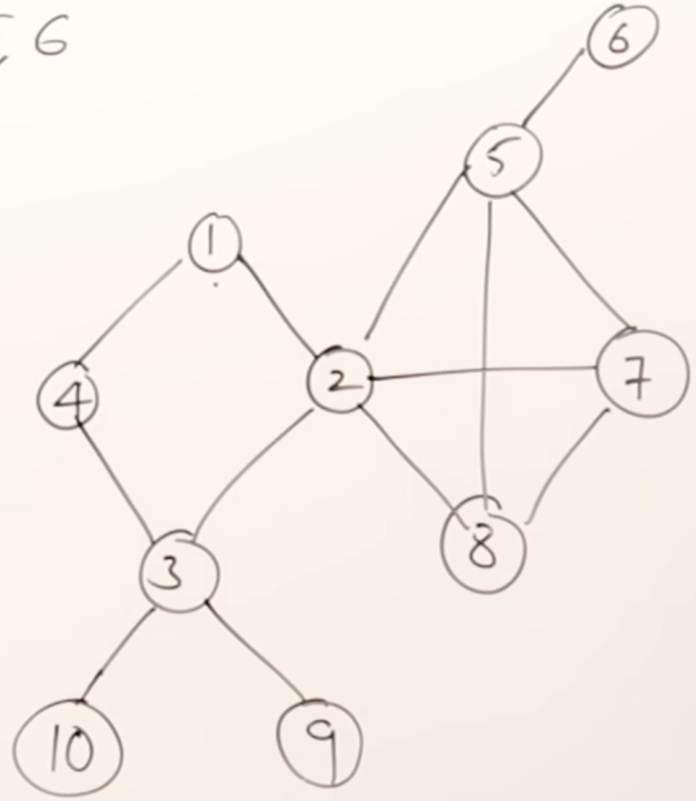


BFS & DFS

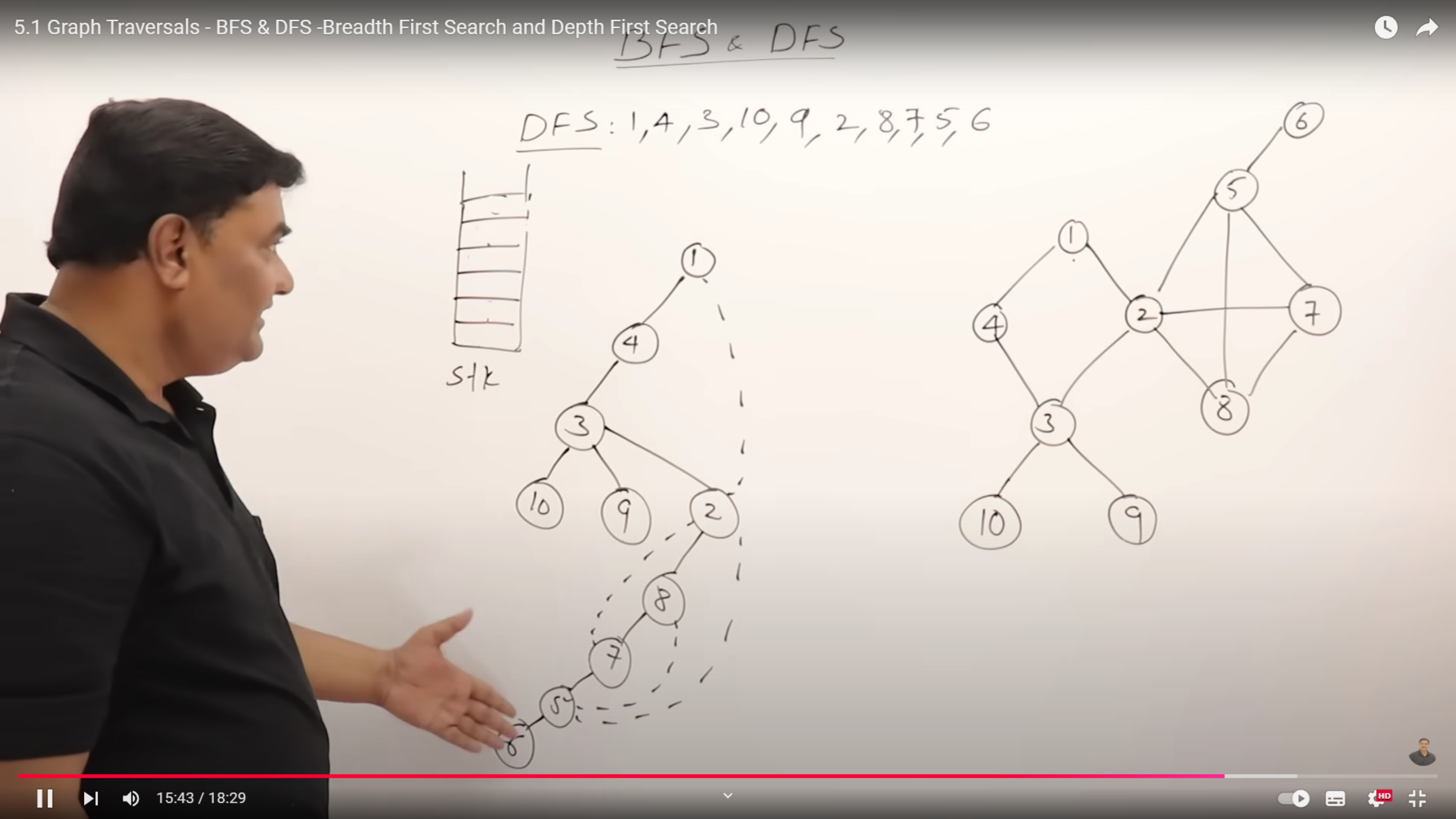
DFS: 1, 4, 3, 10, 9, 2, 8, 7, 5, 6







5.1 Graph Traversals - BFS & DFS -Breadth First Search and Depth First Search



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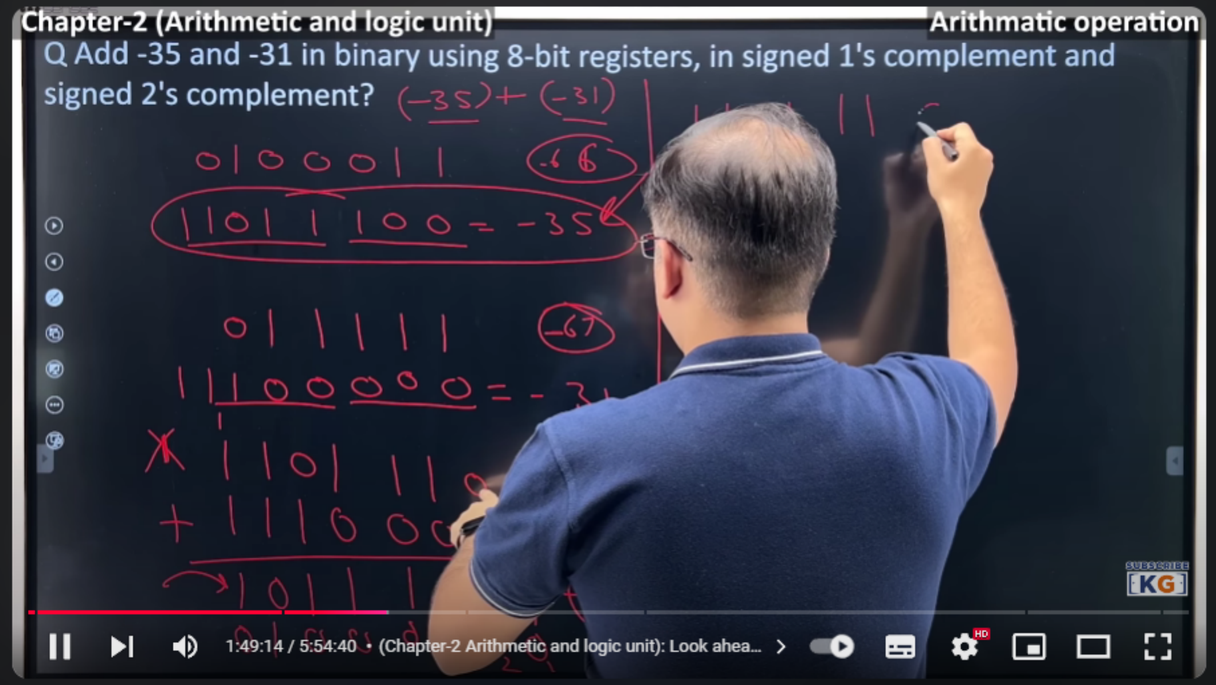

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0	00011	00010	0011	Q0 ← 1

Stop

Q Add -35 and -31 in binary using 8-bit registers, in signed 1's complement and signed 2's complement?

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Floating point representation

- Problem with representation we have already studied is that it do not works well if the number to be stored is either too small or too large, is it take very large amount of memory.
- Imagine a number $6.023 * 10^{23}$ will require around 70 bits to be stored.
- So in scientific application or statics it is a problem to store very small or very large number.

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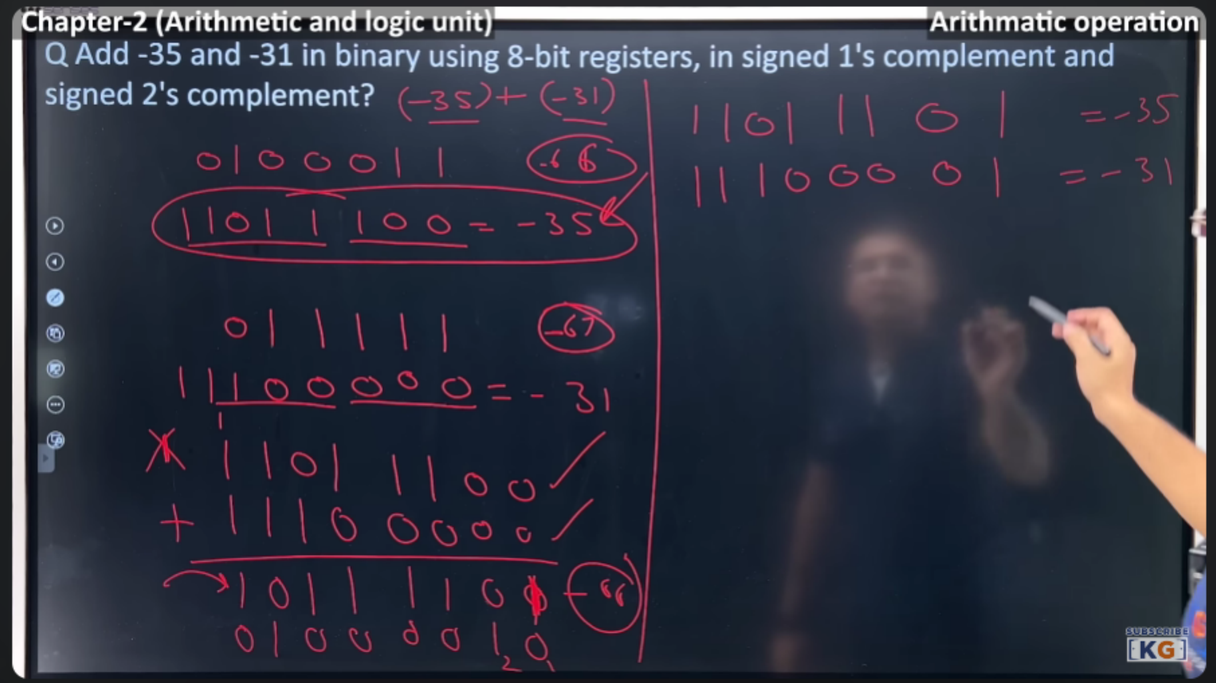

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0	00011	00010	0011	Q0 ← 1

Stop

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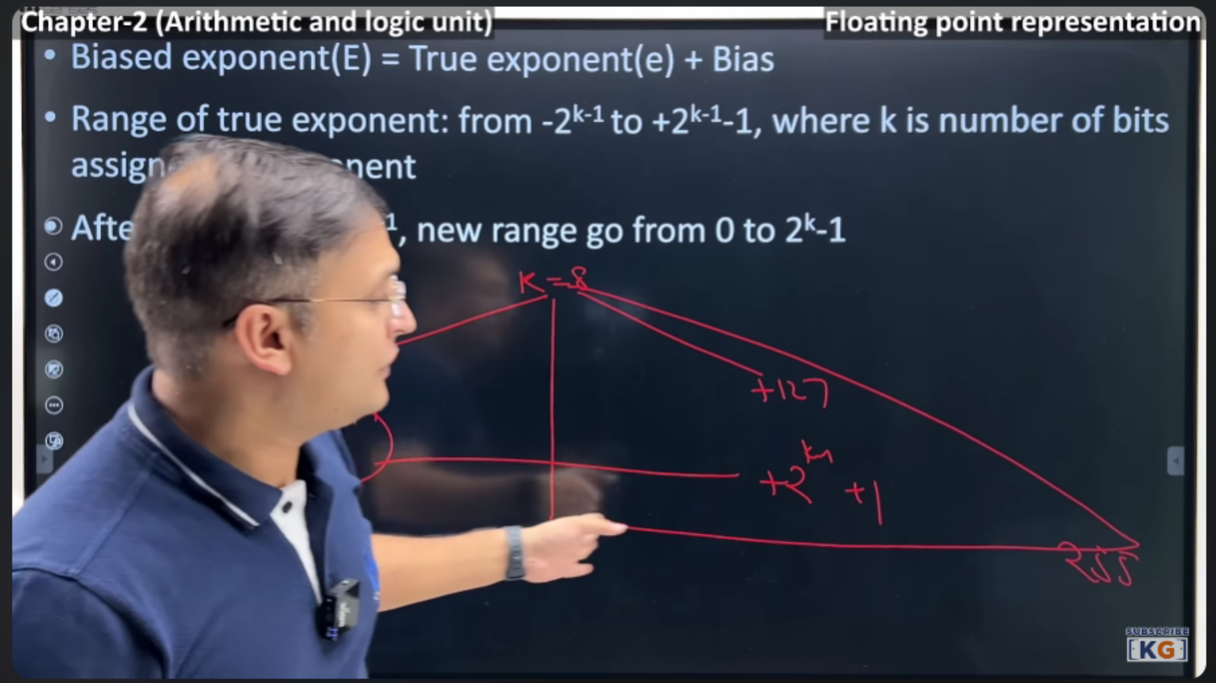

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Q Represent -21.75 (s=1, k=7, m=8)

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IEEE 754 floating point standard

- The **IEEE Standard for Floating-Point Arithmetic (IEEE 754)** is a technical standard for floating-point arithmetic established in 1985 by the Institute of Electrical and Electronics Engineers (IEEE).
- The standard addressed many problems found in the diverse floating-point implementations that mad

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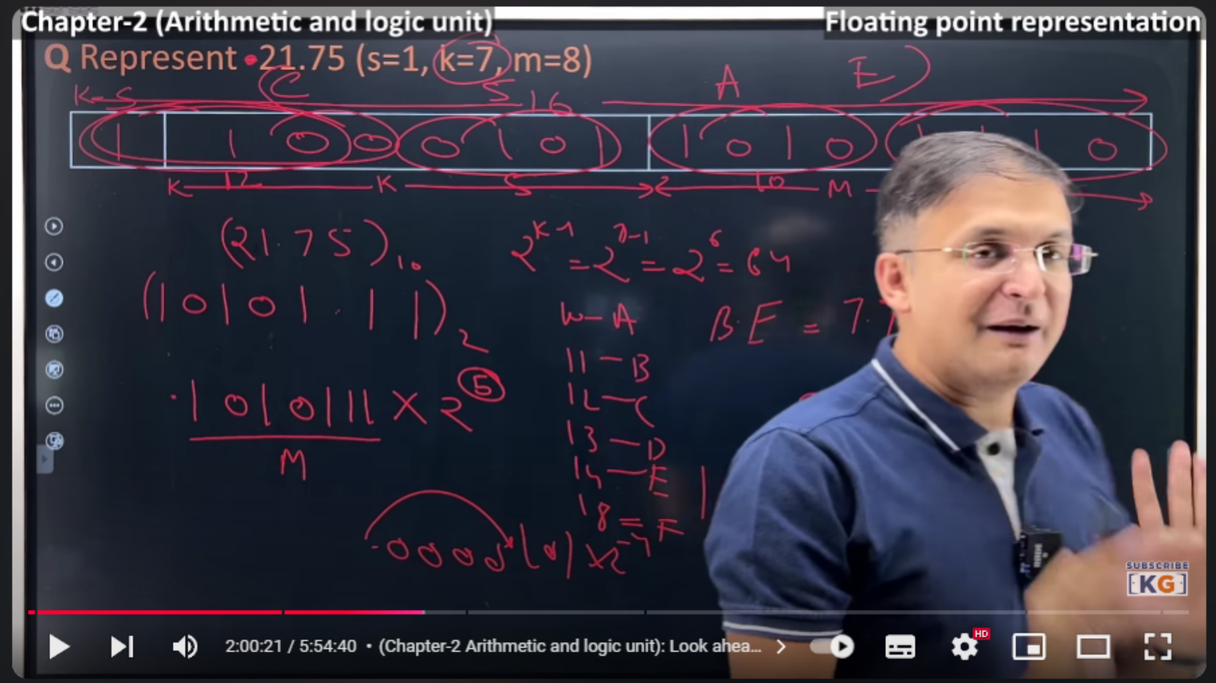

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IEEE 754 floating point standard

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- The standard addressed many problems found in the diverse floating-point implementations that made them difficult to use reliably and portably. Many hardware floating-point units use the IEEE 754 standard.

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IEEE 754 floating point standard

- IEEE 754 standard represent floating point number standards
- It gives a provision for +-0 & +-∞ (by reserving certain pattern for Mantissa/Exponent pattern)

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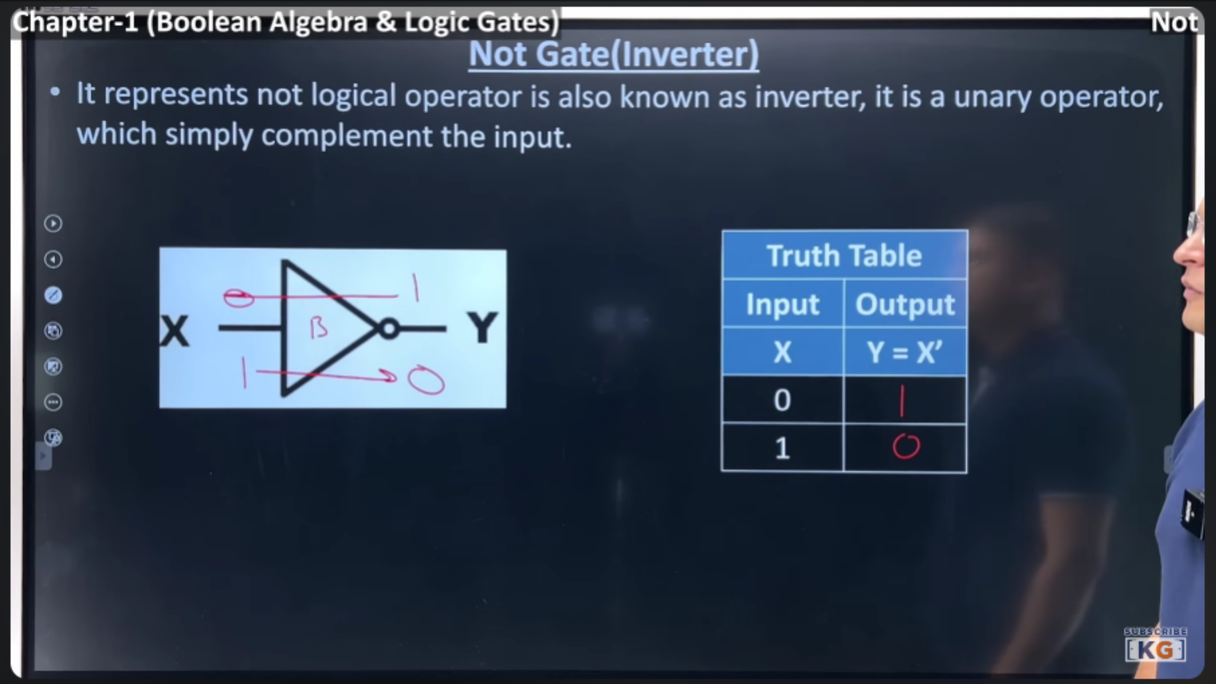

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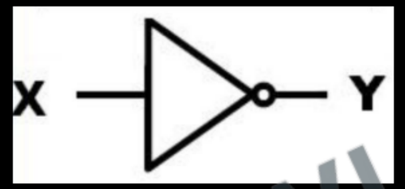
Not Gate(Inverter)

- It represents not logical operator is also known as inverter, it is a unary operator, which simply complement the input.



Truth Table	
Input	Output
X	Y = X'
0	
1	

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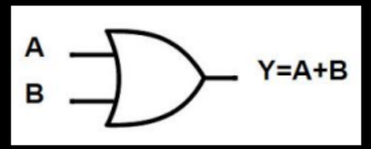
OR Gate

- It is a digital logic gate, that implements logical disjunction. The output will be high if at least one of the input lines is high.



Truth Table		
Input		Output
A	B	Y = A + B
0	0	
0	1	

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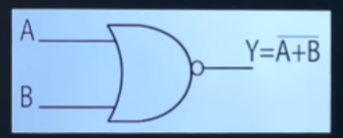
Chapter-1 (Boolean Algebra & Logic Gates) NOR

Nor gate

- The output will be high if and only if all inputs are low. Or simply a OR gate followed by an invertor.
- NOR gate is also called universal gate because it can be used to implement any other logic gate.



Truth Table		
Input		Output
A	B	Y = (A + B)'
0	0	
0	1	
1	0	
1	1	

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Nor gate

- The output will be high if and only if all inputs are low. Or simply a OR gate followed by an invertor.
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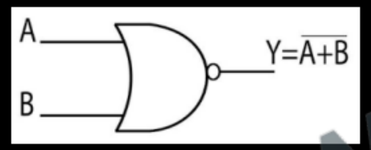

Truth Table		
Input		Output
A	B	Y = (A + B)'
0	0	
0	1	
1	0	
1	1	

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NAND Gate

- The output will be low if and only if all inputs are high. Or simply an and gate followed by an invertor
- NAND gate is also called universal gate.

Truth Table		
Input		Output
A	B	Y = (A . B)'

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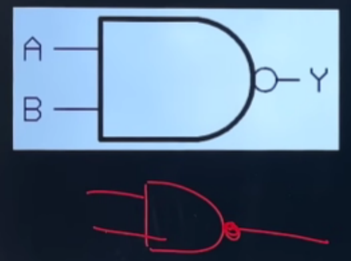
Chapter-1 (Boolean Algebra & Logic Gates) NAND

NAND Gate

- The output will be low if and only if all inputs are high. Or simply an and gate followed by an invertor
- NAND gate is also called universal gate.



Truth Table		
Input		Output
A	B	Y = (A . B)'
0	0	1
0	1	1
1	0	1
1	1	0

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NAND Gate

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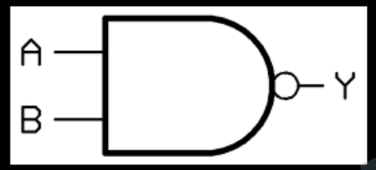

Truth Table		
Input		Output
A	B	Y = (A . B)'
0	0	
0	1	
1	0	
1	1	

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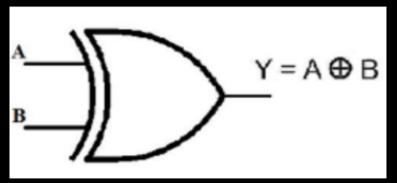
EX-OR

- For two inputs, output will be high if and only if both the input values are different.
- $a \oplus b = a'.b + a.b'$



Truth Table		
Input		Output
A	B	Y = A ⊕ B
0	0	
0	1	

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Chapter-1 (Boolean Algebra & Logic Gates) NAND

NAND Gate

- The output will be low if and only if all inputs are high. Or simply an and gate followed by an invertor
- NAND gate is also called universal gate.

Truth Table		
Input		Output
A	B	Y = (A . B)'
0	0	1
0	1	1
1	0	1
1	1	0

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- The output will be low if and only if all inputs are high. Or simply an and gate followed by an invertor
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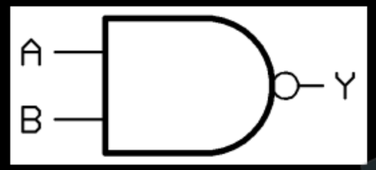

Truth Table		
Input		Output
A	B	Y = (A . B)'
0	0	
0	1	
1	0	
1	1	

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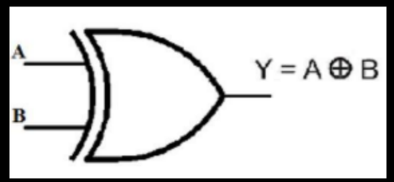
EX-OR

- For two inputs, output will be high if and only if both the input values are different.
- $a \oplus b = a'.b + a.b'$



Truth Table		
Input		Output
A	B	Y = A ⊕ B
0	0	
0	1	

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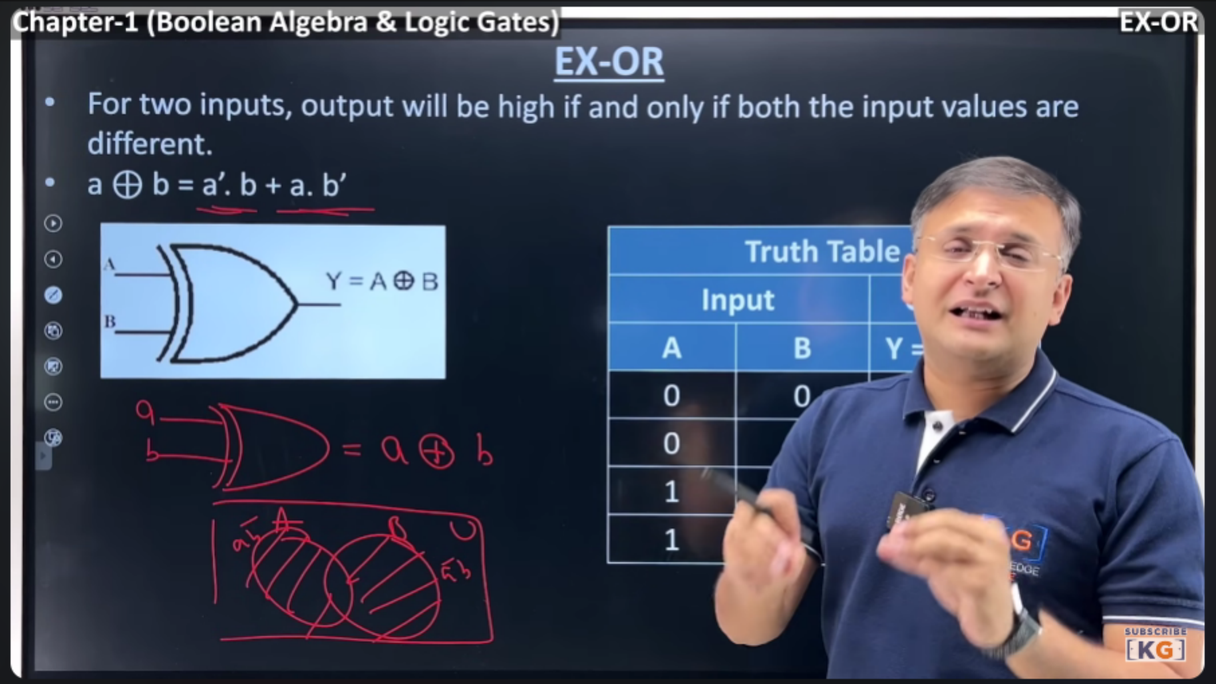

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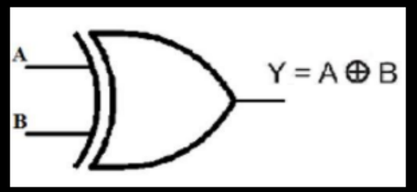
EX-OR

- For two inputs, output will be high if and only if both the input values are different.
- a ⊕ b = a'. b + a. b'



Truth Table		
Input		Output
A	B	Y = A ⊕ B
0	0	
0	1	
1	0	
1	1	

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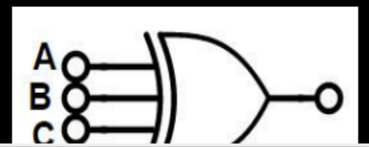
EX-OR

- The XOR gate is a digital logic gate that gives High as output when the number of inputs High are odd.



A	B	C	a ⊕ b ⊕ c
0	0	0	
0	0	1	

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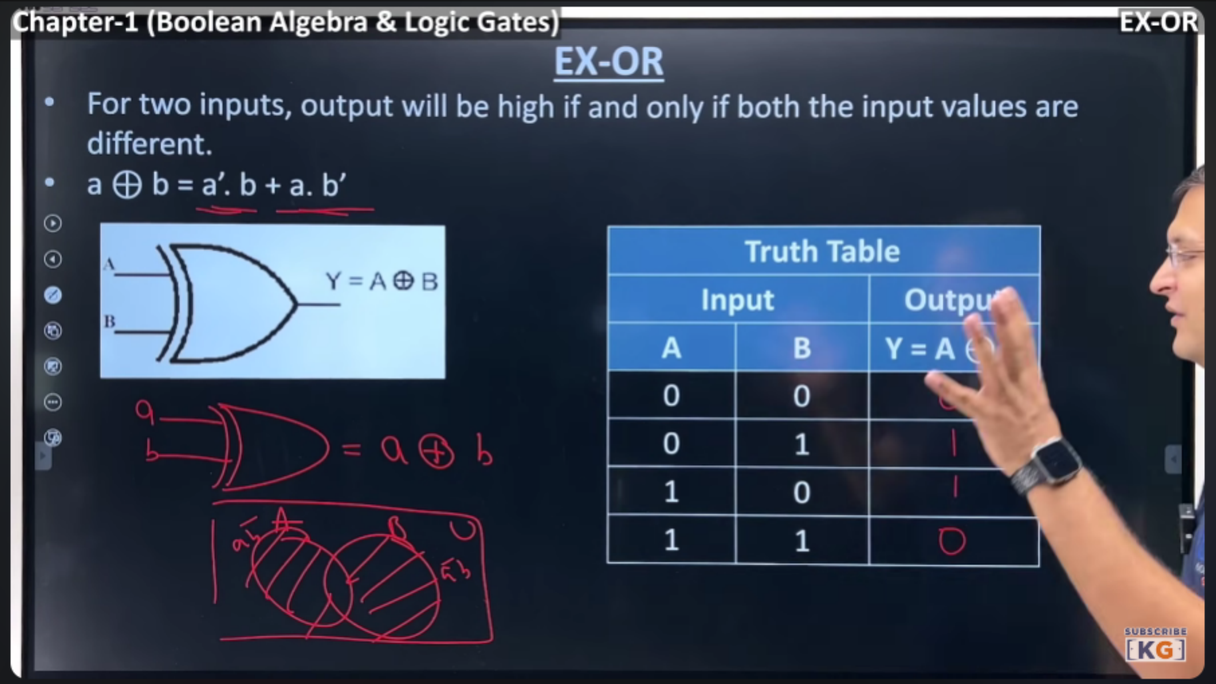

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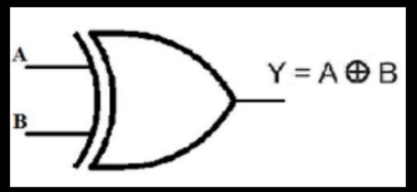

Truth Table		
Input		Output
A	B	Y = A ⊕ B
0	0	
0	1	
1	0	
1	1	

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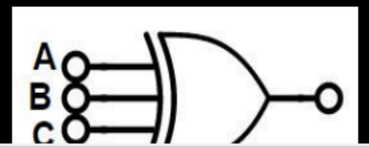
EX-OR

- The XOR gate is a digital logic gate that gives High as output when the number of inputs High are odd.



A	B	C	a ⊕ b ⊕ c
0	0	0	
0	0	1	

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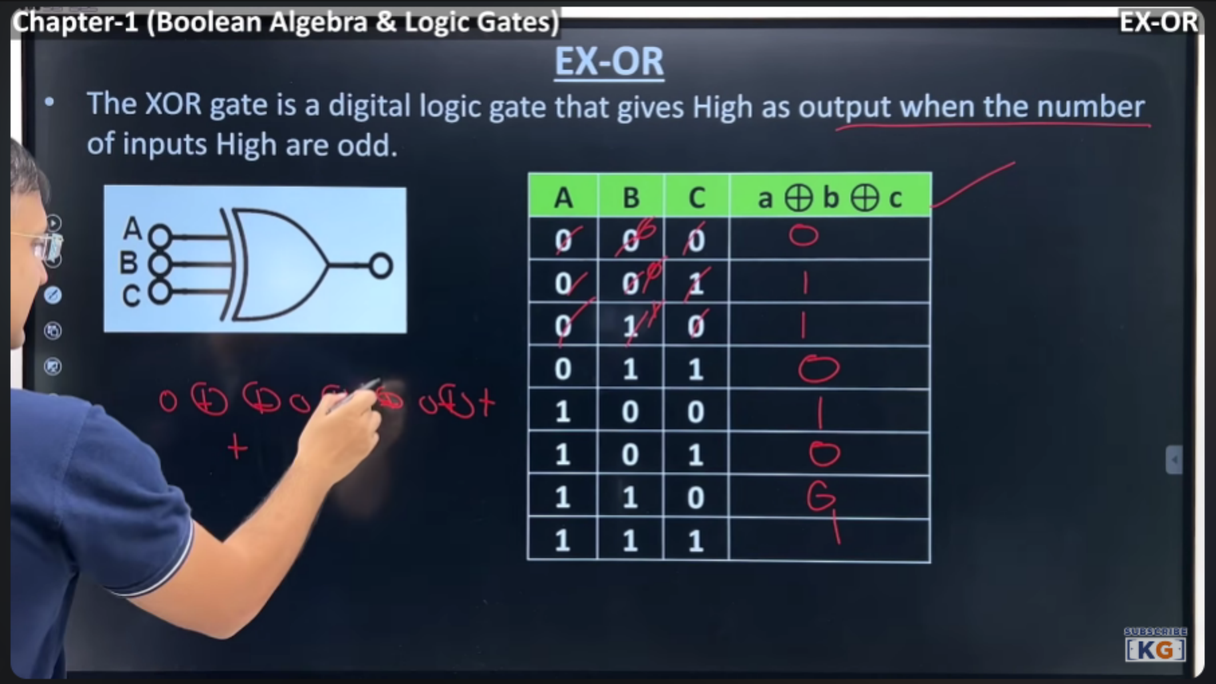

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EX-OR

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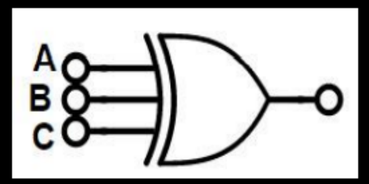

A	B	C	a ⊕ b ⊕ c
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

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EX-NOR

- For two input, output will be high if and only if both the input values are same
- $a \odot b = a'.b' + a.b$

Truth Table

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Chapter-1 (Boolean Algebra & Logic Gates) EX-NOR

EX-NOR

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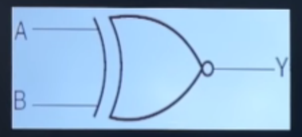

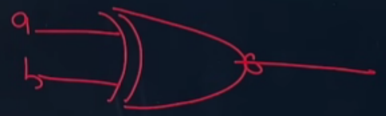

Truth Table		
Input		Output
A	B	Y = A ⊙ B
0	0	0
0	1	0
1	0	0
1	1	1

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EX-NOR

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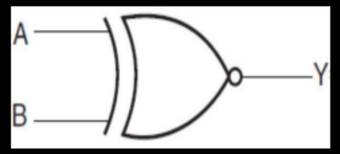
- a ⊙ b = a'. b' + a. b



Truth Table		
Input		Output
A	B	Y = A ⊙ B
0	0	
0	1	
1	0	
1	1	

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EX-NOR

- The EX-NOR gate is a digital logic gate that gives output High when the numbe inputs low are even.

A	B	C	a ⊙ b ⊙ c

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Chapter-1 (Boolean Algebra & Logic Gates) EX-NOR

EX-NOR

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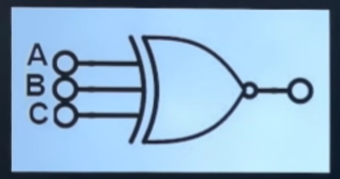

A	B	C	a ⊙ b ⊙ c
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

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EX-NOR

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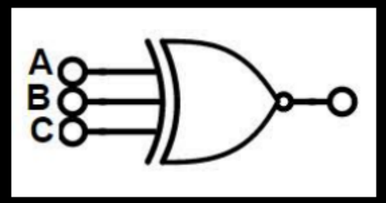

A	B	C	a ⊙ b ⊙ c
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

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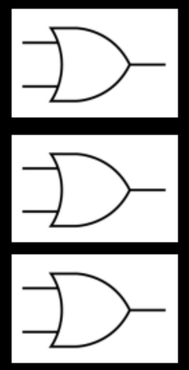

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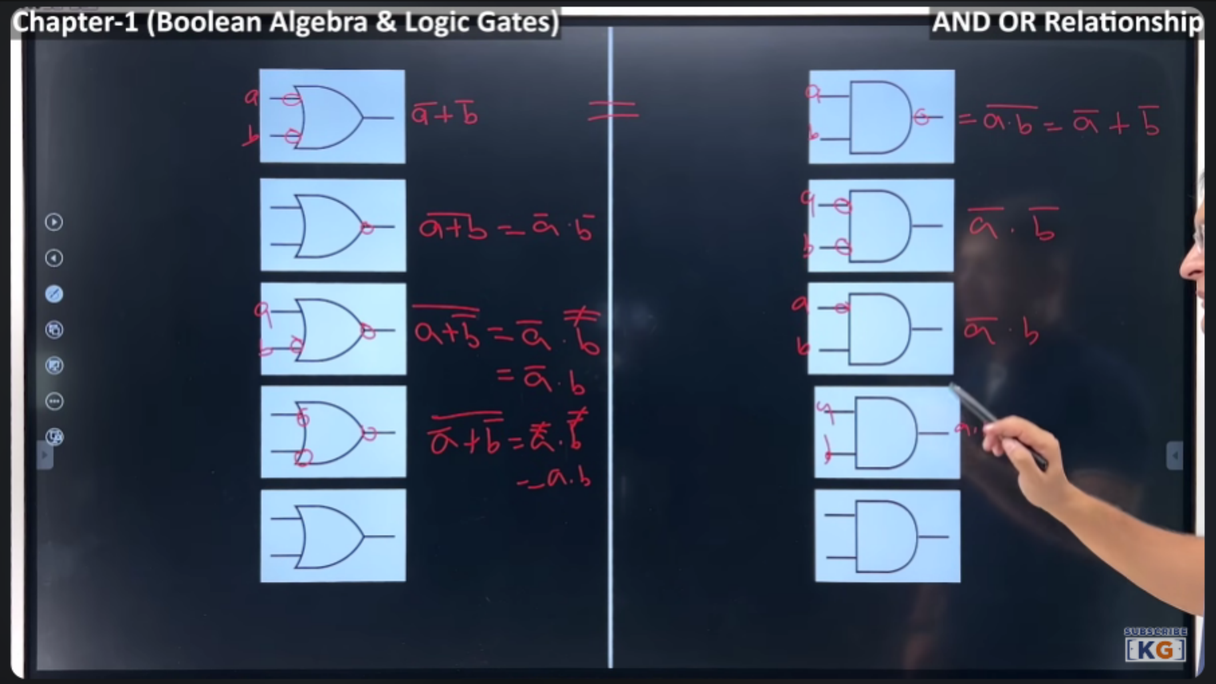

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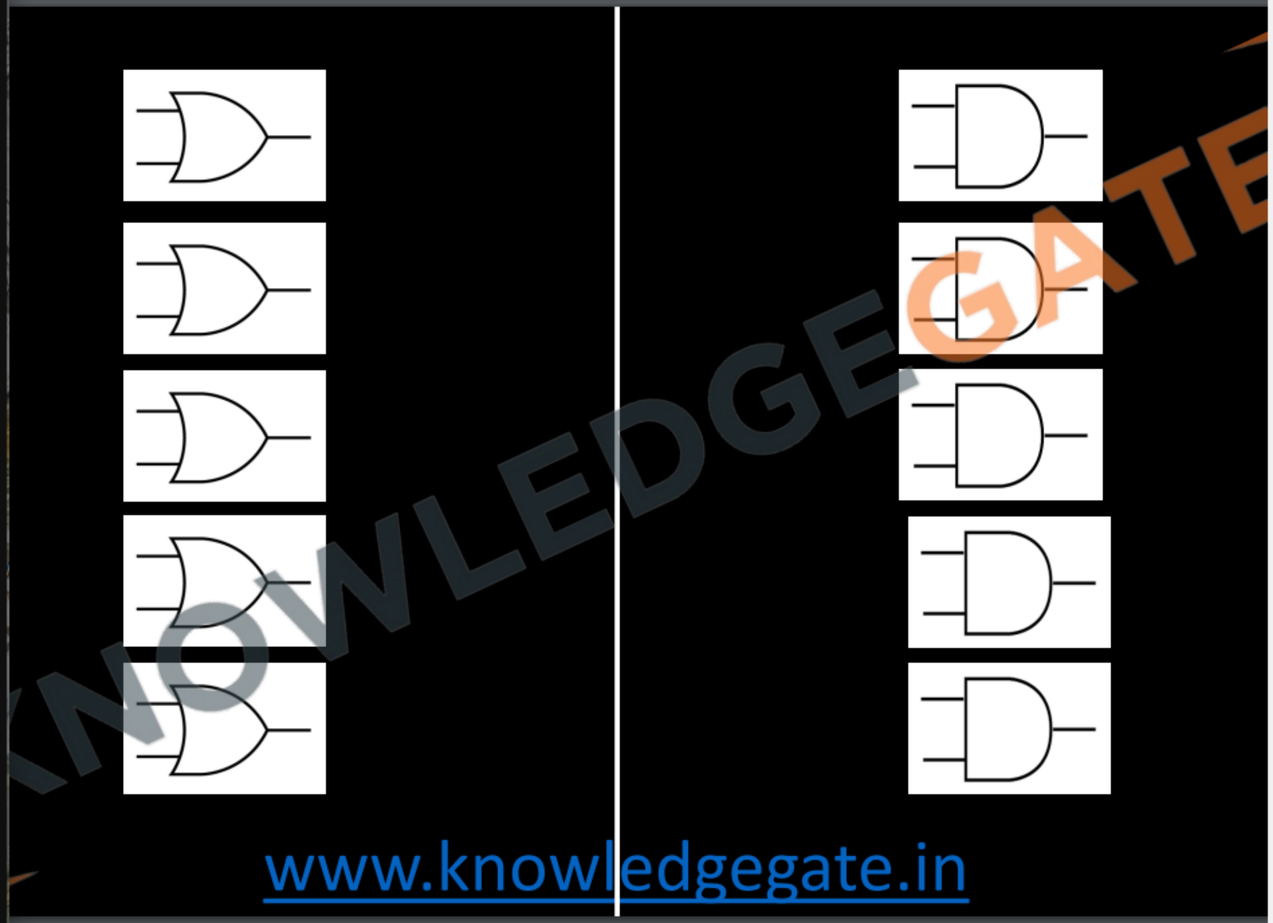

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AND-OR(NAND-NAND) Implementation

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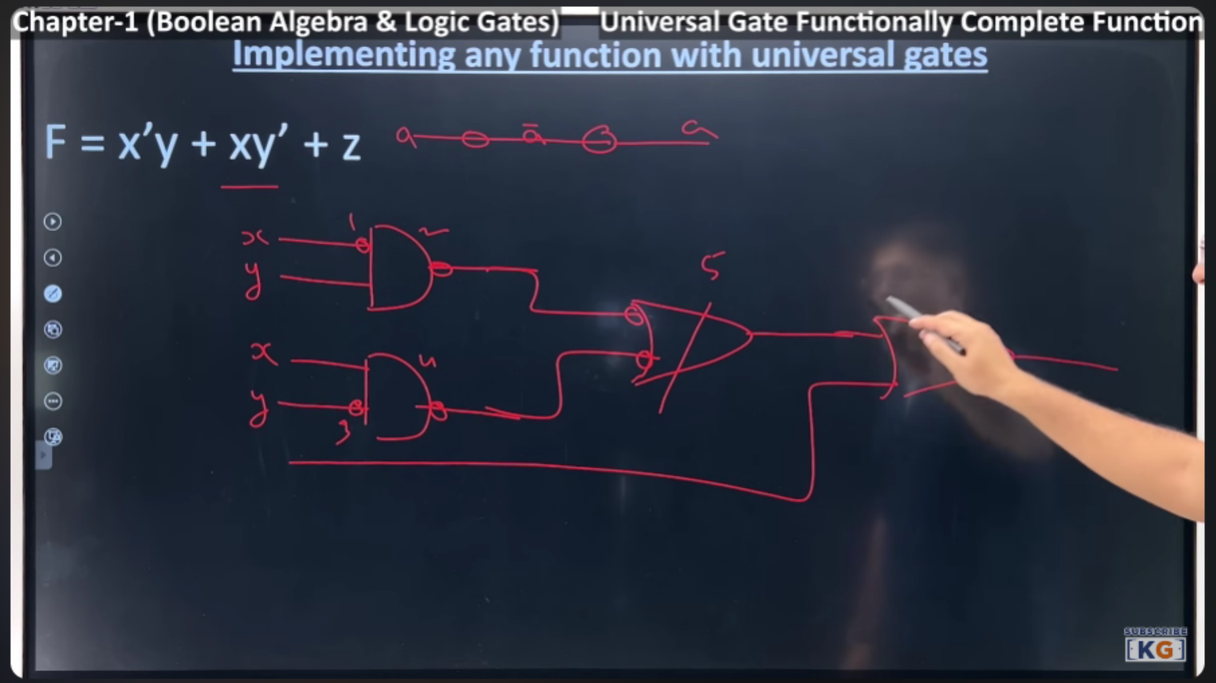

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Implementing any function with universal gates

$F = x'y + xy' + z$

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$F = bd + bc + acd'$

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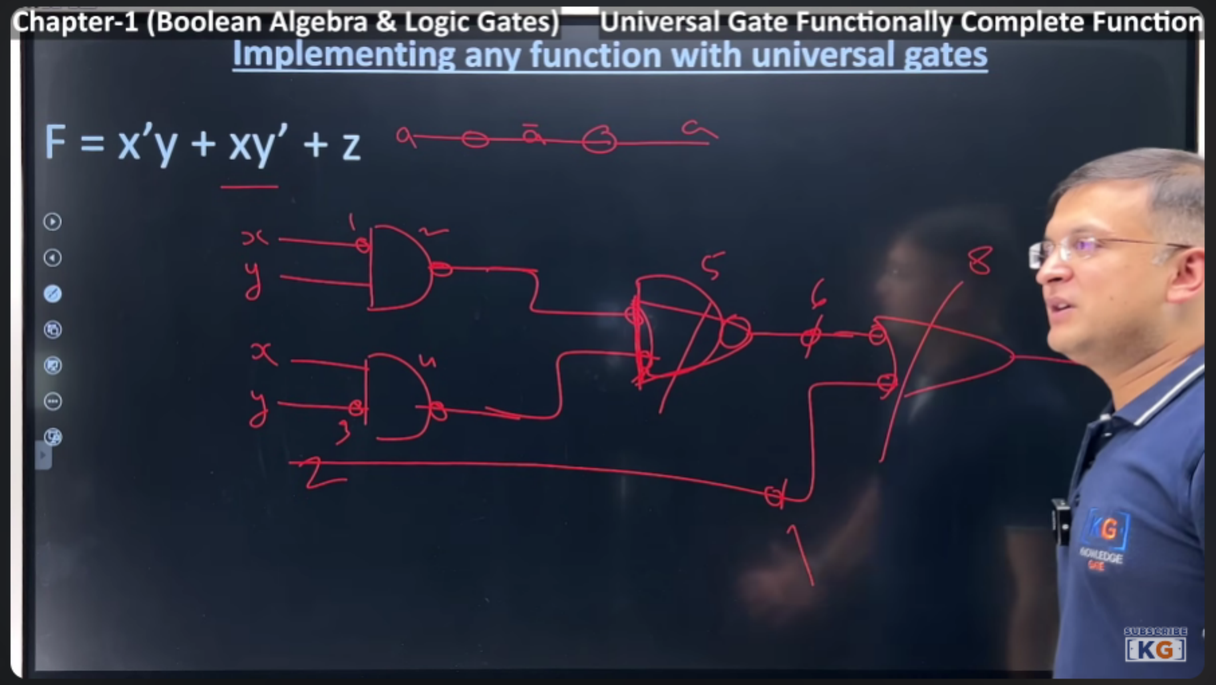

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Implementing any function with universal gates

$F = x'y + xy' + z$

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$F = bd + bc + acd'$

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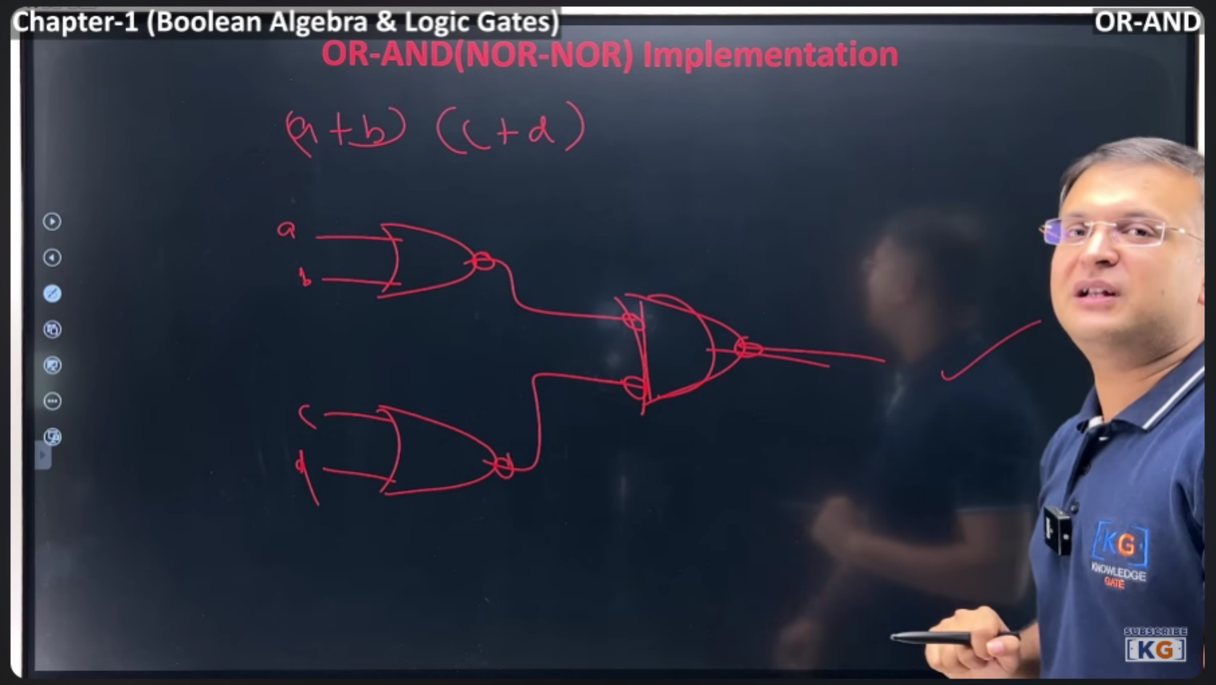

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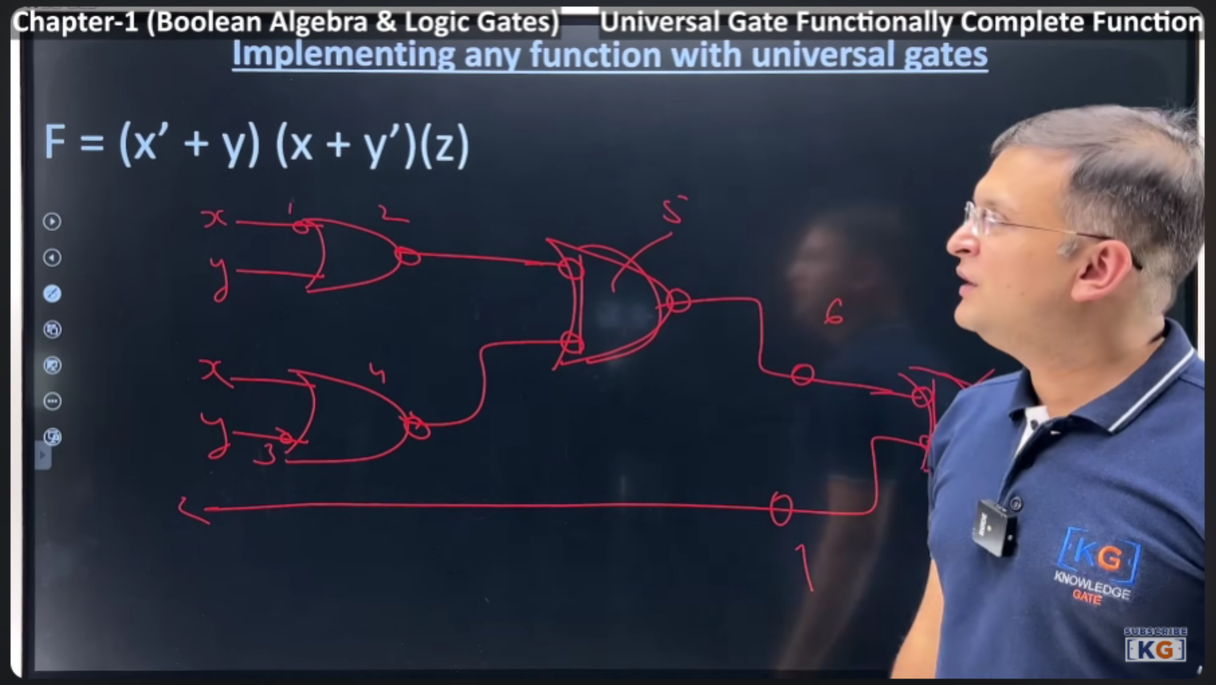

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Implementing any function with universal gates

$$F = (x' + y)\,(x + y')(z)$$

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Boolean Expressions

- Boolean expressions are the method using which we save the information about the Boo function, that when we get value 1 and when we get value 0 as output.
- So, we convert the truth table of the function into an expression, reading which we can

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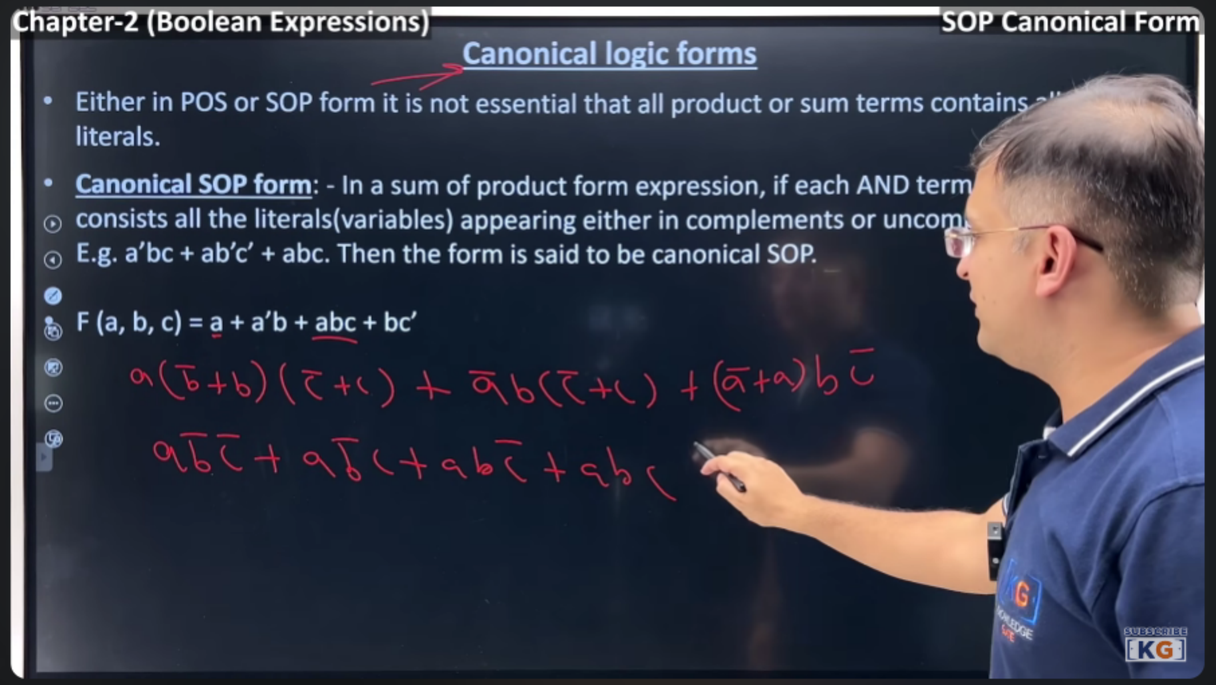

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Canonical logic forms

- Either in POS or SOP form it is not essential that all product or sum terms contains all the literals.
- **Canonical SOP form**: - In a sum of product form expression, if each AND term (product term) consists all the literals(variables) appearing either in complements or uncomplemented form E.g. a'bc + ab'c' + abc. Then the form is said to be canonical SOP.
- F (a, b, c) = a + a'b + abc + bc'

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POS (Product of Sum)

- A product of sum (POS) form of expression contains OR (sum) terms which are AND (product) together, that's why called product of sum expression.
- Each OR term (sum term) consists of one or more literals(variables) appearing either in complemented or uncomplemented form. (a' + b). (b' + c'). (a + c)
- A OR (sum) term which contains all the literals(variables) either in complemented or uncomplemented form is called maxterm. In a n variable function, there will be 2^n maxterms.

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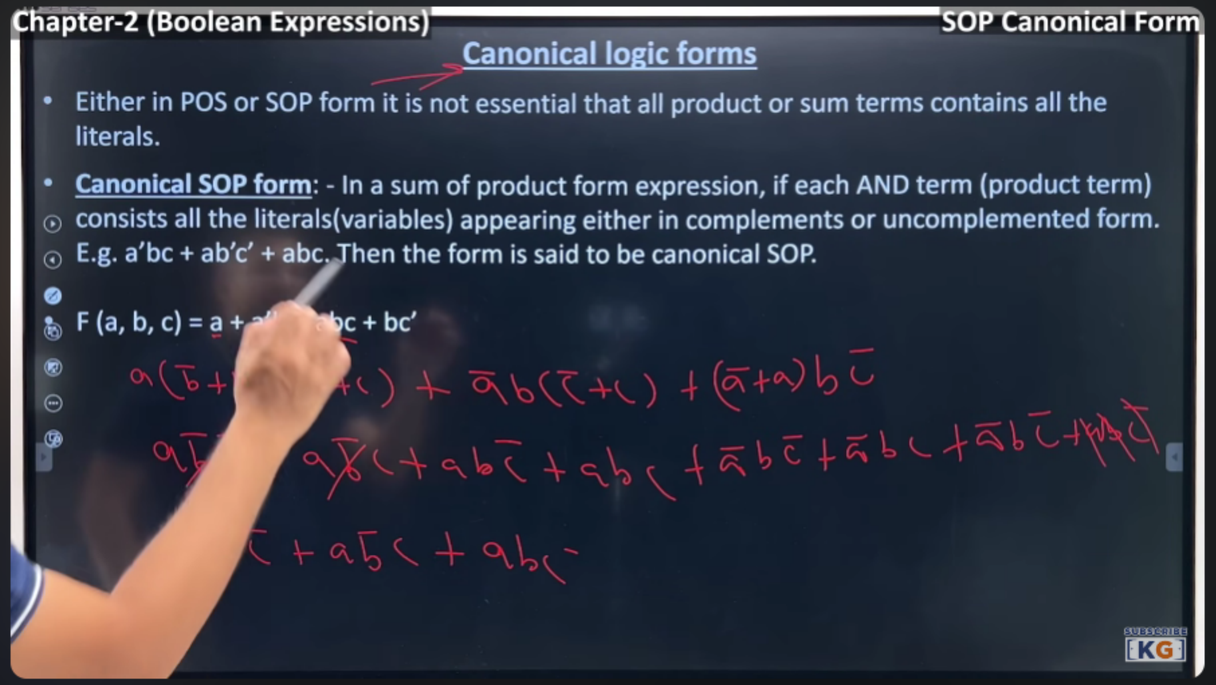

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Chapter-2 (Boolean Expressions) No of Functions Possible

No of functions possible

Q With n-Boolean variables how many different Boolean functions are possible?

With n binary variable we can generate 2^n combinations. And as we know that a Boolean function can also have only 2 possible values either 0 or 1, so total number of different functions possible will be $2^{(2^n)}$.

Similarly, we can generalize this idea as $x^{(y^z)}$ are the total number of functions possible, x is the nature of the function, y is the nature of the variable and z is the number of variables.

A	B	f_0	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8	f_9	f_{10}	f_{11}	f_{12}	f_{13}	f_{14}	f_{15}
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

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No of functions possible

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A	B	f_0	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8	f_9	f_{10}	f_{11}	f_{12}	f_{13}	f_{14}	f_{15}
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

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Complementation

- Let us consider a function f(a, b, c, d,....., 0, 1, +, ·), then the complement of the function is defined as f'(a', b', c',....., z', 1, 0, ·, +).

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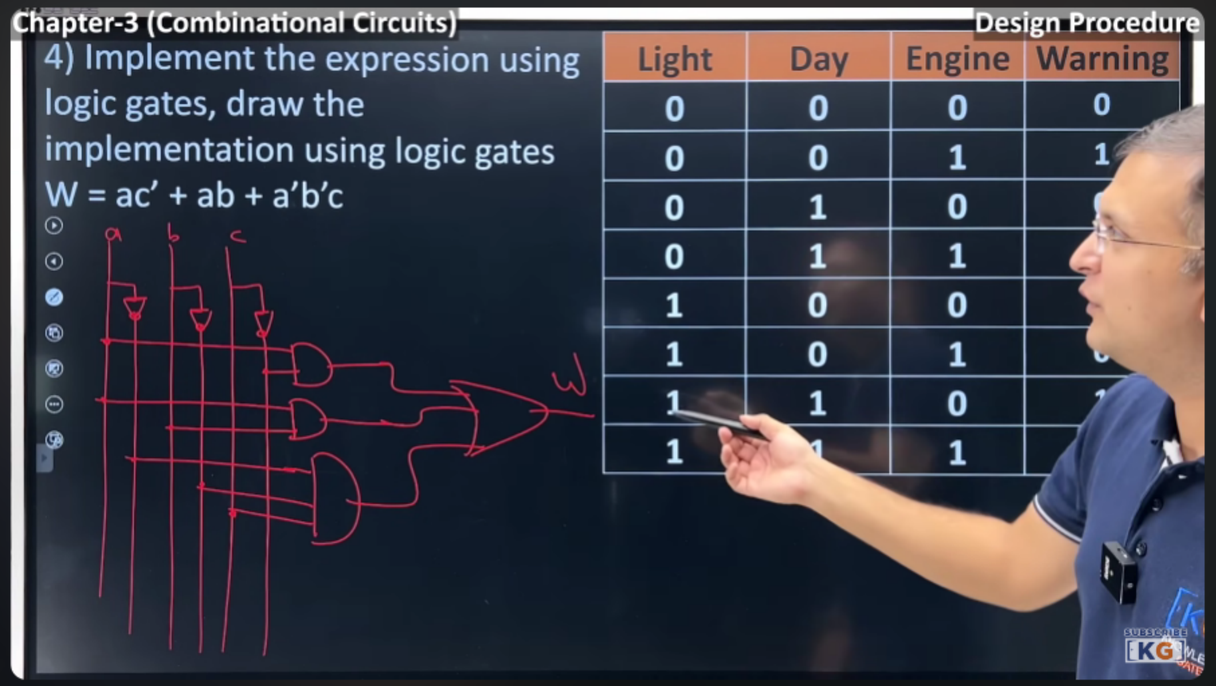

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c'	0	0	2	6	4
c	1	1	3	7	5

W =

1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

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4) Implement the expression using logic gates, draw the implementation using logic gates
W = ac' + ab + a'b'c

Light	Day	Engine	Warnin
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

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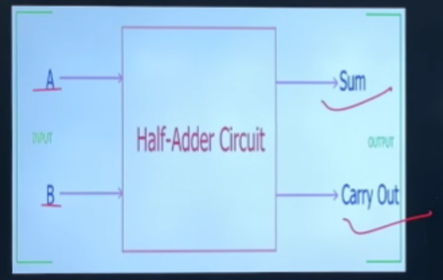
Chapter-3 (Combinational Circuits) Half Adder

- It is a combinational circuit, which perform the arithmetic addition of two one-bit binary numbers is referred to as an half-adder.
- So, in half adder inputs are adds two single binary bits *A* and *B*, and two outputs, sum (*S*) and carry (C).



INPUTS		OUTPUTS	
A	B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

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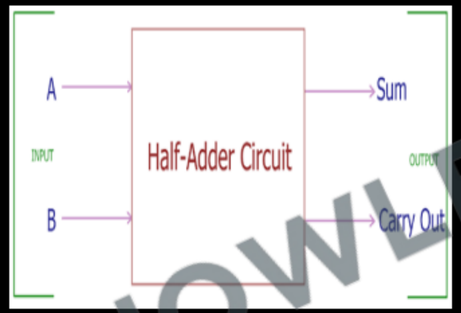
It is a combinational circuit, which perform the arithmetic addition of two one-bit binary numbers is referred to as an half-adder.

So, in half adder inputs are adds two single binary bits *A* and *B*, and two outputs, sum (*S*) and carry (C).



INPUTS		OUTPUTS	
A	B	Carry	Sum
0	0		
0	1		
1	0		
1	1		

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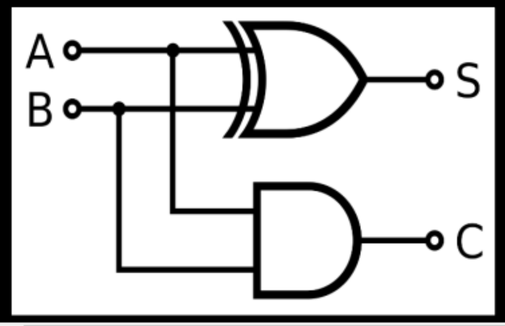

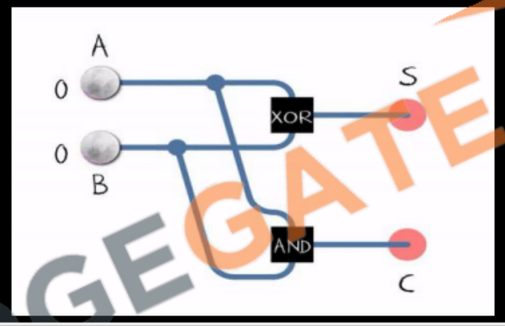

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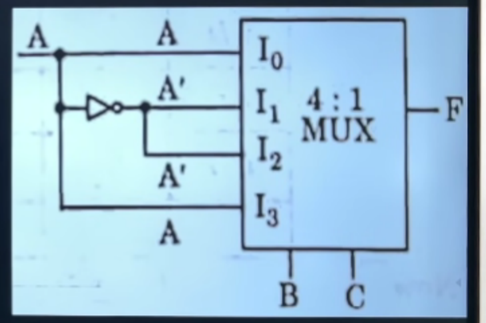
Chapter-3 (Combinational Circuits) Multiplexer

Q Implement the function F(a,b,c) = a'b'c + a'bc' + ab'c' + abc. With b and c variable on select line?

	I_0	I_1	I_2	I_3
A'	0	1	2	3
A	4	5	5	7



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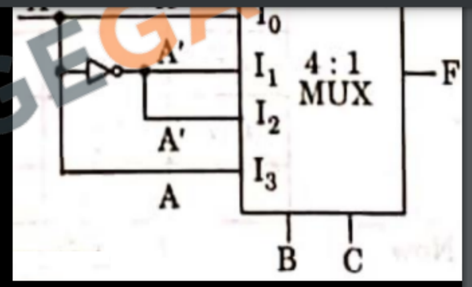
	I_0	I_1	I_2	I_3
A'	0	1	2	3
A	4	5	5	7



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Q Implement the function F(a,b,c) = a'b'c + a'bc' + ab'c' + abc. With one, two and three variable on the select line?

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Demultiplexer

1. A demultiplexer (or DeMux) is a device that takes a single input line and routes it to one of

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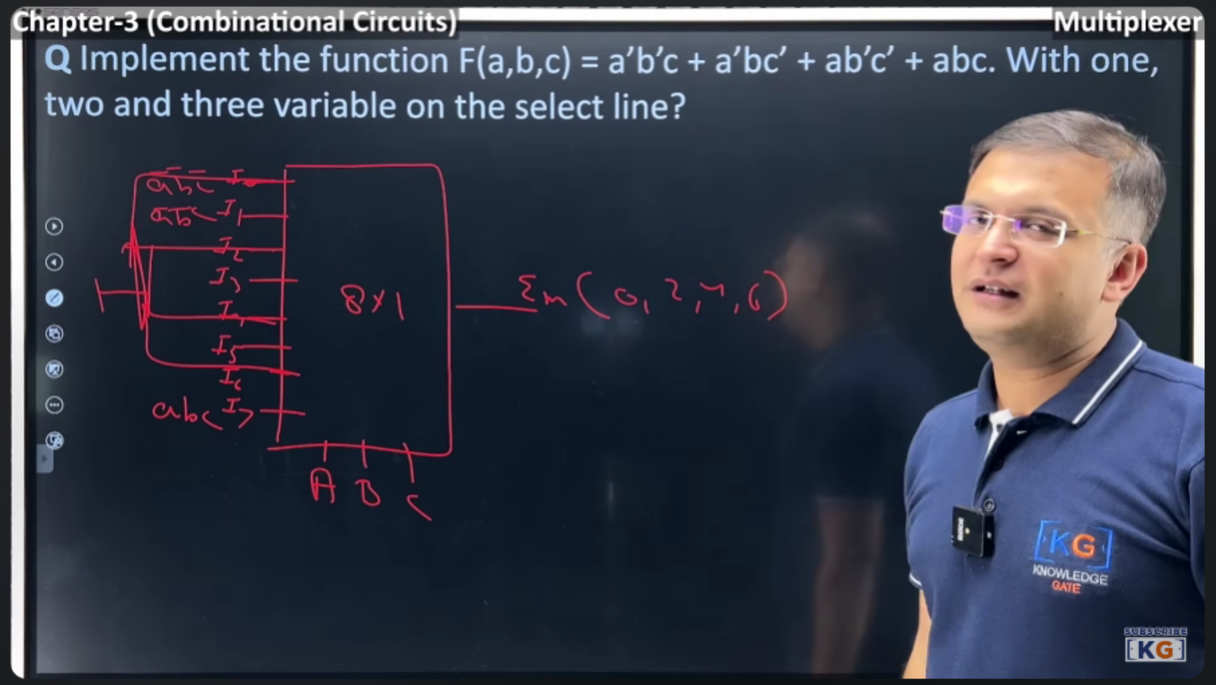

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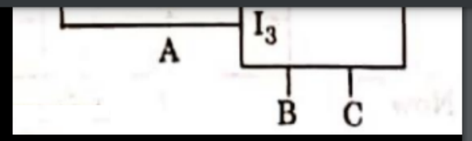

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Q Implement the function F(a,b,c) = a'b'c + a'bc' + ab'c' + abc. With one, two and three variable on the select line?

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Demultiplexer

1. A demultiplexer (or DeMux) is a device that takes a single input line and routes it to one of several digital output lines.
2. A demultiplexer is also called a data distributor.
3. It is conceptually same as Mux just with reverse logic.

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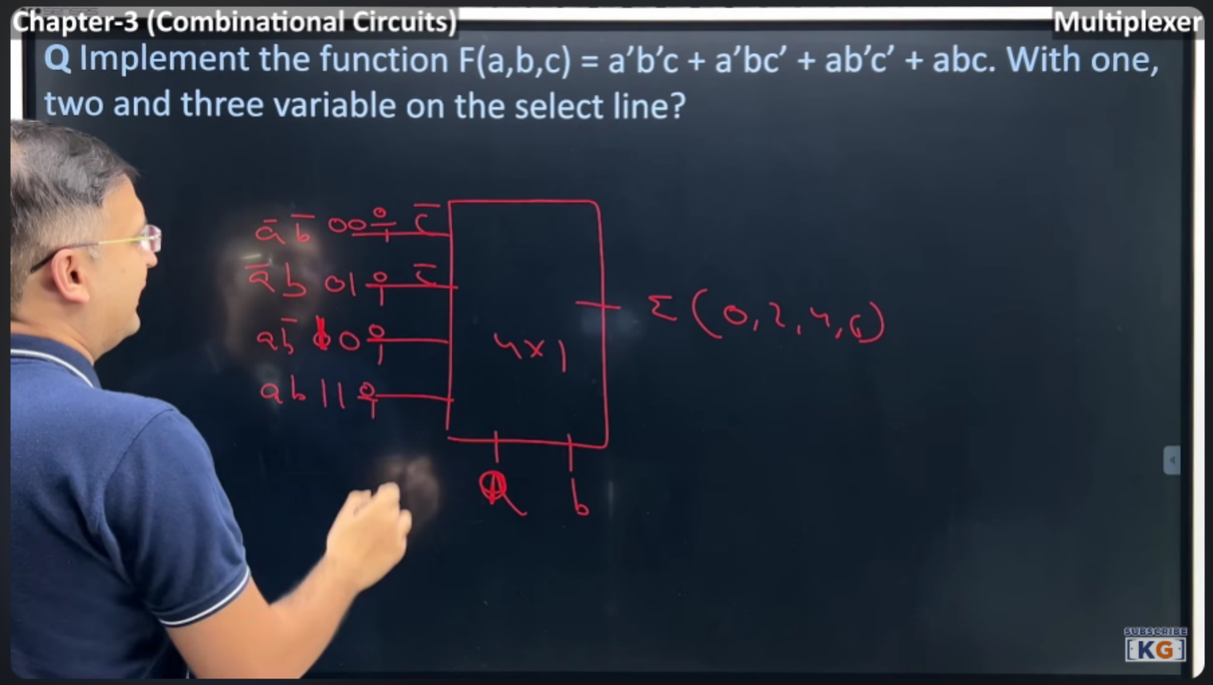

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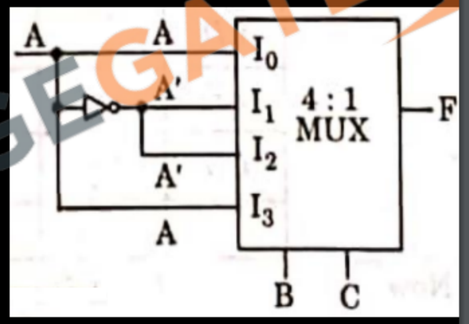
Q Implement the function F(a,b,c) = a'b'c + a'bc' + ab'c' + abc. With b and c variable on select line?

	I_0	I_1	I_2	I_3
A'	0	1	2	3
A	4	5	5	7



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Q Implement the function F(a,b,c) = a'b'c + a'bc' + ab'c' + abc. With one, two and three variable on the select line?

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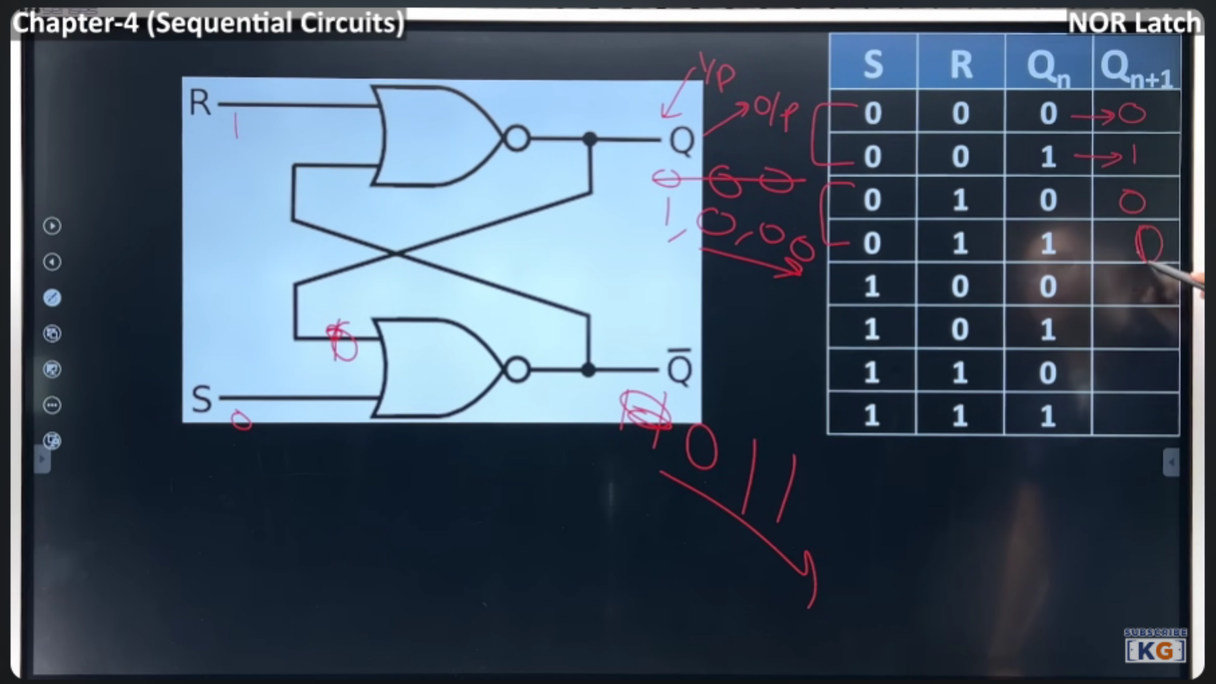

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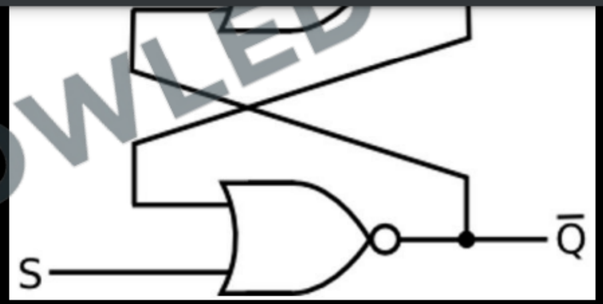

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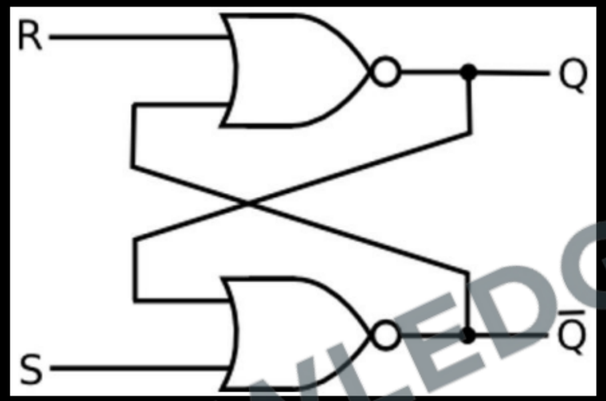

S	R	Q_n	Q_{n+1}
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

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S	R	Q_n	Q_{n+1}

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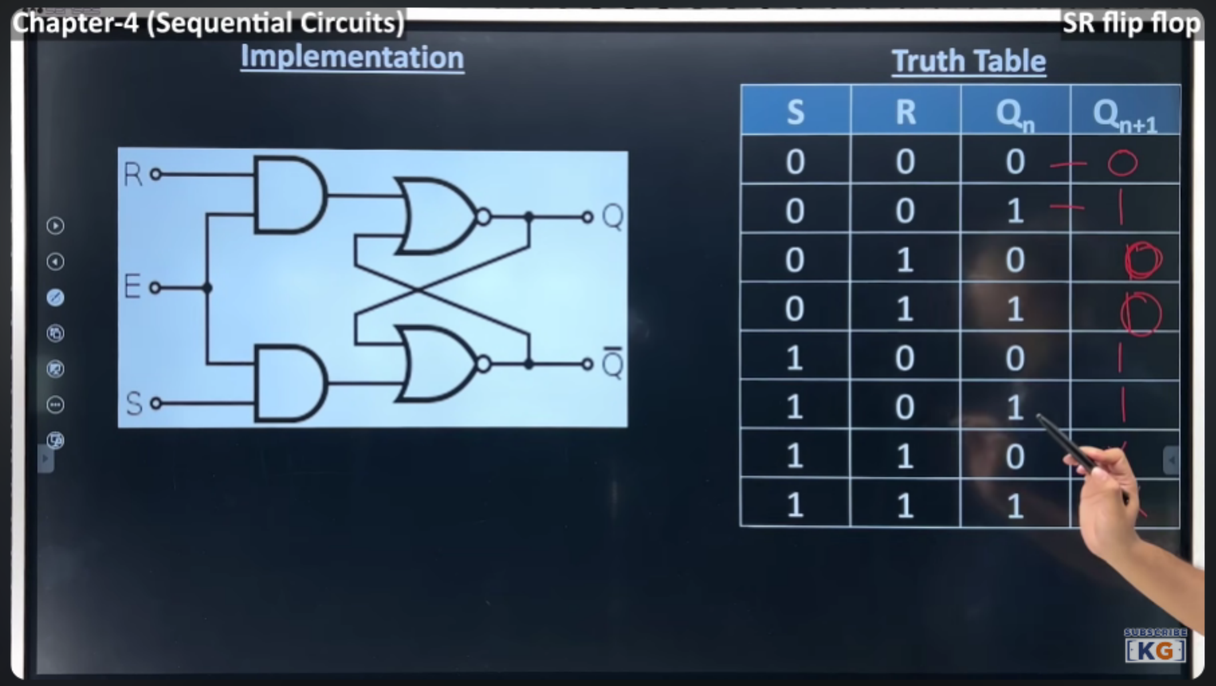

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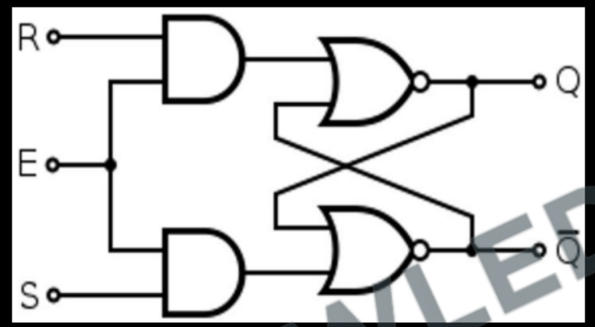

Truth Table

S	R	Q_n	Q_{n+1}
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

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Truth Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0

K-Map

	sr	s'r'	s'r	sr	sr'
q		00	01	11	10
q'	00				

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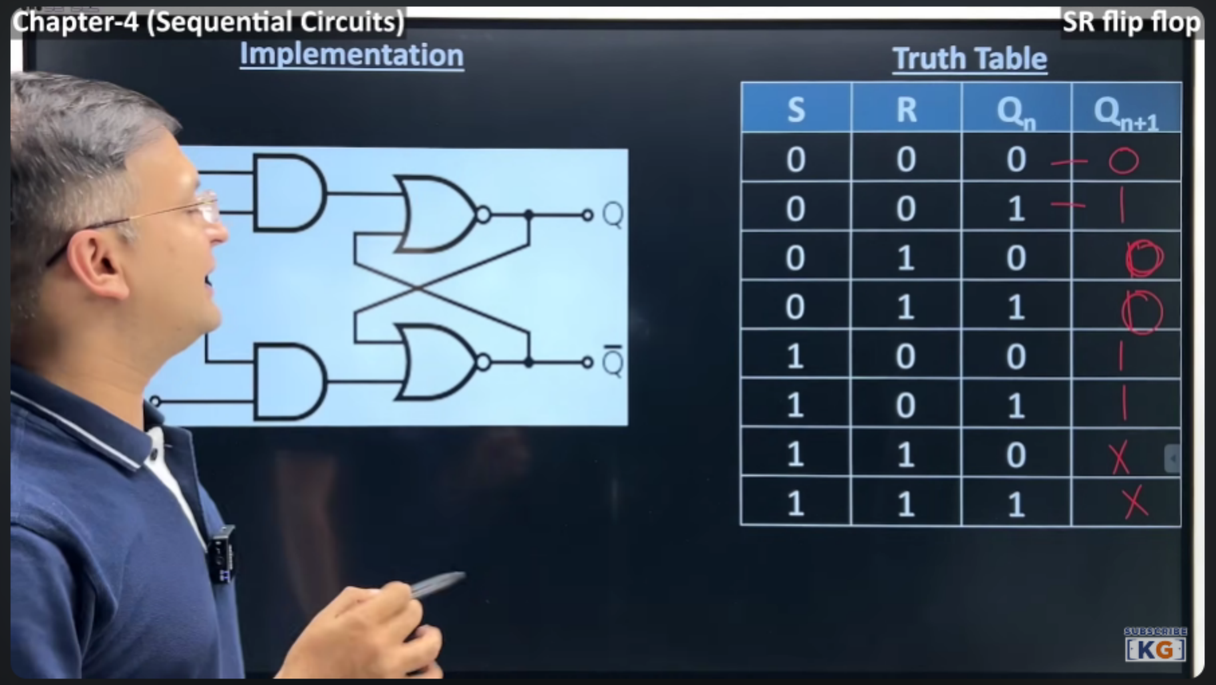

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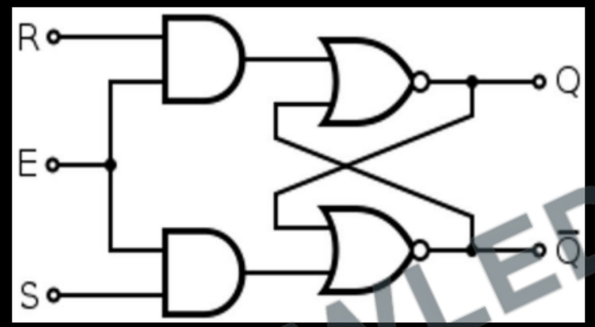

Truth Table

S	R	Q_n	Q_{n+1}
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

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Truth Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0

K-Map

	sr	s'r'	s'r	sr	sr'
q		00	01	11	10
q'	00				

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Chapter-4 (Sequential Circuits)

SR flip flop

Truth Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

K-Map

	sr	s'r'	s'r	sr	sr'
q		00	01	11	10
q'	00				
q	01				

Characteristics Equation

$Q_{n+1} = S + \bar{R} Q_n$

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Truth Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

K-Map

	sr	s'r'	s'r	sr	sr'
q		00	01	11	10
q'	00				
q	01				

Characteristics Equation

$Q_{n+1} =$

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Truth Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1

Characteristics Equation

$Q_{n+1} = S + R' Q_n$

Function Table

S	R	Q_{n+1}
0	0	
0	1	
1	0	
1	1	

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Chapter-4 (Sequential Circuits)

SR flip flop

Truth Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

Characteristics Equation

$$Q_{n+1} = S + R' Q_n$$

Function Table

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

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1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

Characteristics Equation

$Q_{n+1} =$

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Truth Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

Characteristics Equation

$$Q_{n+1} = S + R' Q_n$$

Function Table

S	R	Q_{n+1}
0	0	
0	1	
1	0	
1	1	

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Chapter-4 (Sequential Circuits)

SR flip flop

Truth Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

Characteristics Equation

$$Q_{n+1} = S + R' Q_n$$

Function Table

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

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1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

Characteristics Equation

$Q_{n+1} =$

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Truth Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

Characteristics Equation

$$Q_{n+1} = S + R' Q_n$$

Function Table

S	R	Q_{n+1}
0	0	
0	1	
1	0	
1	1	

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Chapter-4 (Sequential Circuits) SR flip flop

Truth Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

Excitation Table

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

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1	1	1	X

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Truth Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

Excitation Table

Q_n	Q_{n+1}	S	R
0	0		
0	1		
1	0		
1	1		

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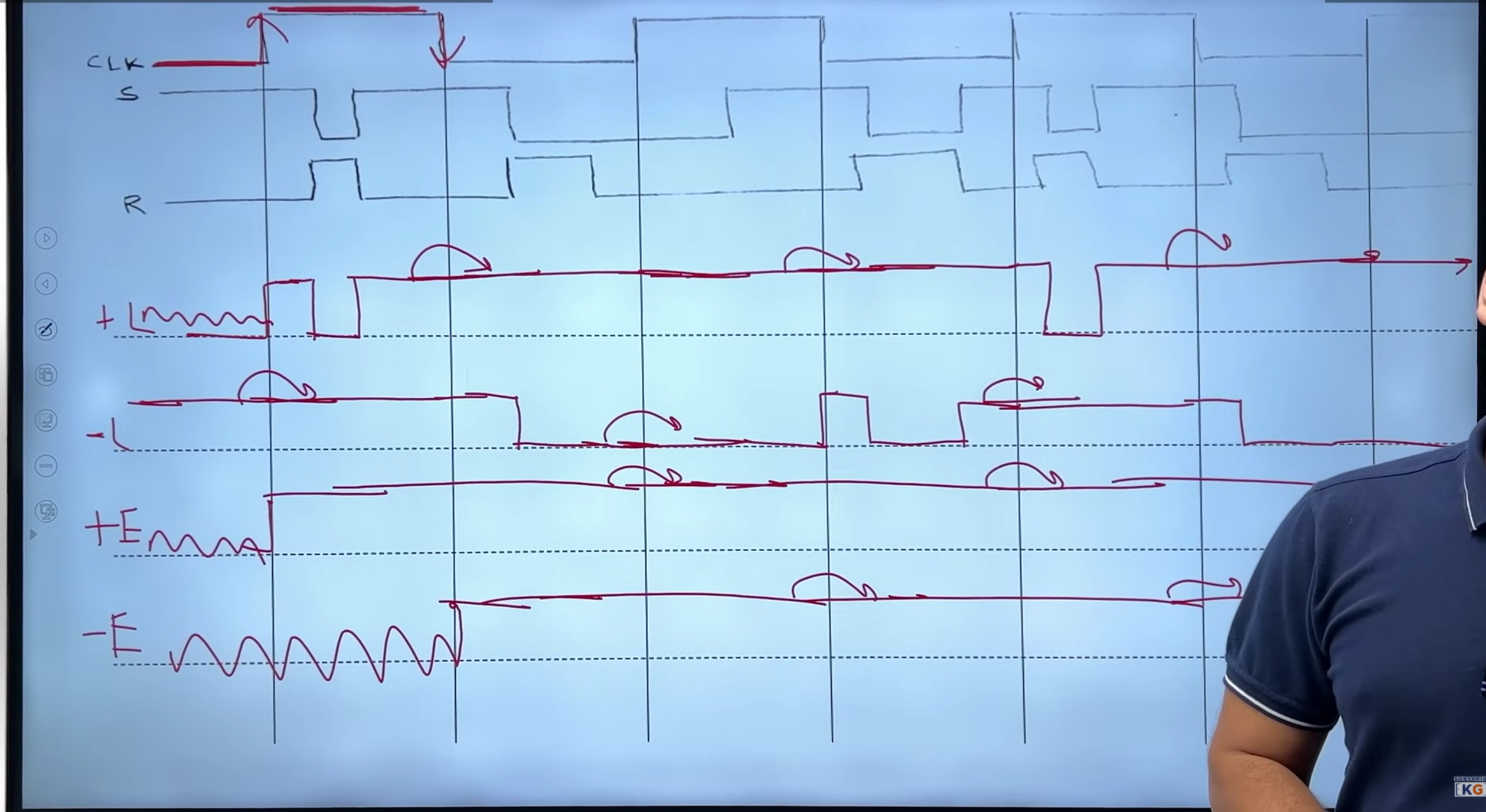
Truth Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1

State Diagram

SR flip flop



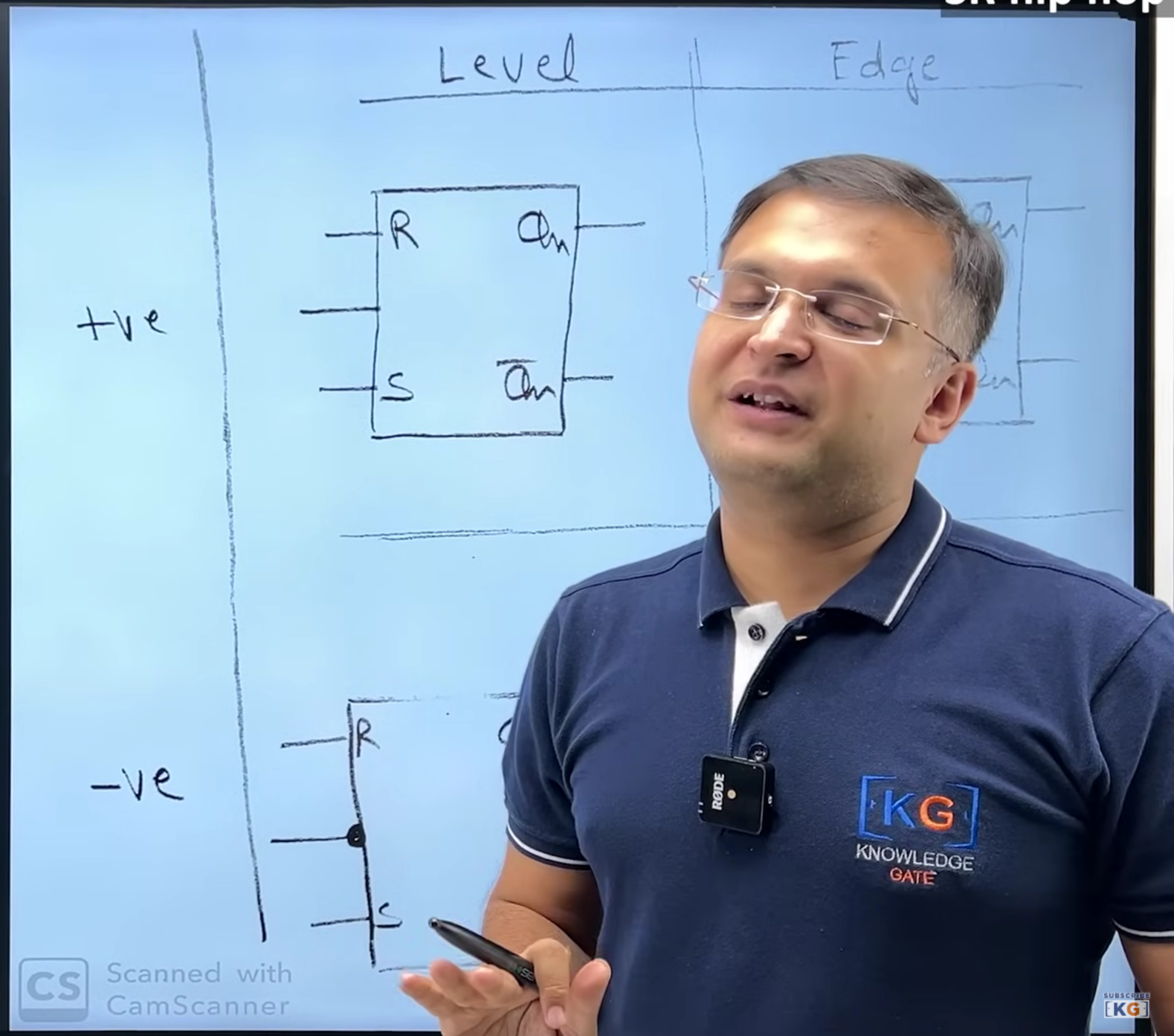
Order of Priority

-ve edge

+ve edge

-ve level

+ve level



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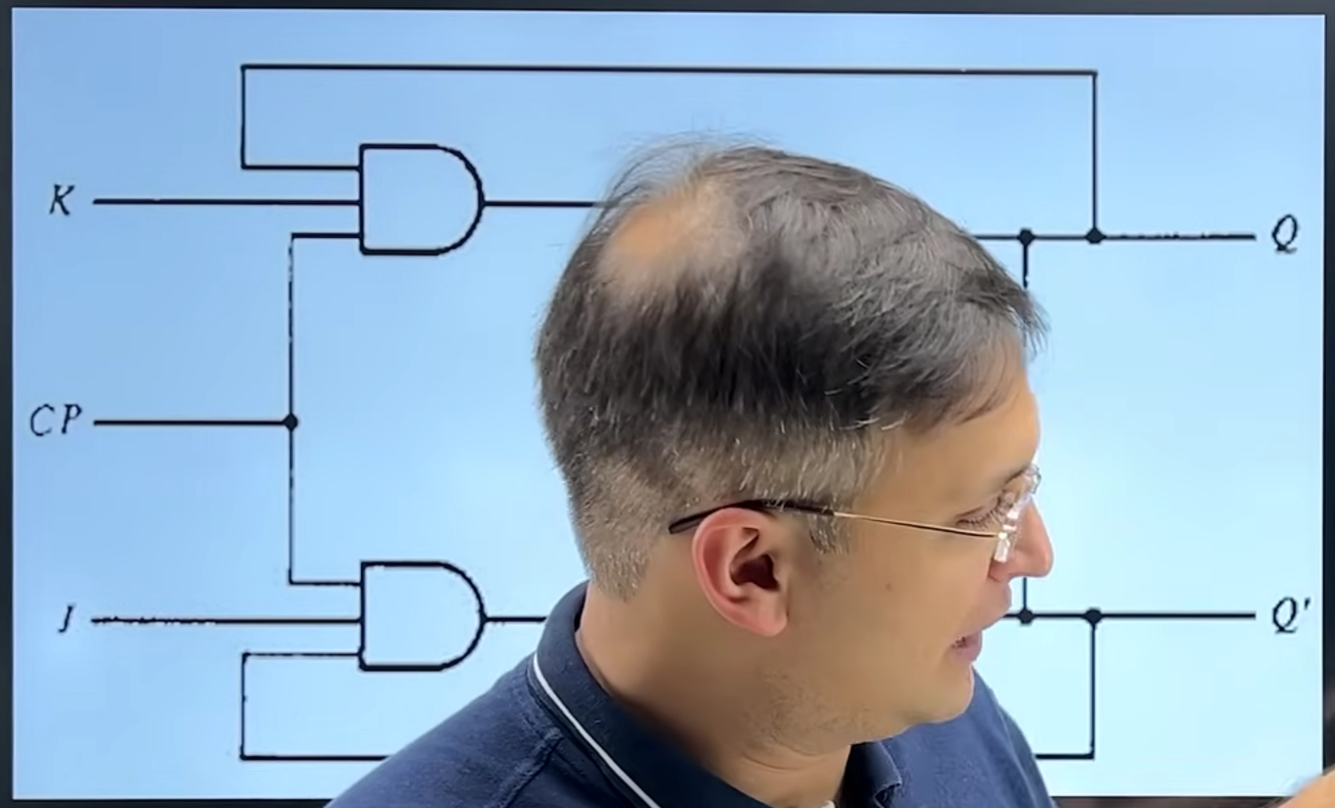
JK flip flop



Truth Table

J/S	K/R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Truth Table

J	K	Q	Q_{n+1}
0	0		0
0	0		
0	1		
0	1		0
1	0		1
1			
1			
1			

K-Map

	JK	J'K'	J'K	JK	JK'
q		00	01	11	10
q'	00			1	1
	01	1			1

Characteristics Equation

Q =

Truth Table

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0		
1	1		

Truth Table

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

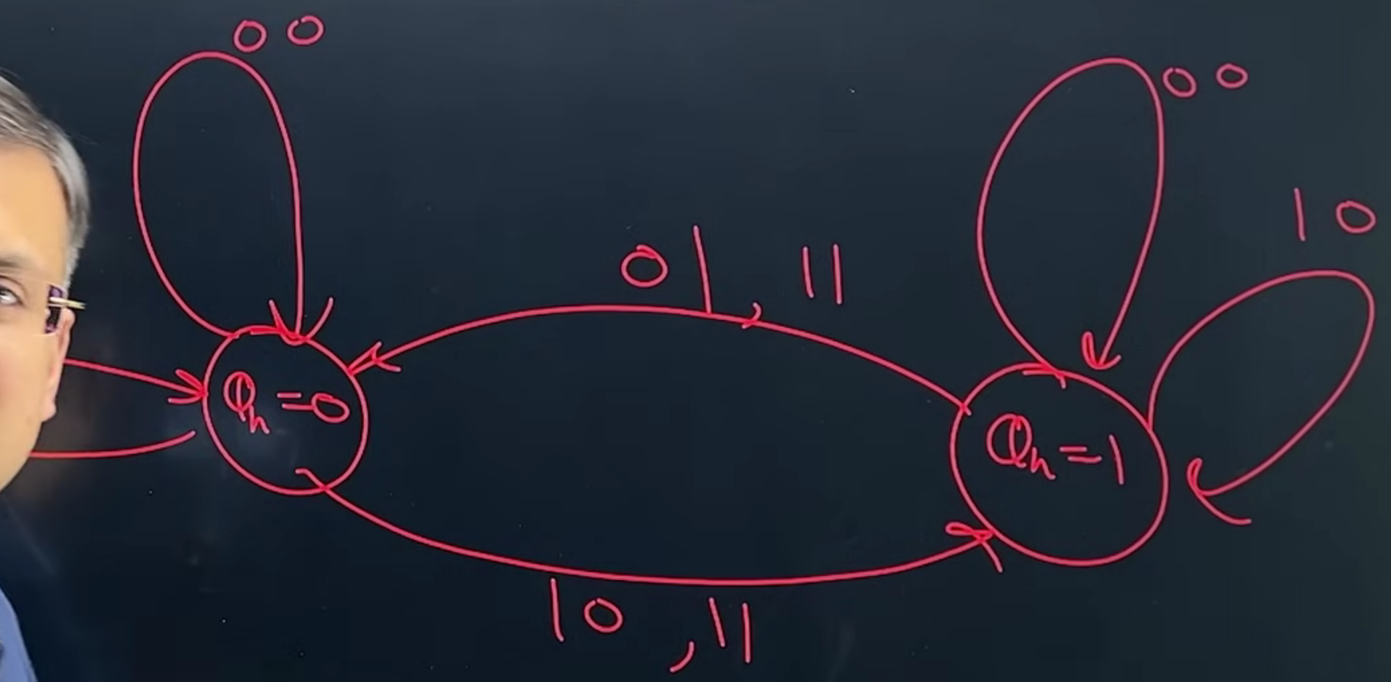
Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Truth Table

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	
1	1		

State Diagram



J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
[illegible]	1	0	0
[illegible]	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Truth Table

T	Q_n	Q_{n+1}
0	0	
0	1	
1	0	
1	1	

Truth Table

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

K-Map

	T	T'	T
q			
q'	0		
q	1		

Characteristics Equ

$Q_{n+1} =$

T(Toggle) flip flop

Truth Table

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Characteristics Equation

$$Q_{n+1} = T \oplus Q_n$$

Function Table

T	Q_{n+1}
0 →	Q_n
1 →	$\overline{Q_n}$

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Convert D Flip Flop to T Flip Flop

Excitation values for characteristics table

T	Q_n	Q_{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

Obtaining simplified expression

T	Q_n	D
0	0	
0	1	
1	0	
1	1	

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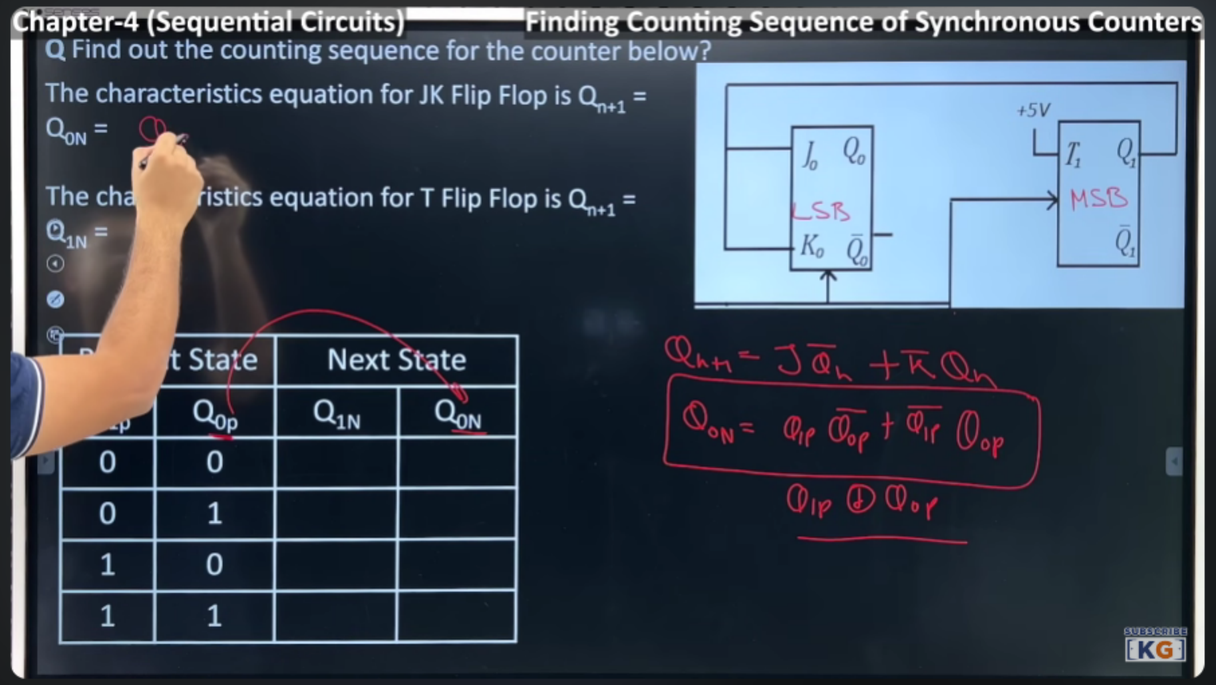

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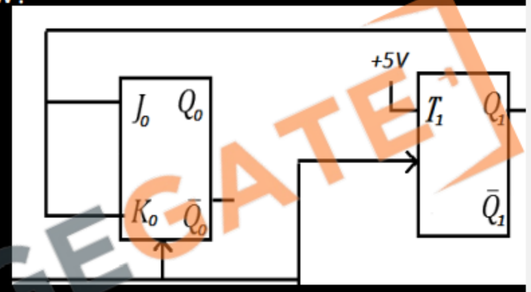
Q Find out the counting sequence for the counter below?

The characteristics equation for JK Flip Flop is Q_{n+1} =
Q_{0N} =

The characteristics equation for T Flip Flop is Q_{n+1} =
Q_{1N} =



Present State		Next State	
Q_{1p}	Q_{0p}	Q_{1N}	Q_{0N}
0	0		
0	1		
1	0		
1	1		

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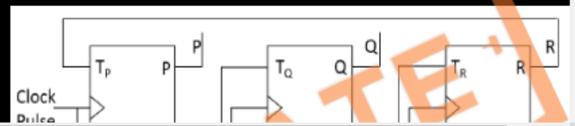
Q Consider a 3-bit counter, designed using T flip-flops, as shown below:



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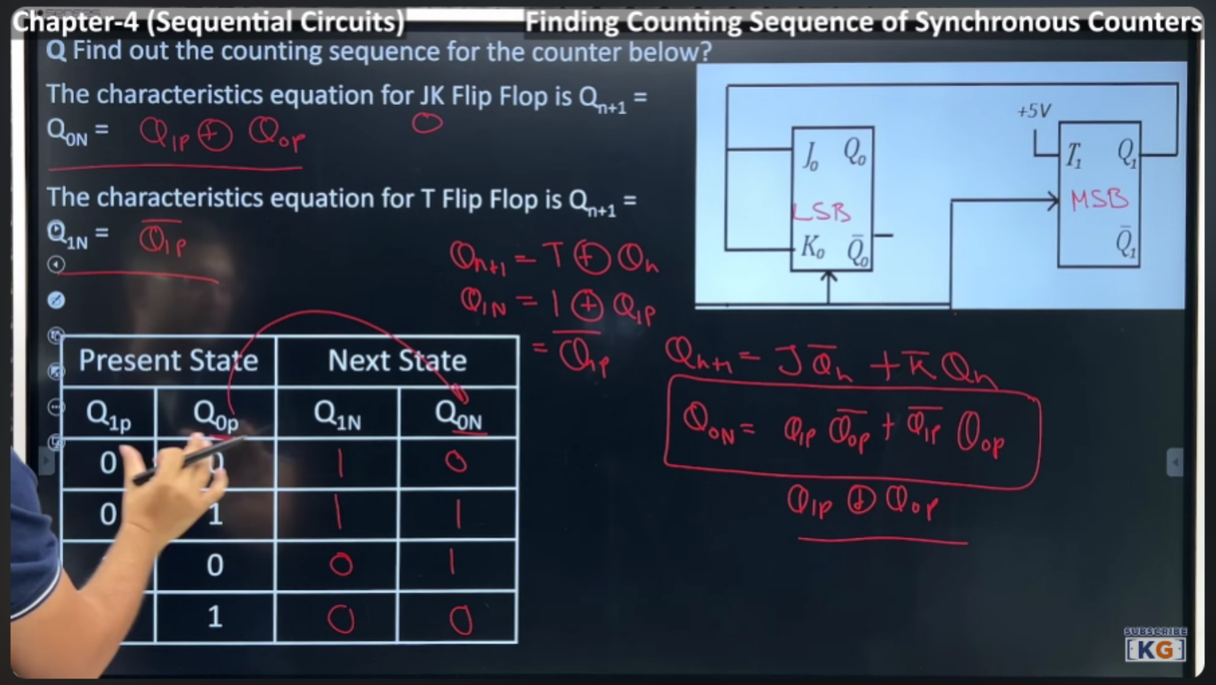

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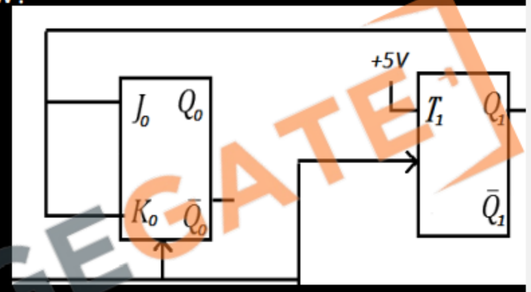
Q Find out the counting sequence for the counter below?

The characteristics equation for JK Flip Flop is Q_{n+1} =
Q_{0N} =

The characteristics equation for T Flip Flop is Q_{n+1} =
Q_{1N} =



Present State		Next State	
Q_{1p}	Q_{0p}	Q_{1N}	Q_{0N}
0	0		
0	1		
1	0		
1	1		

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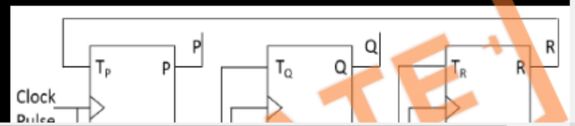
Q Consider a 3-bit counter, designed using T flip-flops, as shown below:



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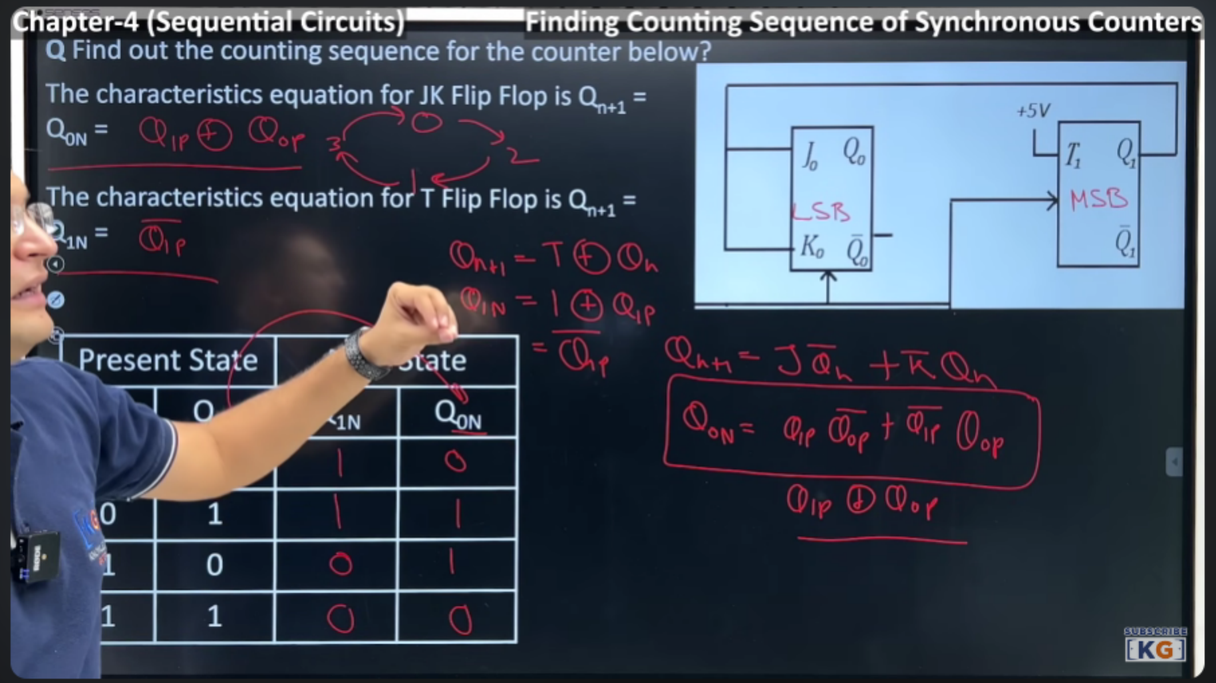

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1	1		

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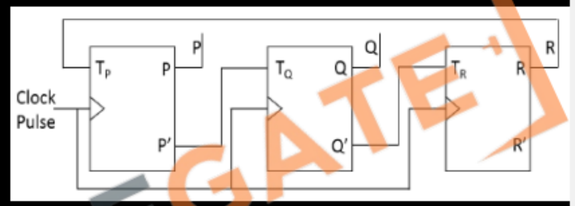
Q Consider a 3-bit counter, designed using T flip-flops, as shown below:



Present State			Next State		
Q_{2p}	Q_{1p}	Q_{0p}	Q_{2N}	Q_{1N}	Q_{0N}
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

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Q Design a synchronous counter for sequence: 0 → 1 → 2 → 3 → 0, using T flip flop.

Present State		Next State	
Q_{1p}	Q_{0p}	Q_{1N}	Q_{0N}
0	0		
0	1		
1	0		

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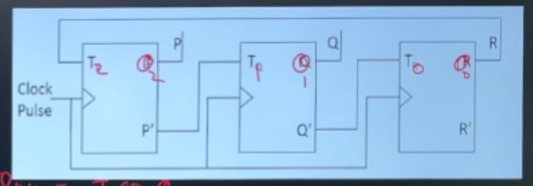
Chapter-4 (Sequential Circuits) Finding Counting Sequence of Synchronous Counters

Q Consider a 3-bit counter, designed using T flip-flops, as shown below:

$Q_{n+1} = T \oplus Q_n$



Present State			Next State		
Q_{2p}	Q_{1p}	Q_{0p}	Q_{2N}	Q_{1N}	Q_{0N}
0	0	0	0	1	1
0	0	1	1	1	0
0	1	0	0	0	0
0	1	1	1	0	1
1	0	0	1	0	1
1	0	1	0	0	0
1	1	0	1	1	0
1	1	1	0	1	1

$Q_{2N} = Q_{0p} \oplus Q_{2p}$

$Q_{1N} = \overline{Q_{2p}} \oplus Q_{1p}$

$Q_{1N} = Q_{2p} \odot Q_{1p}$

$Q_{0N} = \overline{Q_{1p}} \oplus Q_{0p}$

$Q_{0N} = Q_{1p} \odot Q_{0p}$

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Present State		Next State	
Q_{1p}	Q_{0p}	Q_{1N}	Q_{0N}
0	0		
0	1		
1	0		
1	1		

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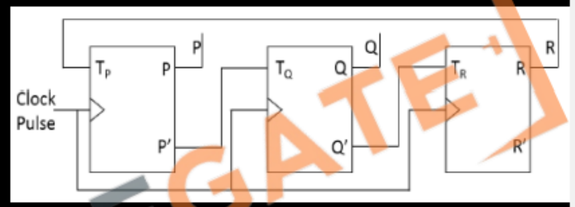
Q Consider a 3-bit counter, designed using T flip-flops, as shown below:



Present State			Next State		
Q_{2p}	Q_{1p}	Q_{0p}	Q_{2N}	Q_{1N}	Q_{0N}
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

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Q Design a synchronous counter for sequence: 0 → 1 → 2 → 3 → 0, using T flip flop.

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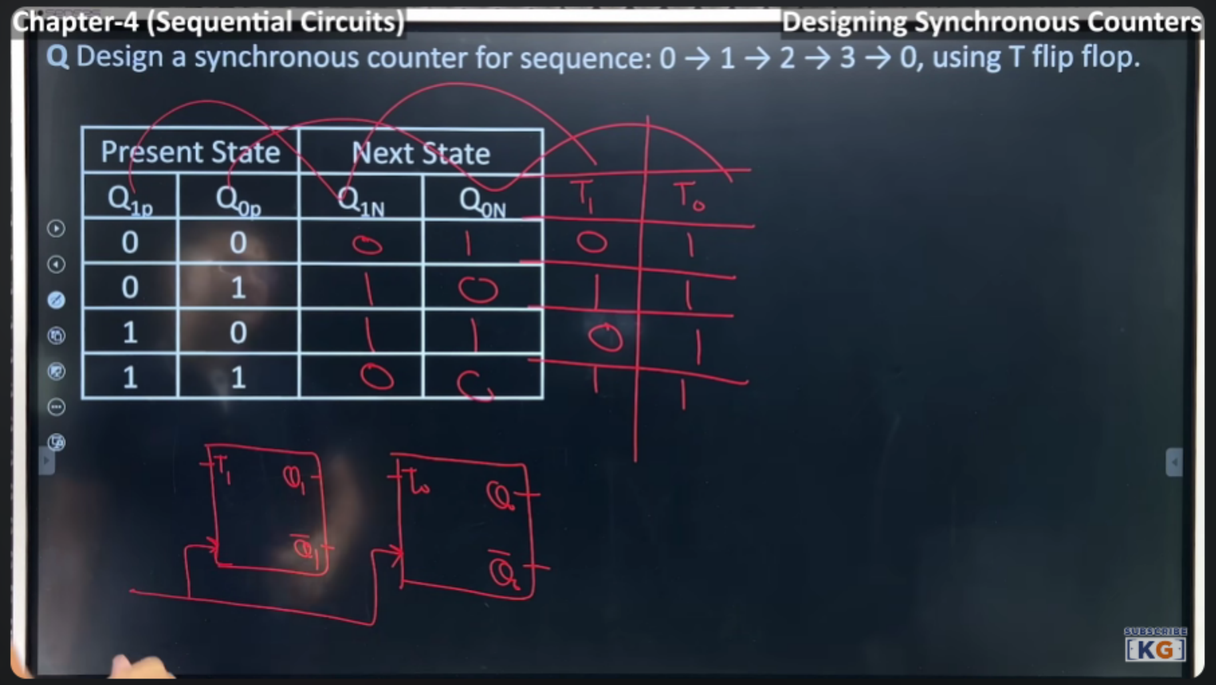

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Q Example: Design a synchronous counter for sequence: 0 → 1 → 2 → 3 → 0, using D flip flop.

Present State		Next State	
Q_{1p}	Q_{0p}	Q_{1N}	Q_{0N}
0	0		
0	1		
1	0		
1	1		

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Q Design synchronous counter for sequence: 0 → 1 → 3 → 4 → 5 → 7 → 0, using T flip-flop.

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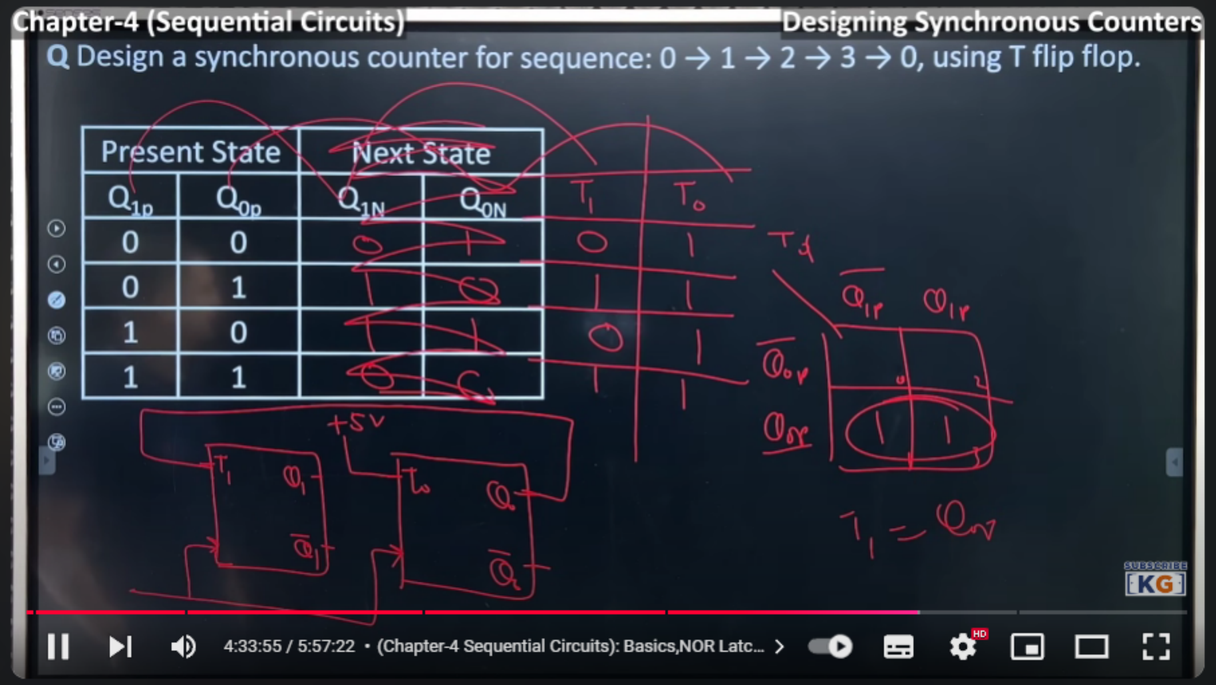

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Q Example: Design a synchronous counter for sequence: 0 → 1 → 2 → 3 → 0, using D flip flop.

Present State		Next State	
Q_{1p}	Q_{0p}	Q_{1N}	Q_{0N}
0	0		
0	1		
1	0		
1	1		

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Q Design synchronous counter for sequence: 0 → 1 → 3 → 4 → 5 → 7 → 0, using T flip-flop.

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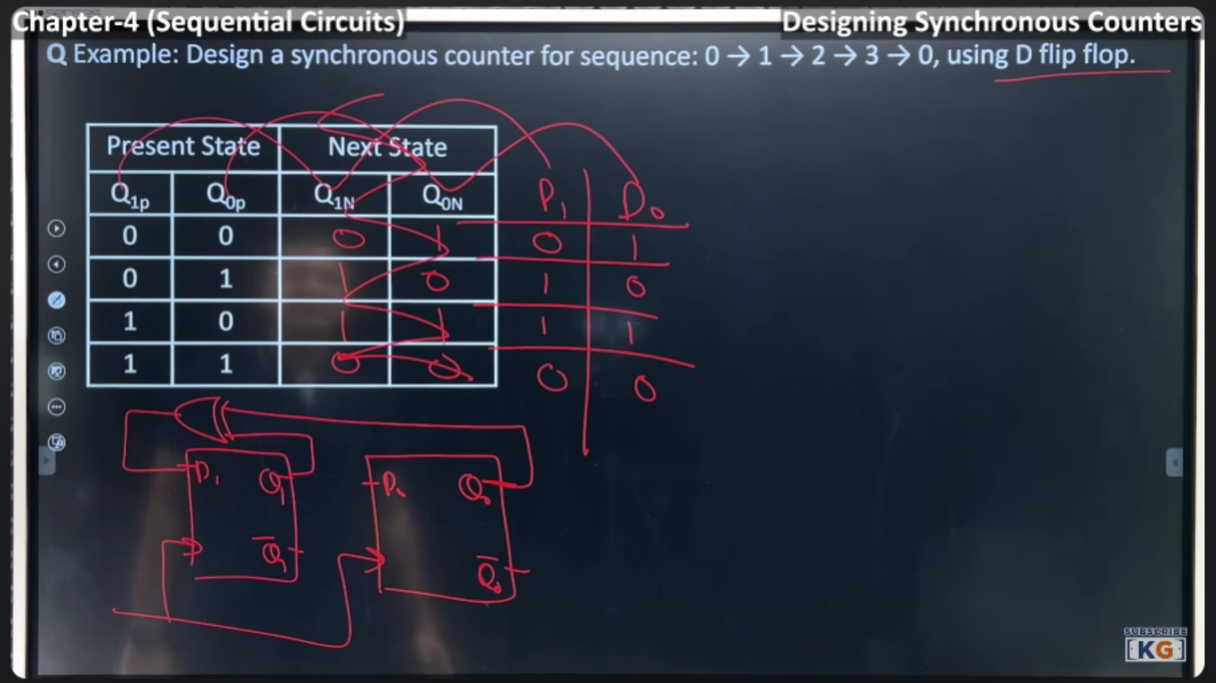

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Q Example: Design a synchronous counter for sequence: 0 → 1 → 2 → 3 → 0, using D flip flop.

Present State		Next State	
Q_{1p}	Q_{0p}	Q_{1N}	Q_{0N}
0	0		
0	1		
1	0		
1	1		

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Q Design synchronous counter for sequence: 0 → 1 → 3 → 4 → 5 → 7 → 0, using T flip-flop.

Present State			Next State		
0	0	0	0	0	0

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Chapter-4 (Sequential Circuits) Designing Synchronous Counters

Q Example: Design a synchronous counter for sequence: 0 → 1 → 2 → 3 → 0, using D flip flop.

Present State		Next State	
Q_{1p}	Q_{0p}	Q_{1N}	Q_{0N}
0	0		
0	1		
1	0		
1	1		

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Q Example: Design a synchronous counter for sequence: 0 → 1 → 2 → 3 → 0, using D flip flop.

Present State		Next State	
Q_{1p}	Q_{0p}	Q_{1N}	Q_{0N}
0	0		
0	1		
1	0		
1	1		

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Q Design synchronous counter for sequence: 0 → 1 → 3 → 4 → 5 → 7 → 0, using T flip-flop.

Present State			Next State		
0	0	0	0	0	0

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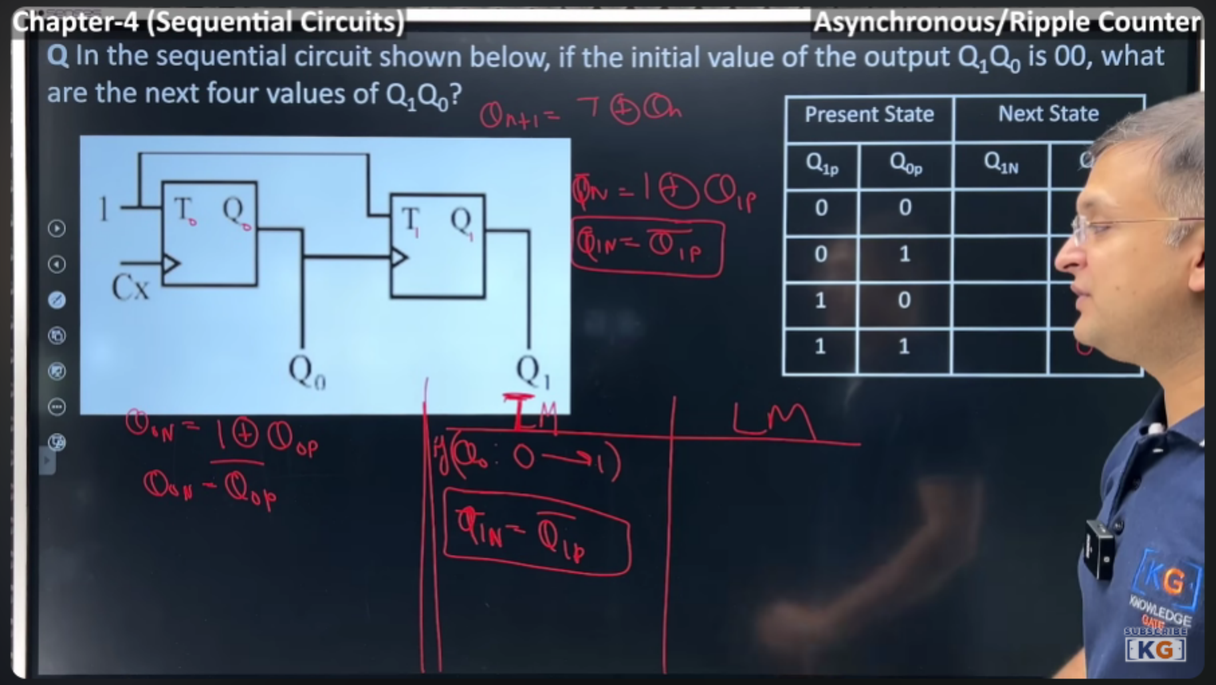

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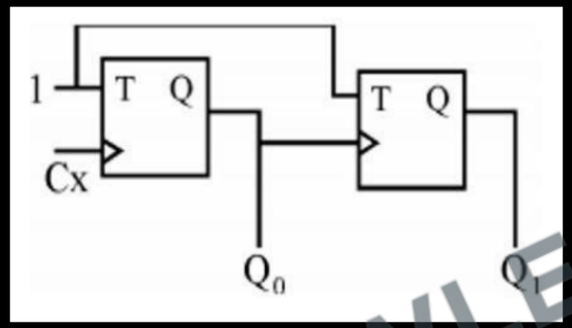
Q In the sequential circuit shown below, if the initial value of the output Q_1Q_0 is 00, what are the next four values of Q_1Q_0?



Present State		Next State	
Q_{1p}	Q_{0p}	Q_{1N}	Q_{0N}
0	0		
0	1		
1	0		
1	1		

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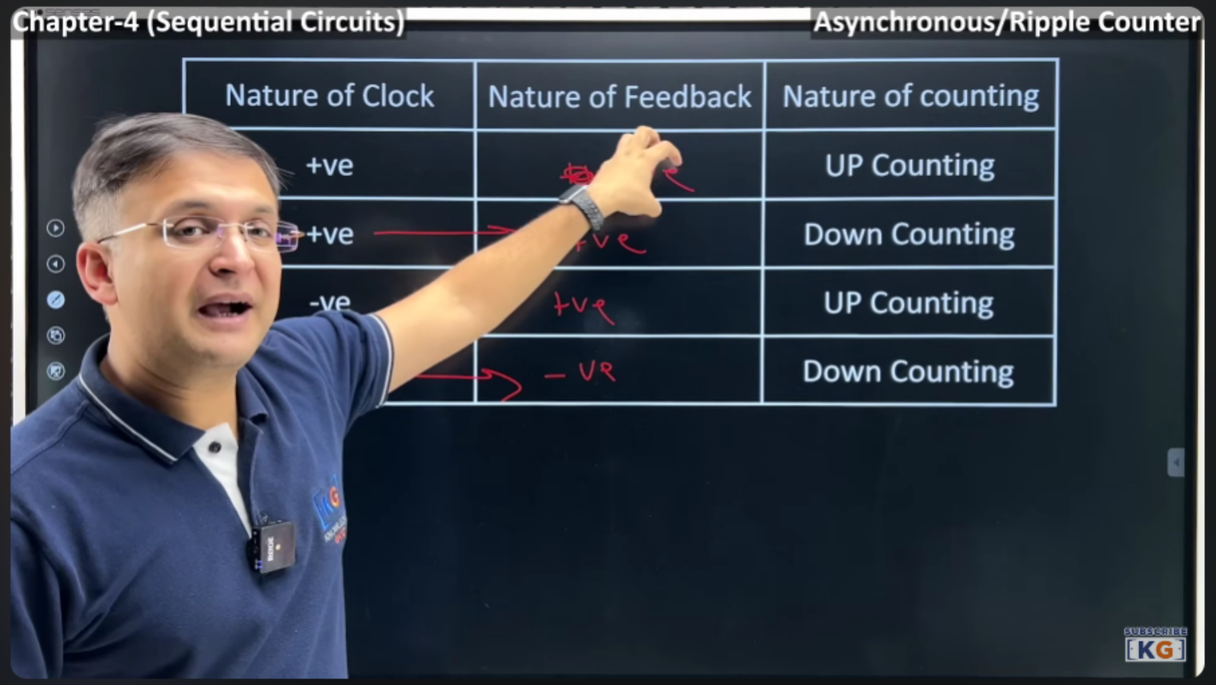

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Nature of Clock	Nature of Feedback	Nature of counting
+ve		UP Counting
+ve		Down Counting
-ve		UP Counting
-ve		Down Counting

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Asynchronous counters

SYNCHRONOUS COUNTER	ASYNCHRONOUS COUNTER
In synchronous counter, all flip flops are triggered with same clock simultaneously.	In asynchronous counter, different flip flops are triggered with different clock, not simultaneously.
Synchronous Counter is faster than asynchronous counter in operation. $T_{delay} = T_{FF} + T_{CC}$	Asynchronous Counter is slower than synchronous counter in operation. $T_{delay} = n \times T_{FF} + T_{CC}$

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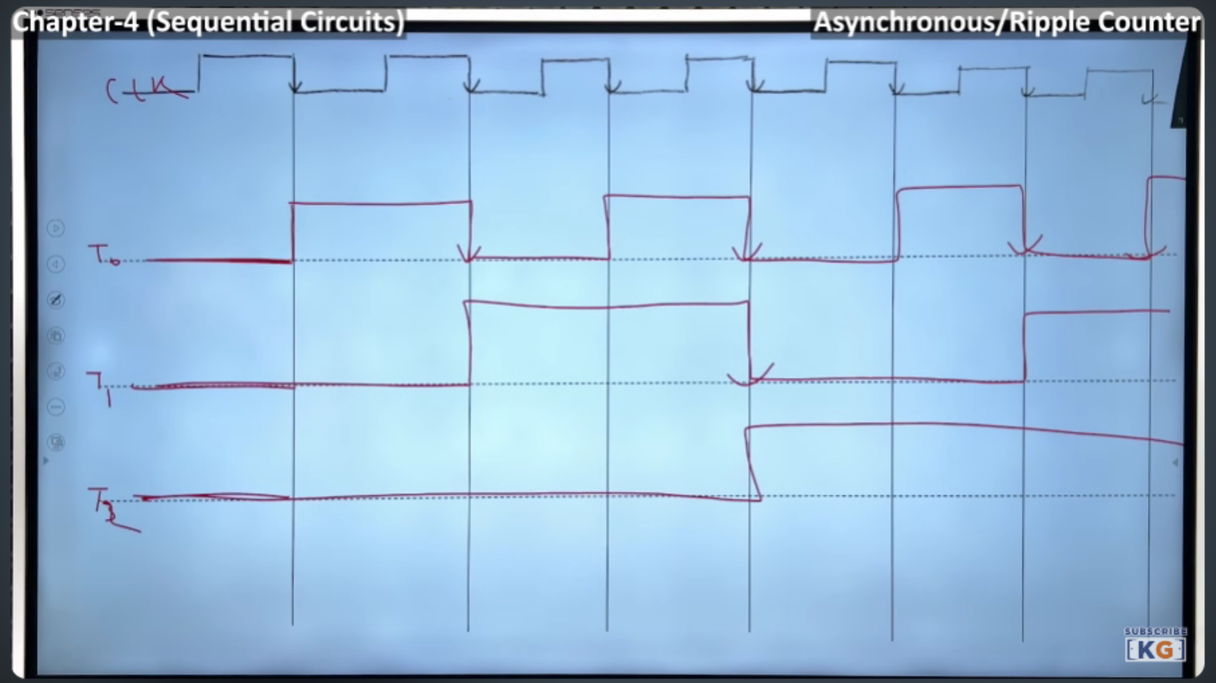

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Asynchronous counters

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Synchronous Counter is faster than asynchronous counter in operation. $T_{delay} = T_{FF} + T_{CC}$	Asynchronous Counter is slower than synchronous counter in operation. $T_{delay} = n \times T_{FF} + T_{CC}$
Synchronous Counter is also called Parallel Counter.	Asynchronous Counter is also called Serial Counter.
Synchronous Counter designing as well implementation are complex due to increasing the number of states.	Asynchronous Counter designing as well as implementation is very easy.
Synchronous Counter will operate in any desired count sequence.	Asynchronous Counter will operate only in fixed count sequence (UP/DOWN).
Synchronous Counter examples are: Ring counter, Johnson counter.	Asynchronous Counter examples are: Ripple UP counter, Ripple DOWN counter.
A synchronous sequential circuit is a system whose behavior can be defined from the knowledge of its signals at discrete instants of time.	The behavior of an asynchronous sequential circuit depends upon the input signals at any instant of time and the order in which the inputs change.

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Registers

- Registers are basically storing devices which are also designed using basic element called flip-flop.
- D-flip-flop are most popular choice for register because they don't perform any functionality and output is simply based on current input so, they act as a buffer.
- Apart from storing registers sometimes also be used in performing basic mathematical operation like multiply by 2 by left shit and divide by 2 by right shift.

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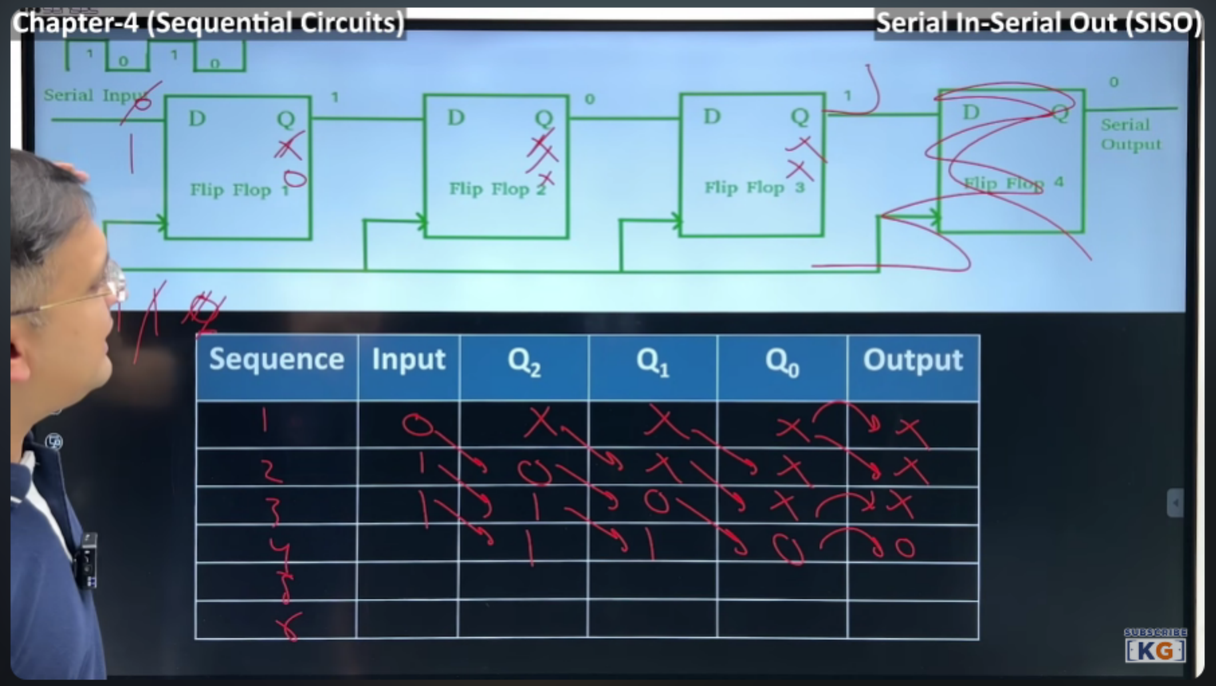

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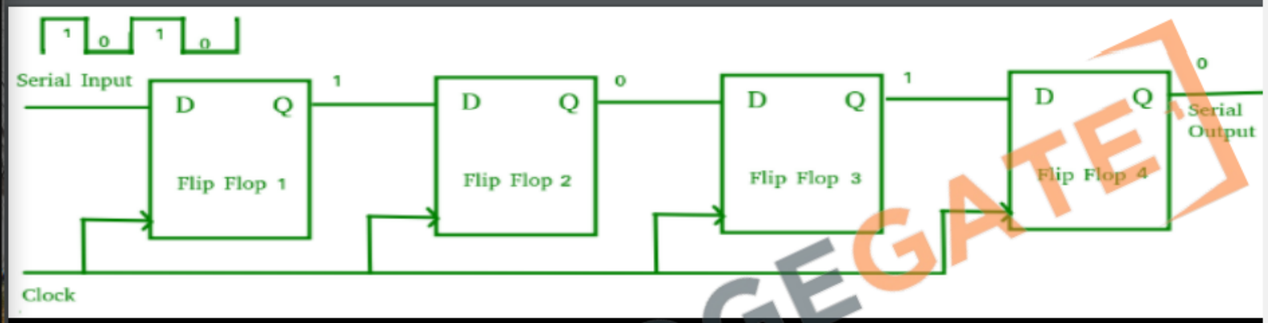

Sequence	Input	Q_2	Q_1	Q_0	Output

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- The main use of a SISO is to act as a delay element.
- In SISO registers to provide n bit data serially in it requires n clock pulse and to provide serial output it requires n - 1 clock pulses.

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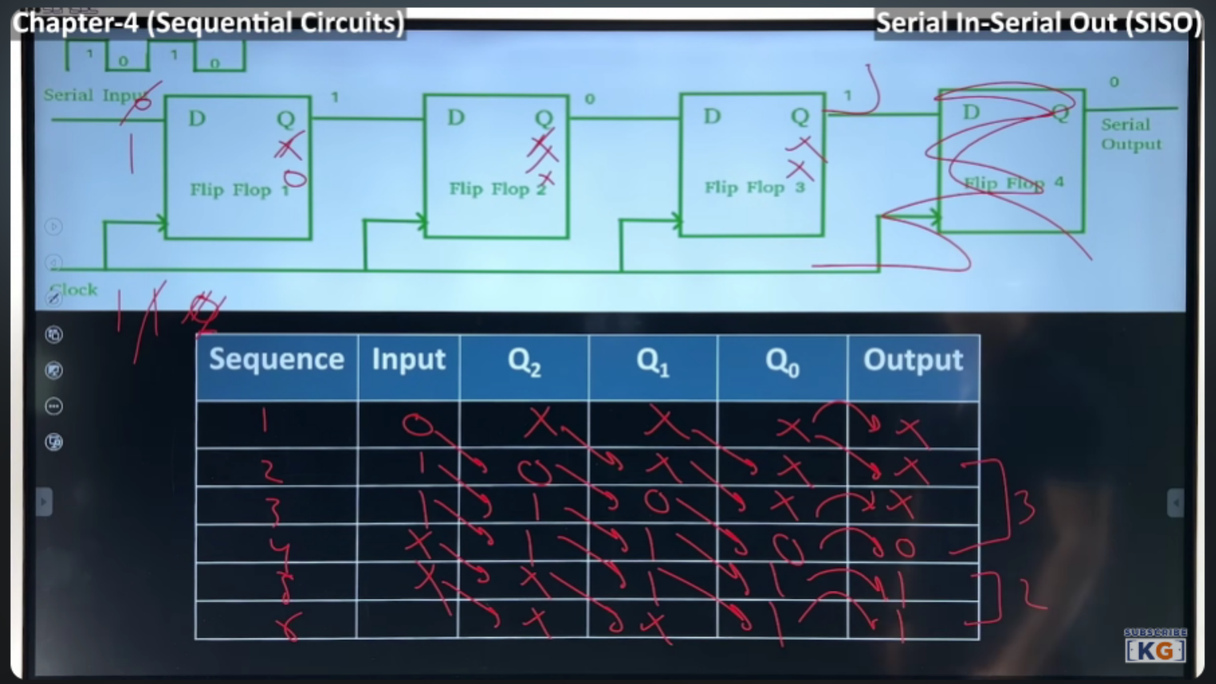

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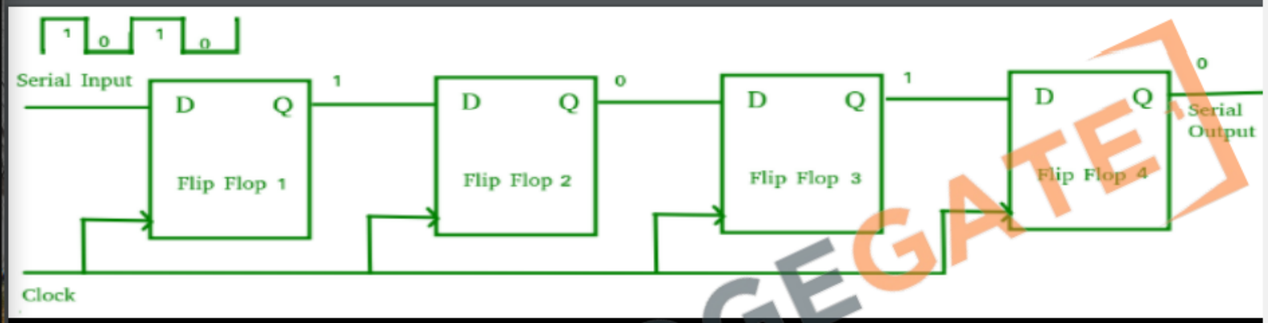

Sequence	Input	Q_2	Q_1	Q_0	Output

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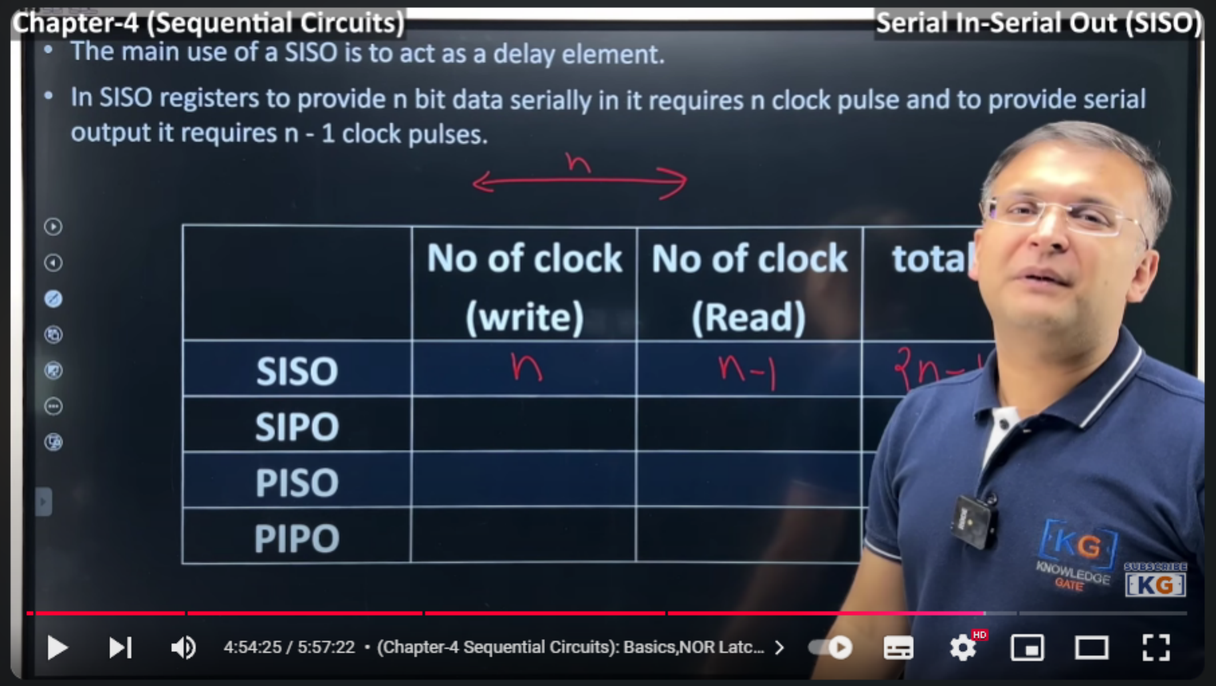

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- The main use of a SISO is to act as a delay element.
- In SISO registers to provide n bit data serially in it requires n clock pulse and to provide serial output it requires n - 1 clock pulses.

	No of clock (write)	No of clock (Read)	total
SISO			
SIPO			
PISO			
PIPO			

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Serial-In Parallel-Out shift Register (SIPO)

- The shift register, which allows serial input (one bit after the other through a single data line) and produces a parallel output is known as Serial-In Parallel-Out shift register.

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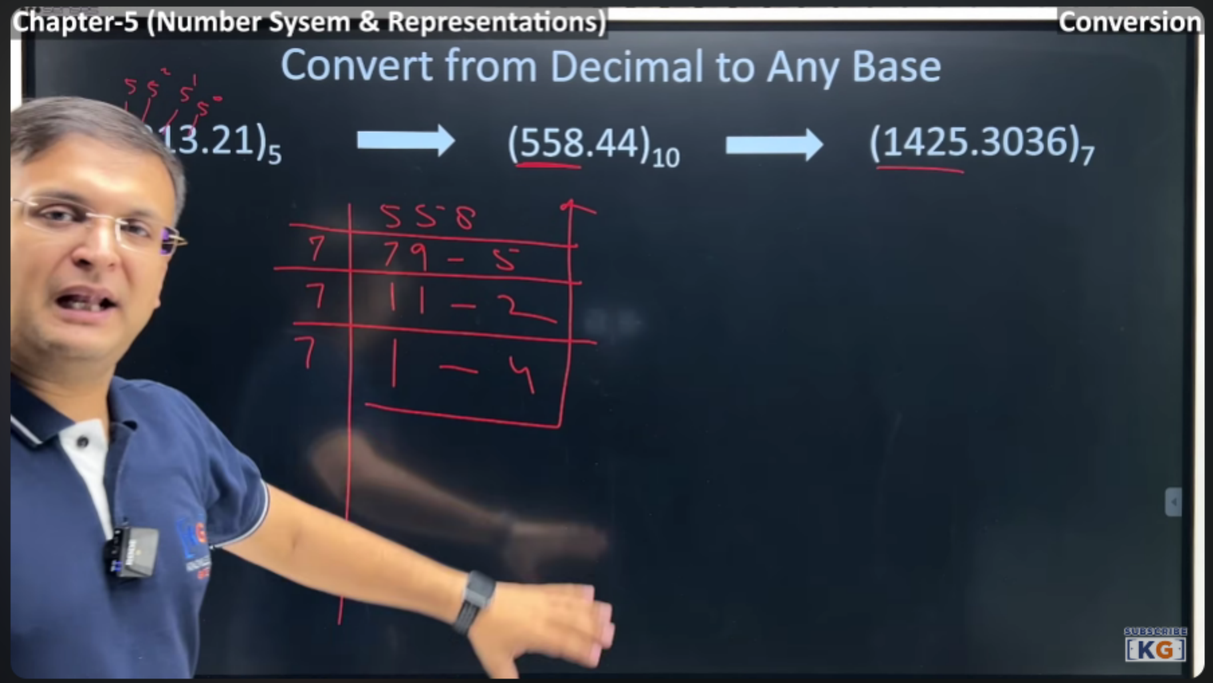

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$(109.125)_{10} \longrightarrow (1101101.001)_2$

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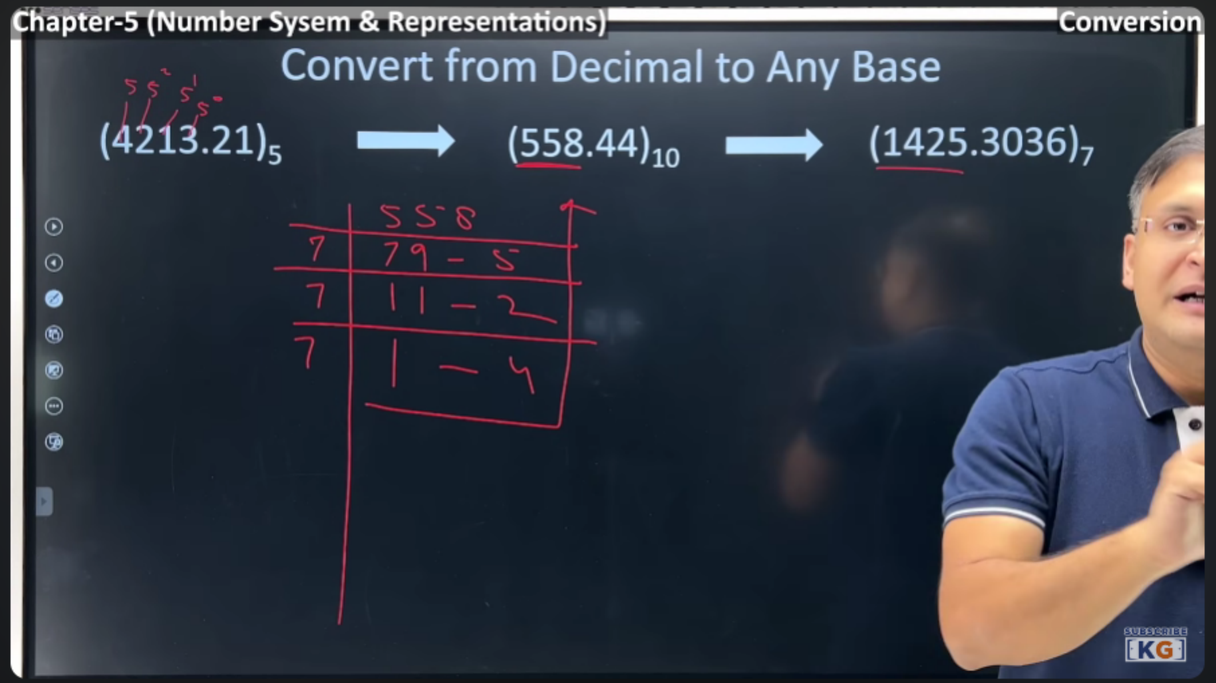

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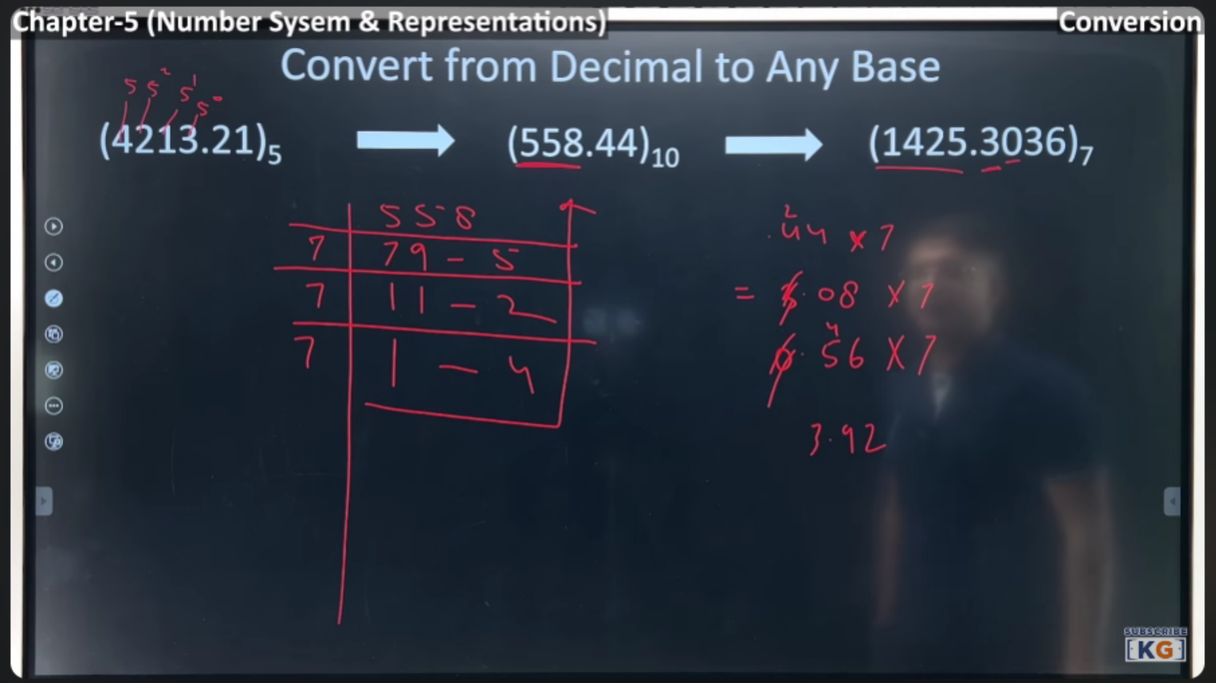

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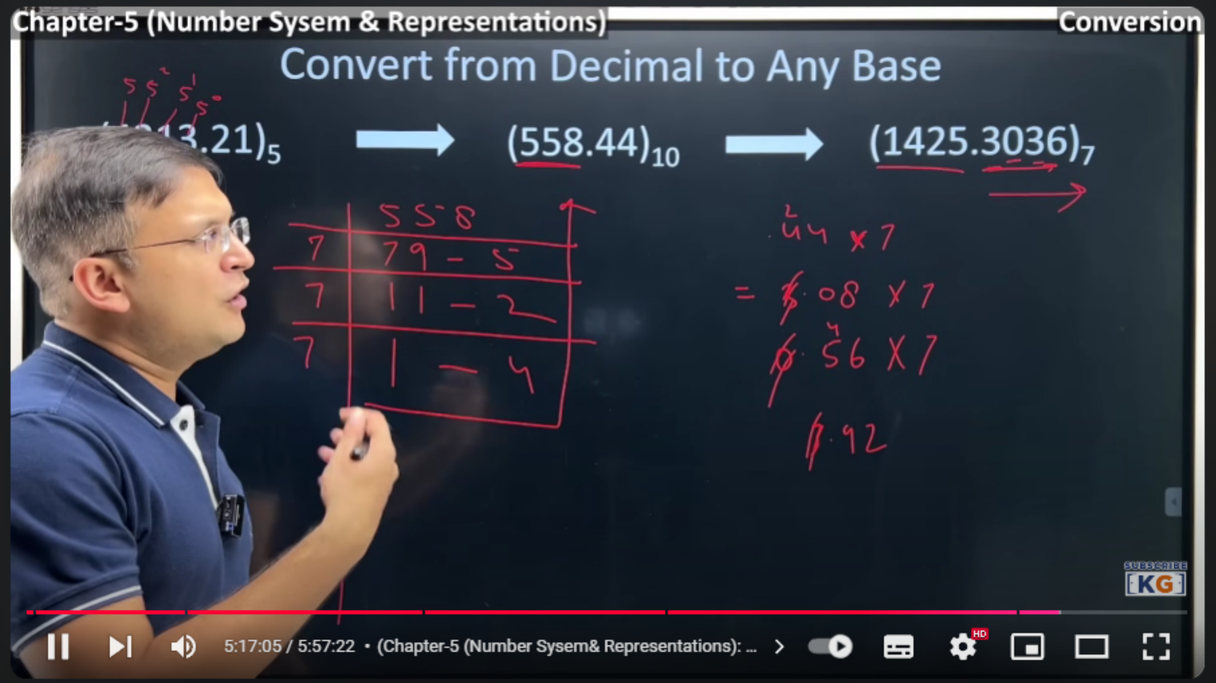

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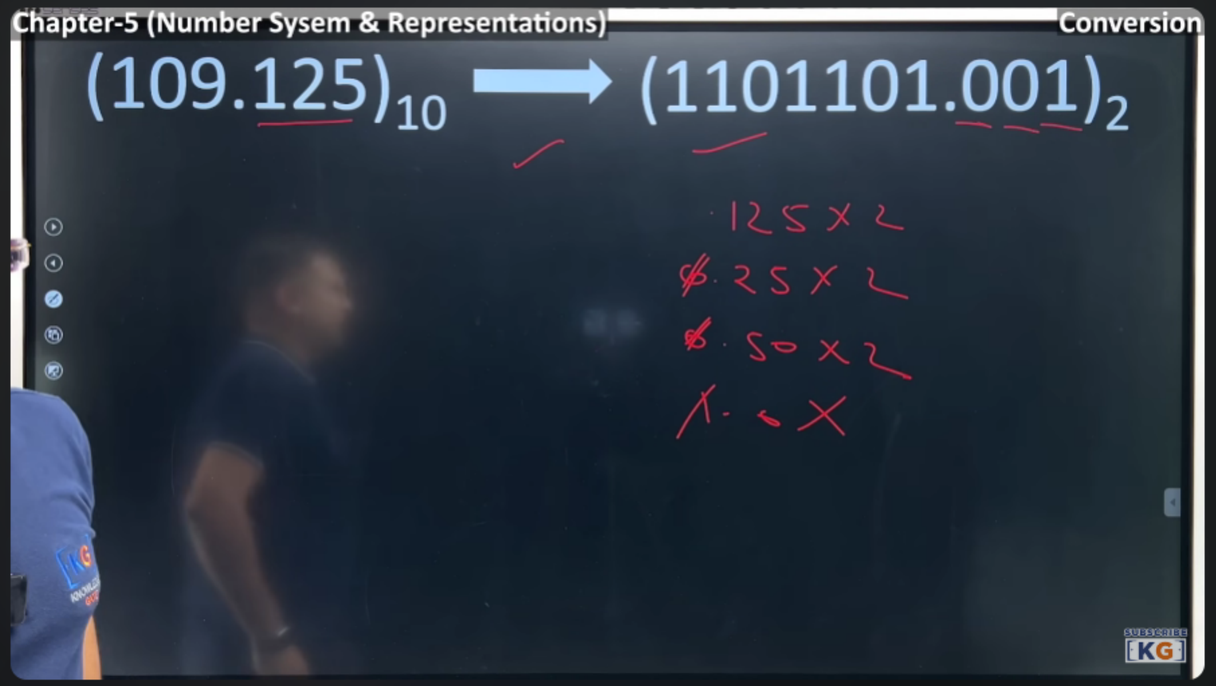

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Octal Number System

$(127.4)_8$

$$1 * 8^2 + 2 * 8^1 + 7 * 8^0 + 4 * 8^{-1} = (87.5)_{10}$$

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Hexadecimal Number System

- When the base of a number system is higher than 10, we use letters from the alphabet to represent the extra digits. For instance, in the Hexadecimal System, which is base-16, the first 10 digits are the same as in the Decimal System: 0 to 9. After that, the letters A, B, C, D, E, and F stand for the numbers 10, 11, 12, 13, 14, and 15 respectively. The hexadecimal system is most popular in digital systems.

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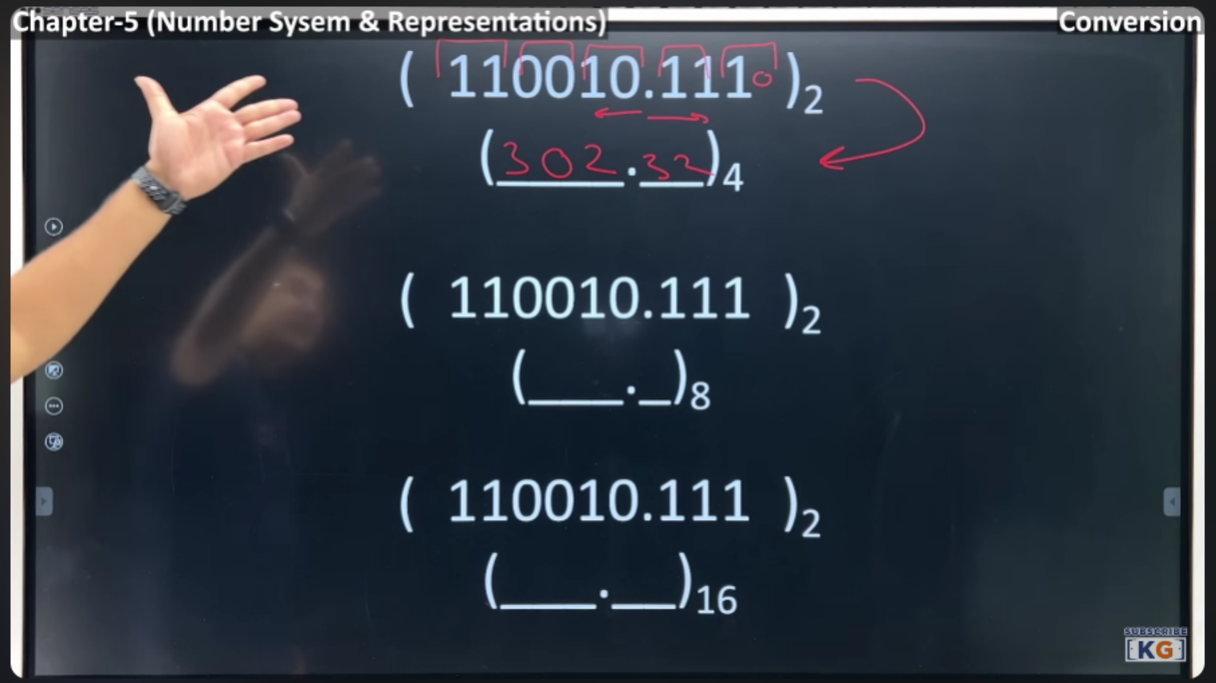

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1100	12-C
1101	13-D
1110	14-E
1111	15-F

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$$(110010.111)_2$$
$$(____.__)_4$$

$$(110010.111)_2$$
$$(___._)_8$$

$$(110010.111)_2$$
$$(___.__)_{16}$$

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$$(62.7)_8$$

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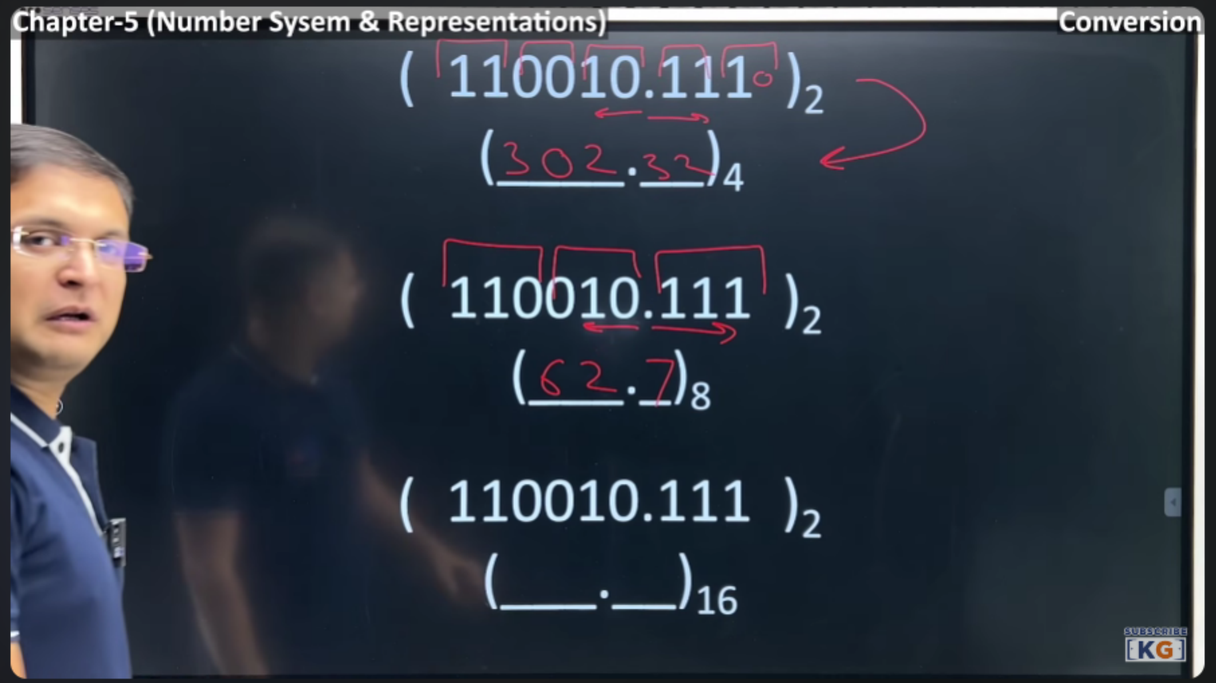

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$(____.__)_4$

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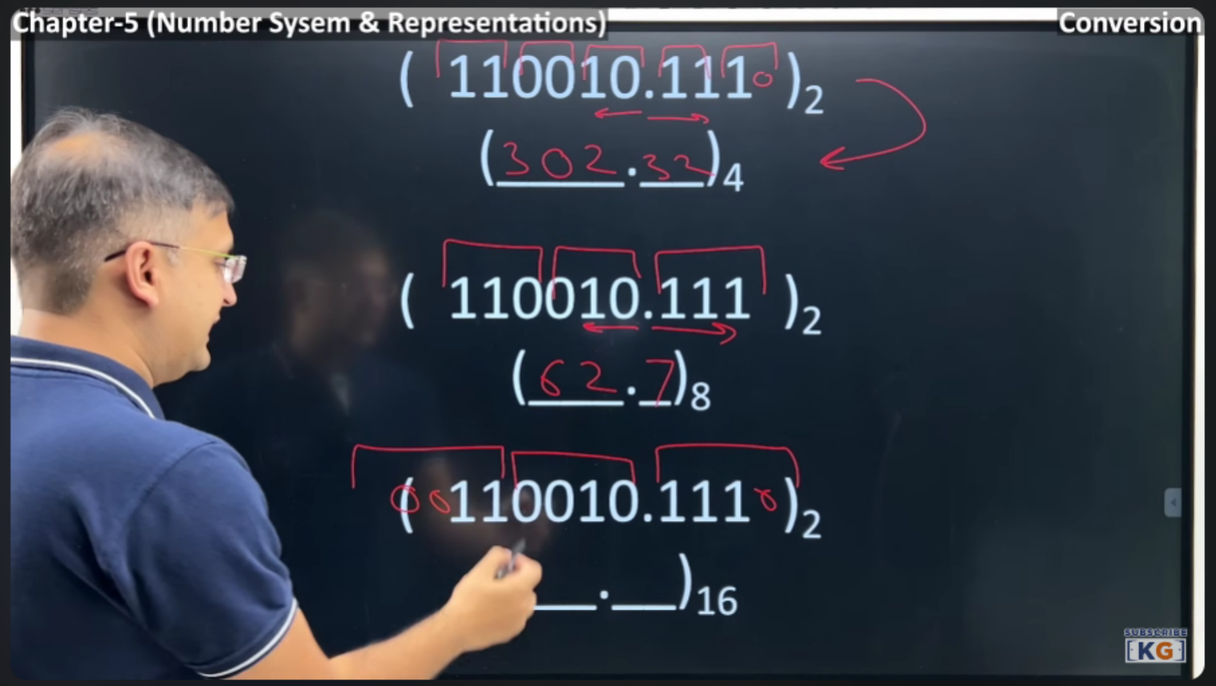

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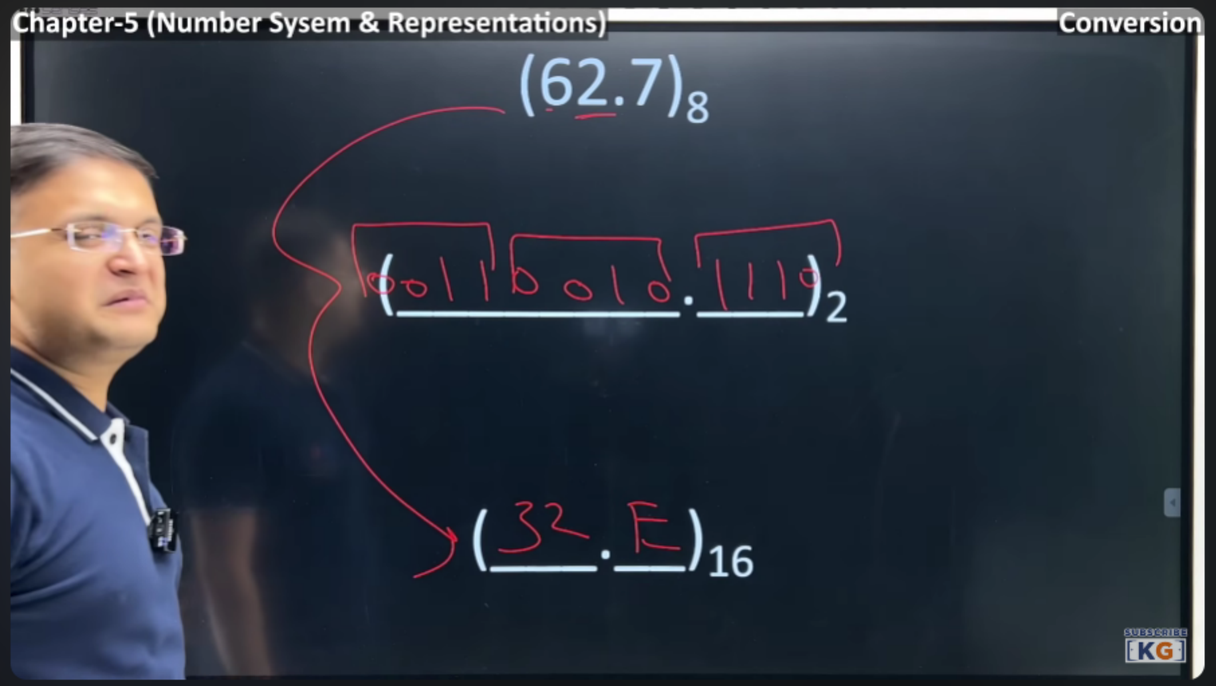

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$(____.___)_{16}$

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Representation of a number

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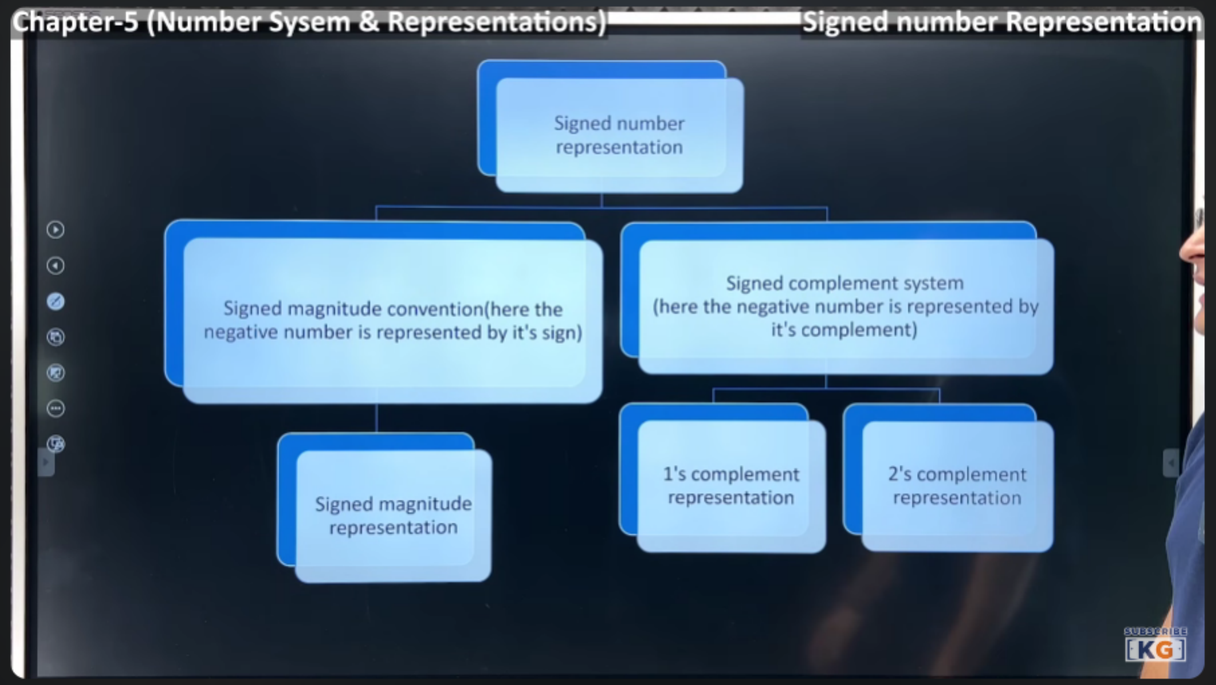

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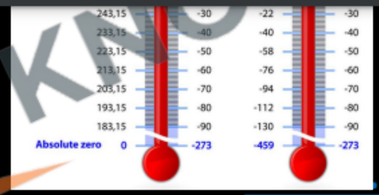

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- In a computer, an n-bit word can store a signed binary number. One usually the leftmost bit is set aside to show if the number is positive or negative, and the other n-1 bits represent the size or magnitude of the number.
- Because of the limitation of the computer hardware as circuit only understand 0 and 1, every piece of information in computer must be represented in terms of numbers i.e. 0 and 1, weather it is sign or magnitude. where first left most bit 0 means +Ve number and 1 means -Ve number.

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Chapter-5 (Number Sysem & Representations) 2's Complement

Decimal	Signed Magnitude	1's Complement	2's Complement
+7	0111	0111	0111
+6	0110	0110	0110
+5	0101	0101	0101
+4	0100	0100	0100
+3	0011	0011	0011
+2	0010	0010	0010
+1	0001	0001	0001
+0	0000	0000	0000
-0	1000	1111	0000
-1	1001	1110	1111
-2	1010	1101	1110
-3	1011	1100	1101
-4	1100	1011	1100
-5	1101	1010	1011
-6	1110	1001	1010
-7	1111	1000	1001
-8	-------	-------	1000

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- 2's Complement

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Sign magnitude representation

- **Introduction: -** It is the simplest form of representation, where in an n-bit word, the right most n-1 bits (from LSB) hold the magnitude of the number and n^{th} bit (Left most, MSB) is assigned for sign, where 0→+ve and 1→-ve.
- **Range: -** from $-(2^{n-1}-1)$ to $+(2^{n-1}-1)$ total 2^n -1
- **Advantage: -** Easy to read and write, because it is a weighted code system, directly reading and writing is possible.
- **Disadvantage: -** One drawback in sign-magnitude representation is addition and subtraction require separate handling of the sign and the magnitude. One more problem is there are two representation for 0, i.e. -0 & +0, because of which there is a loss of one presentation, and create confusion.
- **Number extension : -** In computer the size of a location is fixed, so it is often required to write a smaller number in a larger space, this can be done by sign extension, where, the magnitude is written as far right as possible, sign bit is written left most, and all the empty cells must be filled/padded with zero.

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1's Complement Representation

- **Introduction: -** here the negative number is represented by taking complement.
- **Range: -** from $-(2^{n-1}-1)$ to $+(2^{n-1}-1)$, total 2^n -1 representation

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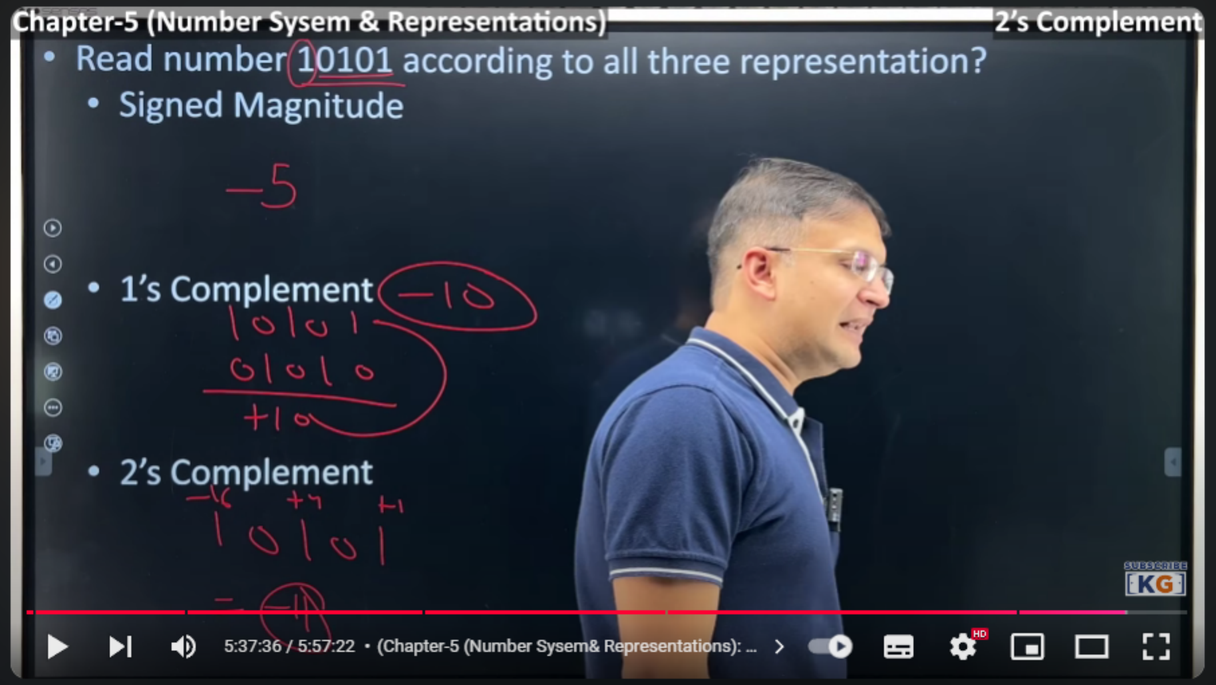

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-4	1100	1011	1100
-5	1101	1010	1011
-6	1110	1001	1010
-7	1111	1000	1001
-8	-------	-------	1000

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- Represent decimal number -13 in all three methods?
  - Signed Magnitude
  - 1's Complement
  - 2's Complement

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- Read number 10101 according to all three representation?
  - Signed Magnitude

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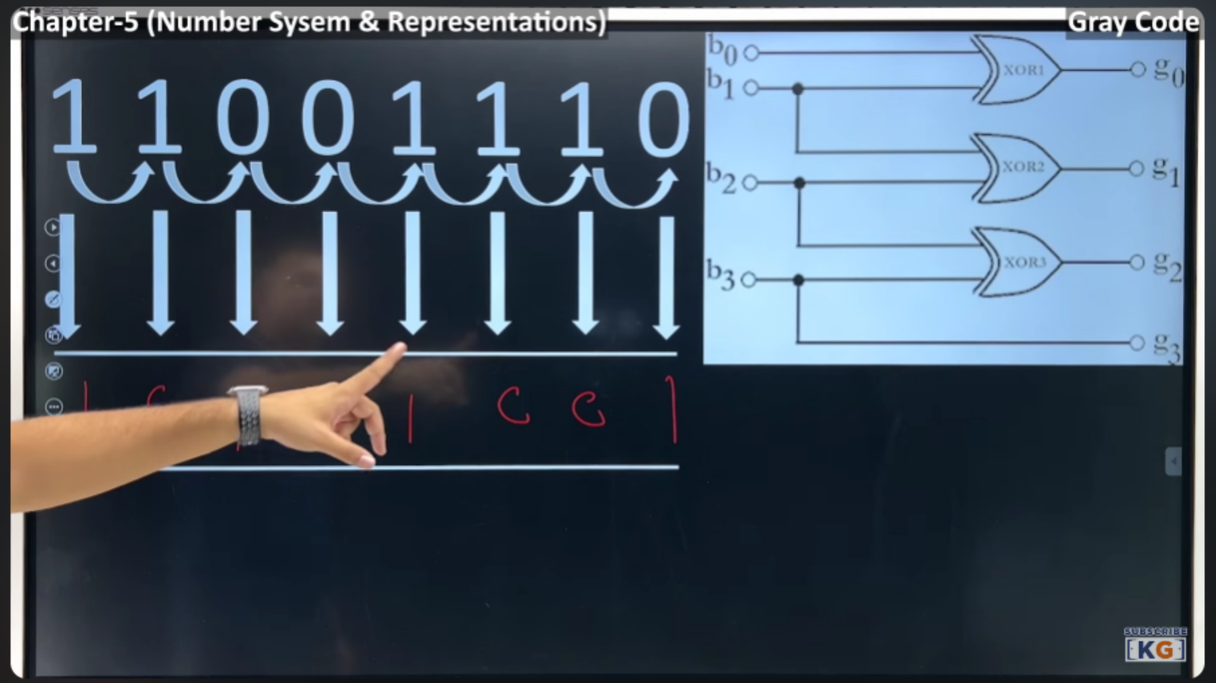

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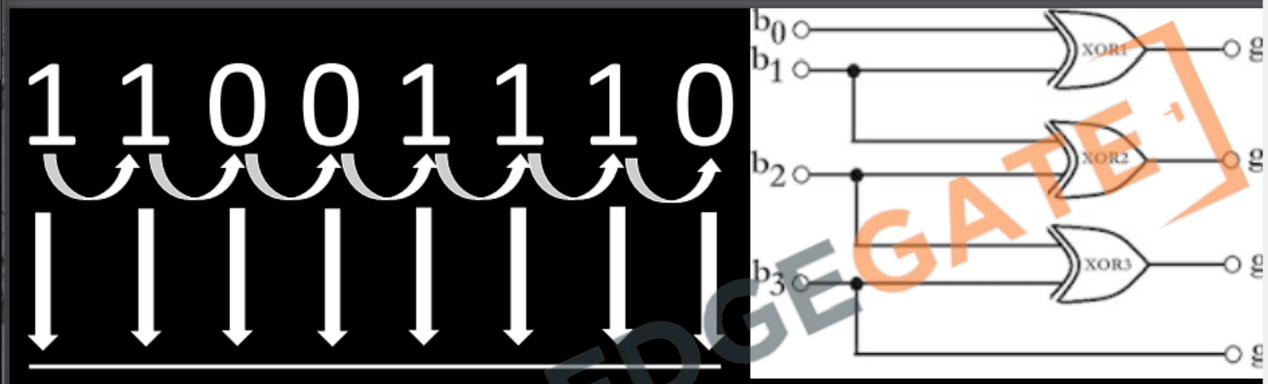

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- $G_0 = B_1 \oplus B_0$
- $G_1 = B_2 \oplus B_1$
- $G_2 = B_3 \oplus B_2$
- $G_3 = B$

4-bit binary				4-bit gray			
B_4	B_3	B_2	B_1	G_4	G_3	G_2	G_1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0

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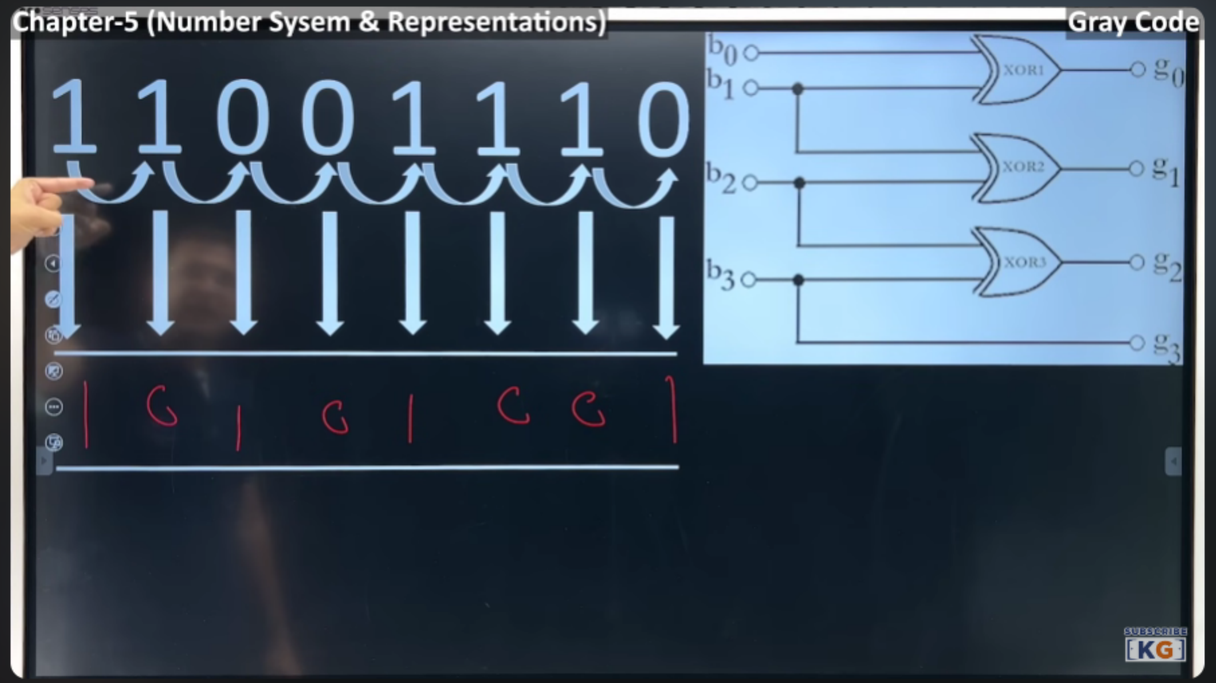

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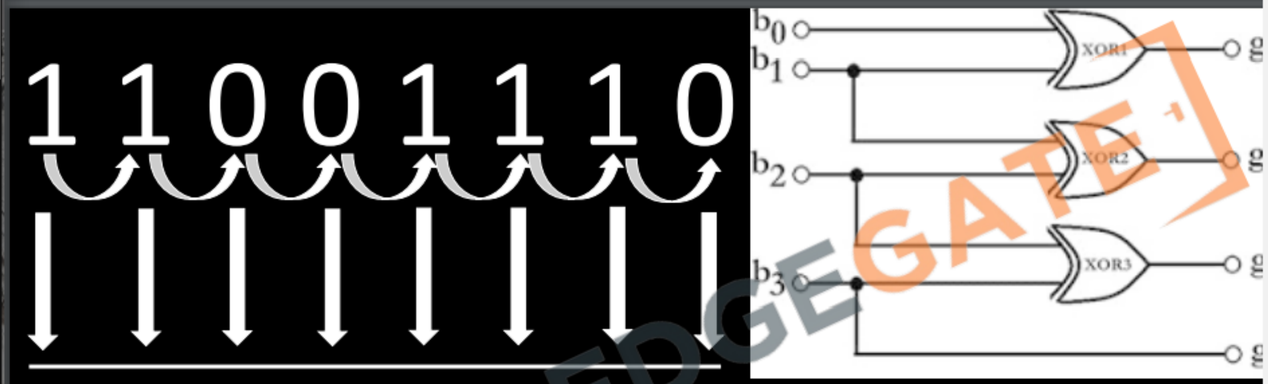

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- $G_0 = B_1 \oplus B_0$
- $G_1 = B_2 \oplus B_1$
- $G_2 = B_3 \oplus B_2$
- $G_3 = B_3$

4-bit binary				4-bit gray			
B_4	B_3	B_2	B_1	G_4	G_3	G_2	G_1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0

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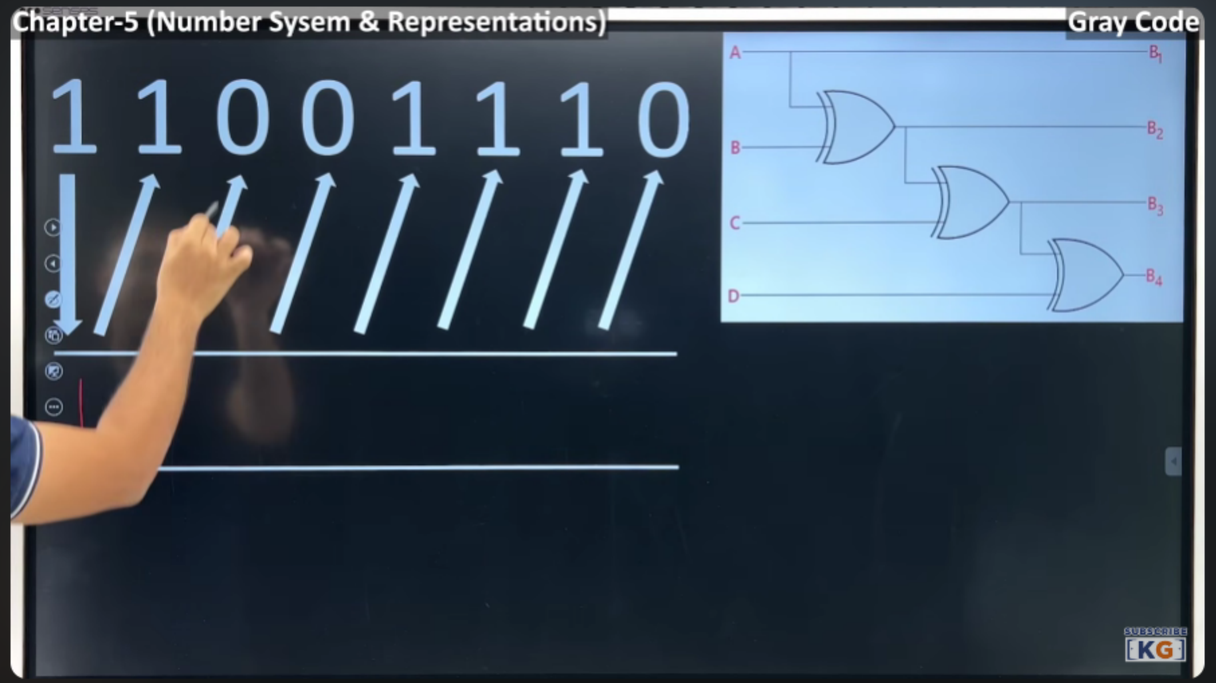

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1	1	0	0	1	0	1	0
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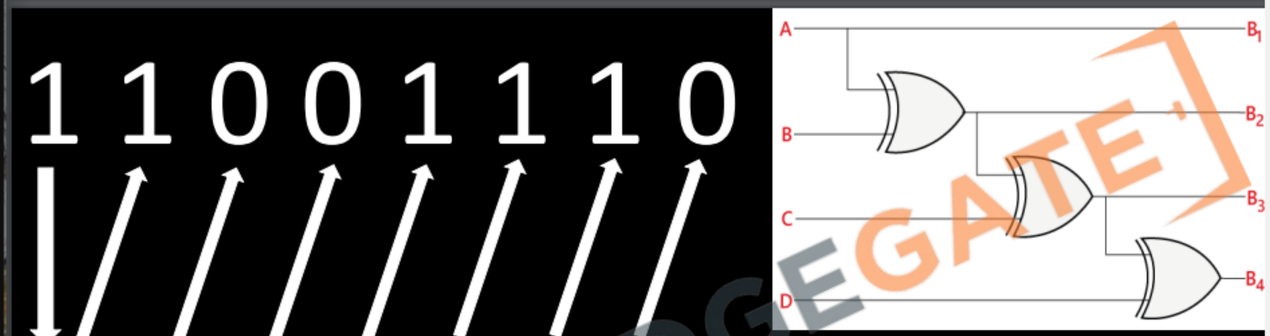

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- $B_0 = B_1 \oplus G_0$
- $B_1 = B_2 \oplus G_1$

G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0

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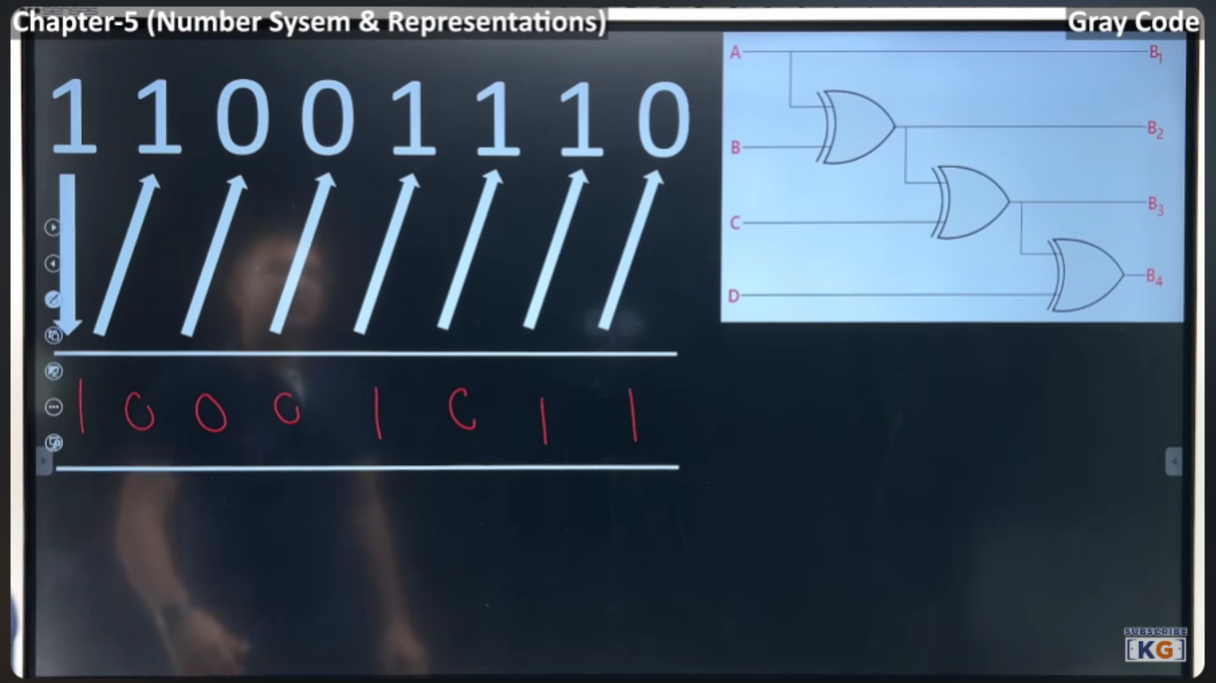

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1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
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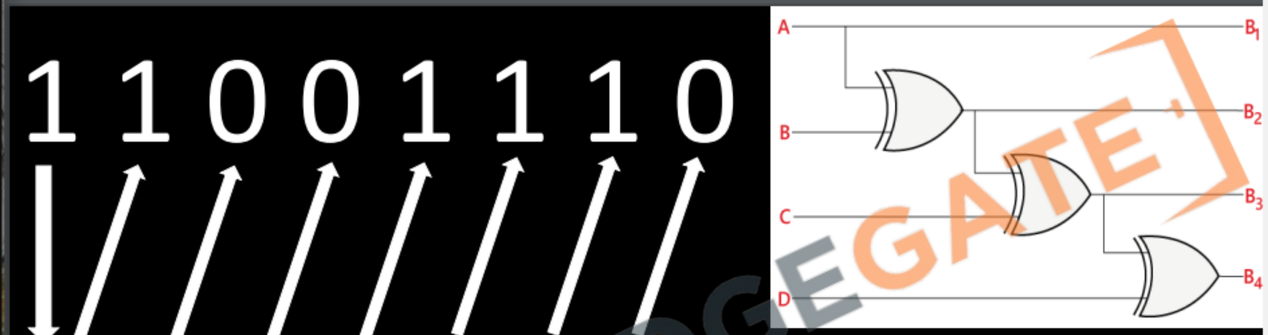

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- $B_0 = B_1 \oplus G_0$
- $B_1 = B_2 \oplus G_1$

G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0

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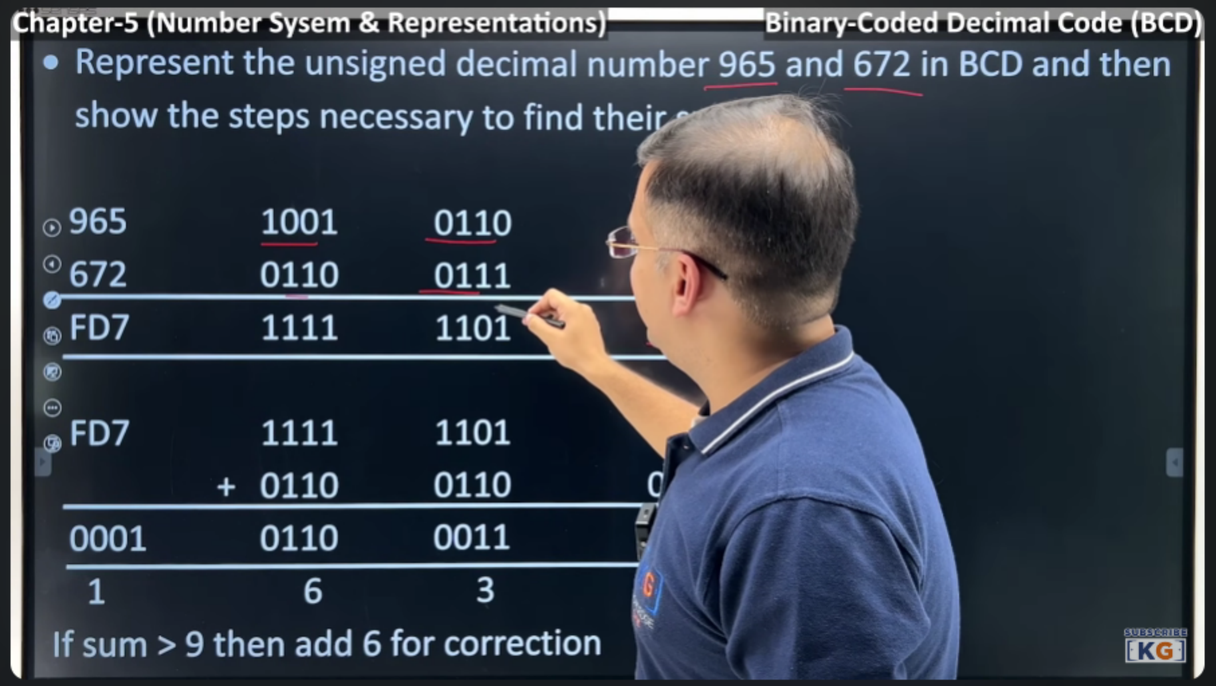

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11	1	0	1	1	0	0	0	1	0	0	0	1
12	1	1	0	0	0	0	0	1	0	0	1	0
13	1	1	0	1	0	0	0	1	0	0	1	1
14	1	1	1	0	0	0	0	1	0	1	0	0
15	1	1	1	1	0	0	0	1	0	1	0	1

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- Represent the unsigned decimal number 965 and 672 in BCD and then show the steps necessary to find their sum?

965	1001	0110	0101
672	0110	0111	0010
FD7	1111	1101	0111
FD7	1111	1101	0111
	+ 0110	0110	0000
0001	0110	0011	0111
1	6	3	7

If sum > 9 then add 6 for correction

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Decimal	Binary Sum					BCD Sum				
	C'	S3'	S2'	S1'	S0'	C	S3	S2	S1	S0
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	1
2	0	0	0	1	0	0	0	0	1	0
3	0	0	0	1	1	0	0	0	1	1

$$C = C' + S'_3S'_2 + S'_3S'_1$$

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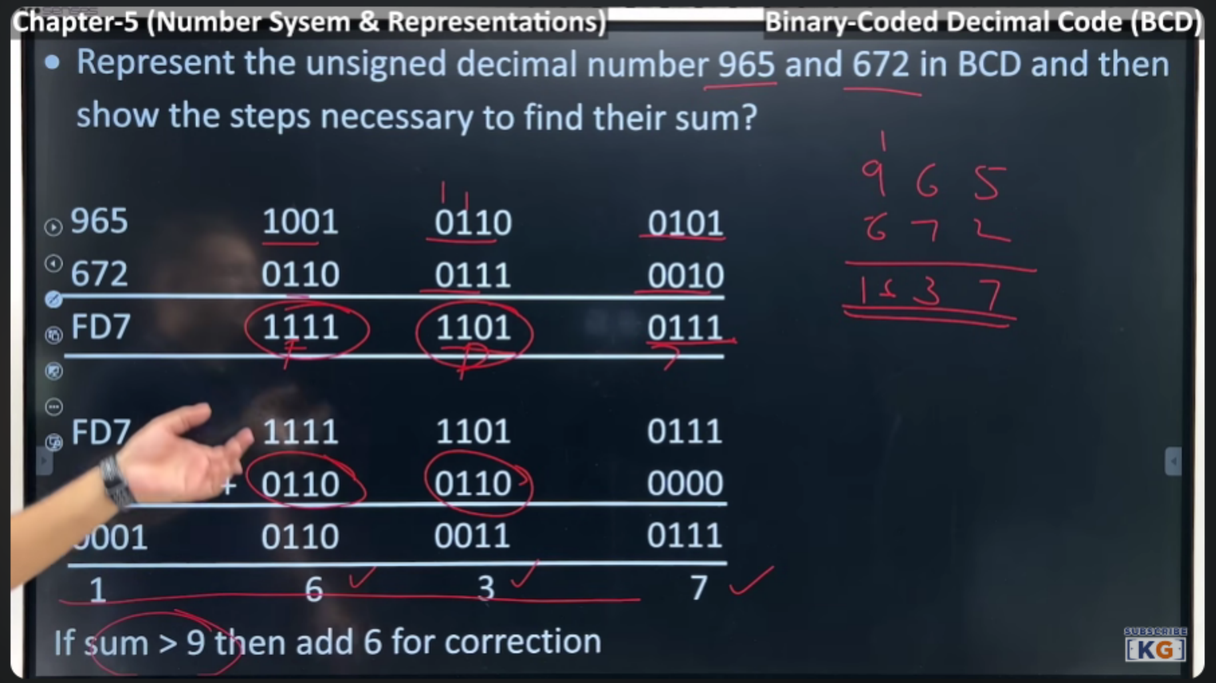

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Excess-3 Code

- Excess-3 Code is a binary-coded decimal (BCD) system that represents each digit of a decimal number by its corresponding 4-bit binary representation, but adds an offset of 3 to each digit. This makes arithmetic operations like addition and subtraction easier to implement.
- Excess-3 Code is primarily used in older computer systems and some types of calculators. It was important for minimizing hardware in early digital systems, where computational resources were limited.
- The main contribution of Excess-3 Code is that it simplifies the hardware required for arithmetic operations. Its self-complementing feature helps in carrying out subtraction by addition, thereby reducing computational complexity.

Decimal	Excess-3
0	0011
1	0100
2	0101
3	0110
4	0111
5	1000
6	1001
7	1010
8	1011
9	1100

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- Example: 395 in decimal will be represented in excess-3 code as:

  0110 1100 1000.

  3 9 5

- 3 in excess-3 representation is: 3 + 3 = 6 (0110)
- 9 in excess-3 representation is: 9 + 3 = 12 (1100)
- 5 in excess-3 representation is: 5 + 3 = 8 (1000)

- First, convert the decimal digits to their 4-bit Excess-3 codes:
  - 5 in Excess-3: 5 + 3 = 8 in decimal, which is 1000 in binary.

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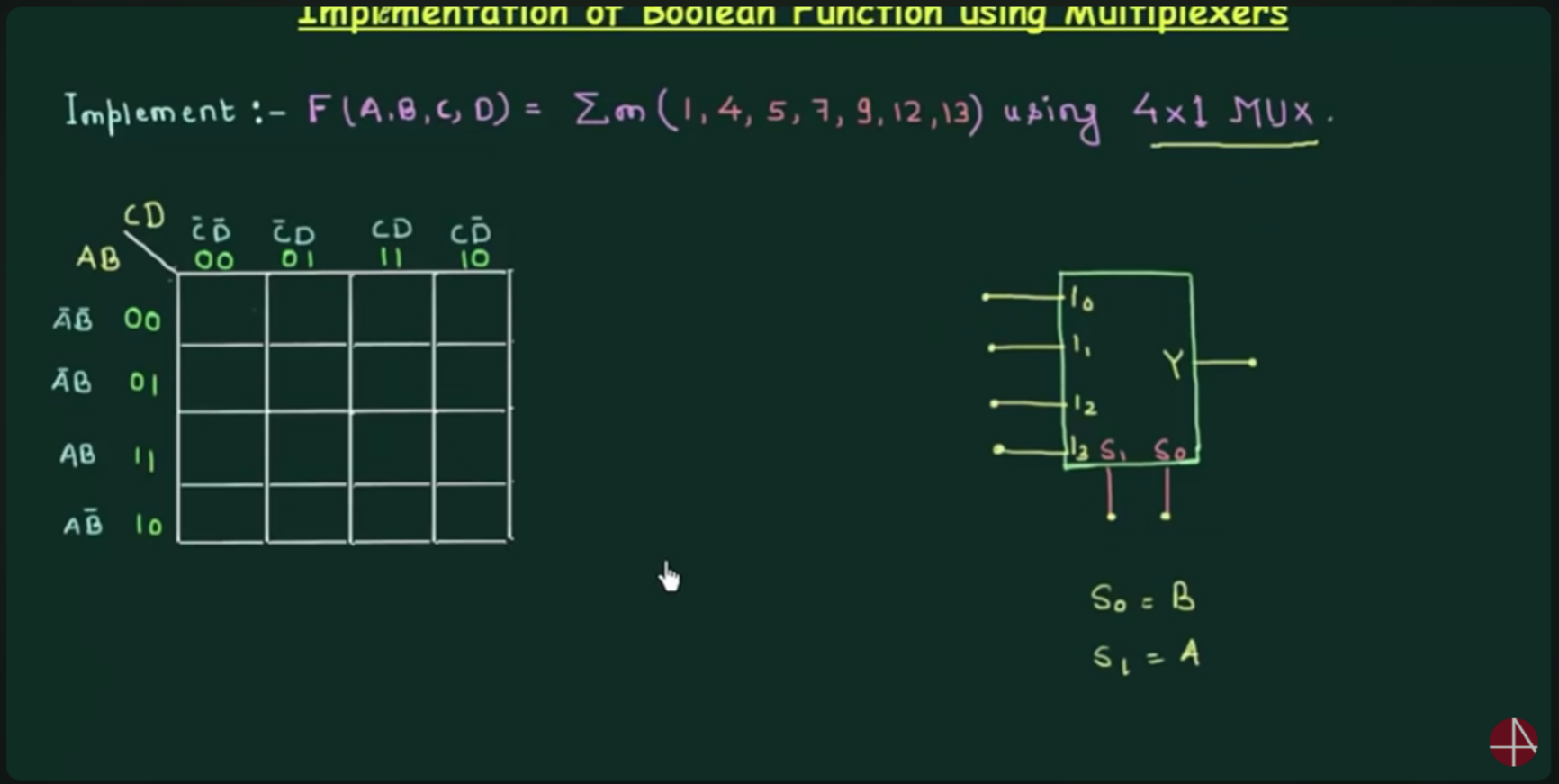

Implementation of Boolean Function using Multiplexers

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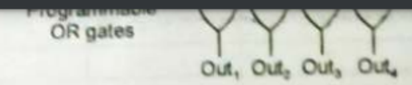
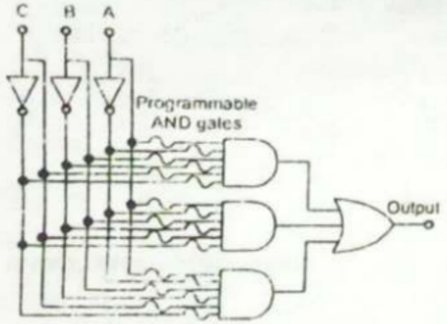
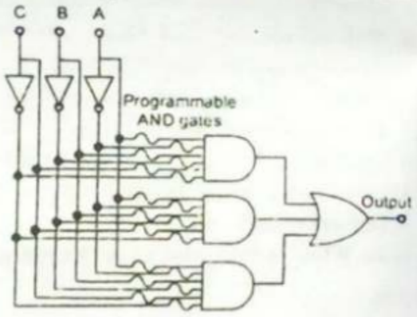
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	not used



Structure of (an unprogrammed) PLA circuit

PLA	PAL
Both AND and OR arrays are programmable.	OR array is fixed and AND array is programmable.
Costliest and more complex than PALs and PROMs.	Cheaper and simpler.
AND array can be programmed to get desired minterms.	AND array can be programmed to get desired minterms.
Any Boolean function in SOP from van be implemented using PLA.	Any Boolean function in SOP from can be implemented using PAL.





PAL circuits (Programmable Array Logic)

Q.26. Design a Delay Flip-Flop using S-R flip flop.

Ans. Step1. Given flip flop is RS flip flop

Required flip flop is D flip flop

Excitation table of RS flip flop

Present state	Next state	Flip flop inputs	
Q_n	Q_{n+1}	R	S
0	0	X	0
0	1	0	1
1	0	1	0
1	1	0	X

Step 3: Conversion table

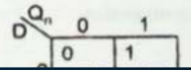
Compute the flip flop inputs by using excitation table of RS flip flop

Required flip flop			Given flip flop	
Flip flop input	Present state	Next state	Flip flop inputs	
D	Q_n	Q_{n+1}	R	S
0	0	0	X	0
0	1	0	1	0
1	0	1	0	1
1	1	1	0	X

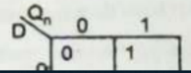
Step 4: K-map simplification

The required flip flop inputs and present state are considered for K-map simplification.

Expression for *R*



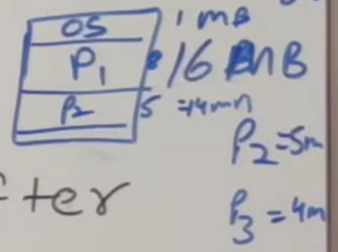
Expression for *S*



Memory Management in O.S

⇒ Memory Management is a form of resource management applied to Computer memory.

⇒ The essential requirement of memory management is to provide the ways to dynamically portions of memory to programs at their request, and free it for reuse when no longer needed.



Why memory management is Required?

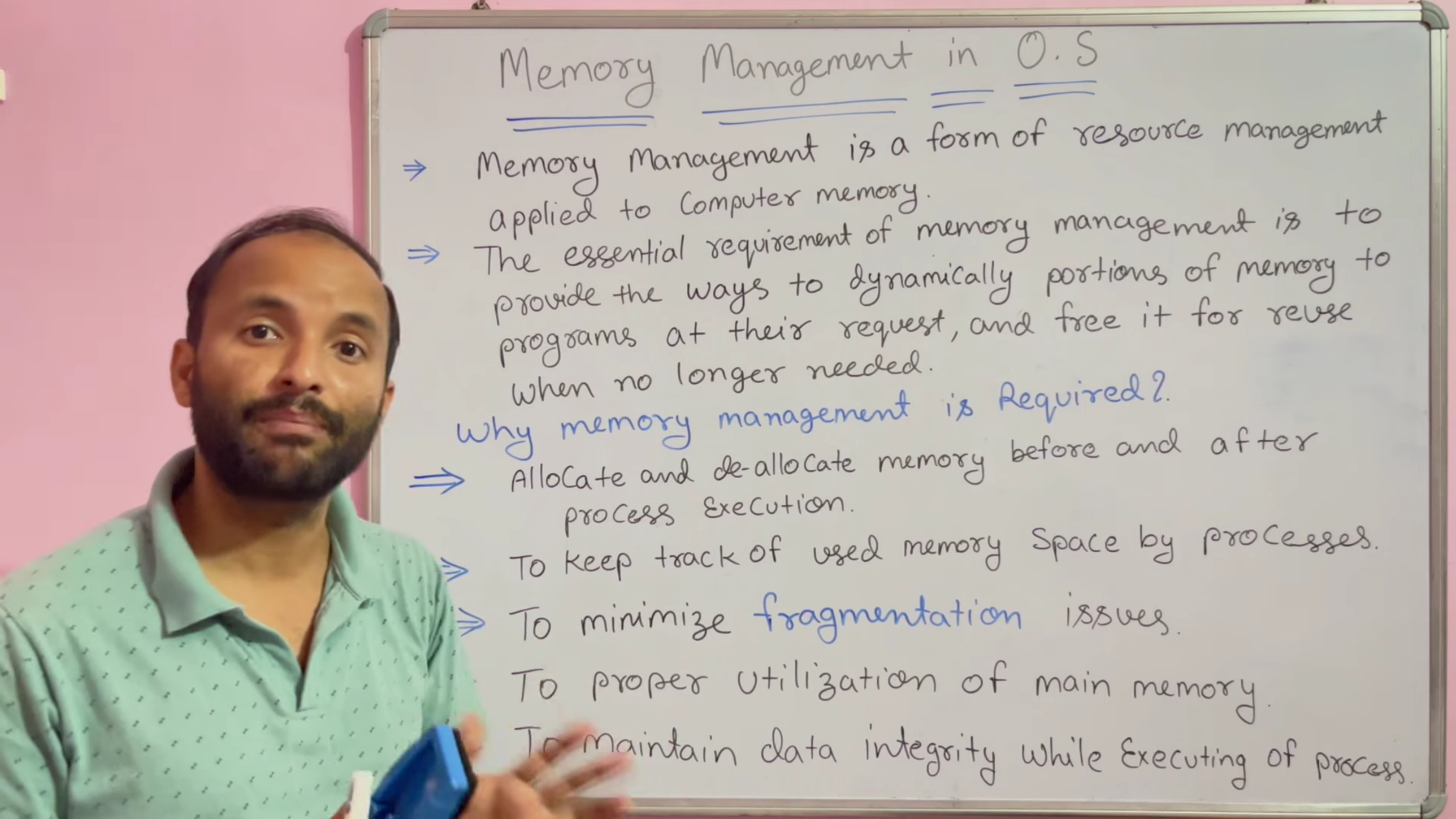
⇒ Allocate and de-allocate memory before and after process Execution.

⇒ [illegible] track of used memory Space by processes.

⇒ To [illegible] e fragmentation issues.

⇒ T[illegible] per utilization of main memory.

⇒ [illegible] maintain data integrity while Executing of process.


Memory Management in O.S
⇒ Memory Management is a form of resource management applied to Computer memory.
⇒ The essential requirement of memory management is to provide the ways to dynamically portions of memory to programs at their request, and free it for reuse when no longer needed.
Why memory management is Required?
⇒ Allocate and de-allocate memory before and after process Execution.
⇒ To keep track of used memory Space by processes.
⇒ To minimize fragmentation issues.
To proper utilization of main memory.
To maintain data integrity while Executing of process.

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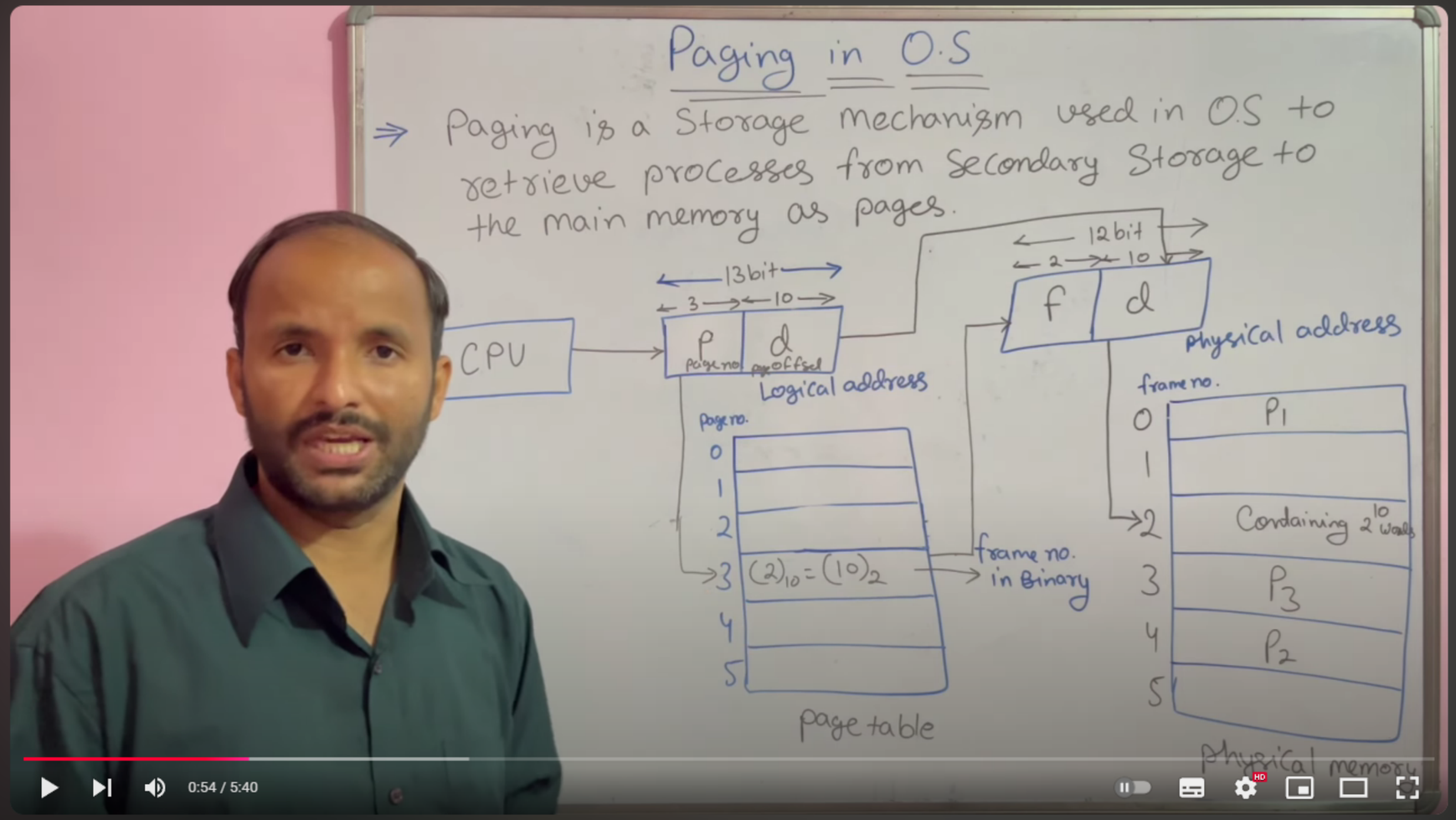

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	(RAM)	
Data-Retention	RAM is a volatile memory that could store the data as long as the power is supplied.	ROM is a non-volatile memory that the could retain the data even when the power is turned off.
Read/Write	Read and write operations are supported.	Only read operations are supported.
Use	Used to store the data that has to be currently processed by CPU temporarily.	It is typically used to store firmware or microcode, which is used to initialize and control hardware components of the computer.
Speed	It is a high-speed memory.	It is much slower than the RAM.
CPU Interaction	CPU can easily access data stored in RAM.	CPU cannot easily access data stored in ROM.
Size and Capacity	Large size with higher capacity, concerning ROM.	Small size with less capacity, concerning RAM.
Used as/in	CPU Cache , Primary memory.	Firmware, Micro-controllers.
Accessibility	The data stored is easily accessible.	The data stored is not as easily accessible as in the concerning RAM.

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