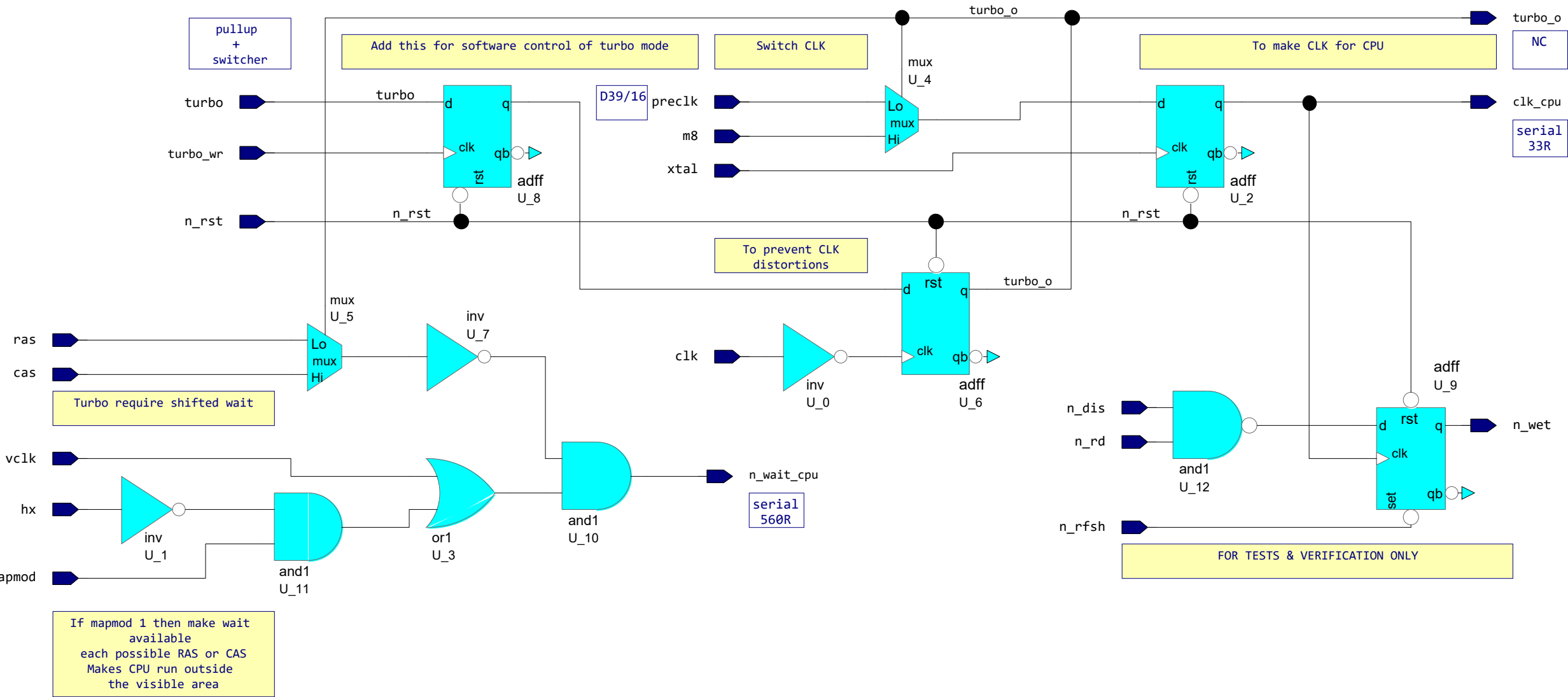


Compiler Directives  
Pre-module directives:  
`resetall  
`timescale 1ns/10ps  
Post-module directives:  
End-module directives:



Declarations  
Ports:  
wire cas;  
wire clk;  
wire hx;  
wire m8;  
wire mapmod;  
wire n\_dis;  
wire n\_rd;  
wire n\_rfst;  
wire n\_rst;  
wire preclk;  
wire ras;  
wire turbo;  
wire turbo\_wr;  
wire vclk;  
wire xtal;  
wire clk\_cpu;  
wire n\_wait\_cpu;  
wire n\_wet;  
wire turbo\_o;  
Diagram Signals:  
wire din;  
wire dout;  
wire dout1;  
wire dout2;  
wire dout3;  
wire dout4;  
wire dout5;  
wire dout6;  
wire q;

Aleste Team		Project:	AlesteOrig		VAP	VVT	VMB
Title:	Turbo Mode Board Design		Turbo mode extension for original Aleste 520ex				AVM
Path:	AlesteOrig_lib/turbo/struct				SAP		
Edited:	by valery on 11 Nov 2017					VPB	