Compiler Directives Pre-module directives: `resetall

`timescale 1ns/10ps Post-module directives: End-module directives:

U_11

If mapmod 1 then make wait available

each ppossible RAS or CAS Makes CPU run outside the visible area

Add this for software control of turbo mode **Declarations** Ports: wire cas; wire clk; wire hx; turbo_o wire m8;
wire mapmod; adff adff Switch CLK To make CLK for CPU wire n_dis; wire n_rd; wire n_rfsh; turbo preclk clk_cpu turbo wire n_rst; wire preclk; wire ras; turbo_wr wire turbo; wire turbo wr; xtal mux wire vclk; wire xtal; U_4 wire clk cpu;
wire n_wait_cpu;
wire n_wet;
wire turbo_o; n_rst n_rst n_rst Diagram Signals:
wire din;
wire dout; turbo_o wire dout1; wire dout2; wire dout3; ras wire dout4;
wire dout5; n_rst FOR TESTS ONLY adff cas wire dout6; adff U_9 wire q; Turbo require shifted wait U_0 U_6 U_7 n_dis mux n_wet U_5 To prevent CLK distortions clk_cpu FOR TESTS ONLY vclk vclk and1 n_wait_cpu U_12 and1 or1 U_10 U_3 U_1 and1 n_rfsh mapmod

| Aleste Team | | Project: | AlesteOrig |
|-------------|-----------------------------|--|------------|
| | | Turbo mode extension for original Aleste 520ex | |
| Title: | Turbo Mode Board Design | | 3 |
| Path: | AlesteOrig_lib/turbo/struct |] | |
| Edited: | by valery on 10 Nov 2017 | 1 | |