Declarations
Ports:
```
wire cas;
wire clk;
wire hx;
wire m8;
wire n_rst;
wire preclk;
wire ras;
wire turbo;
wire vclk;
wire xtal;
wire clk_cpu;
wire n_wait_cpu;
wire turbo_o;
```
Diagram Signals:
```
wire dout;
wire dout1;
wire dout2;
wire dout3;
wire dout4;
wire dout5;
wire dout6;
wire dout7;
wire ena;
wire sel;
```
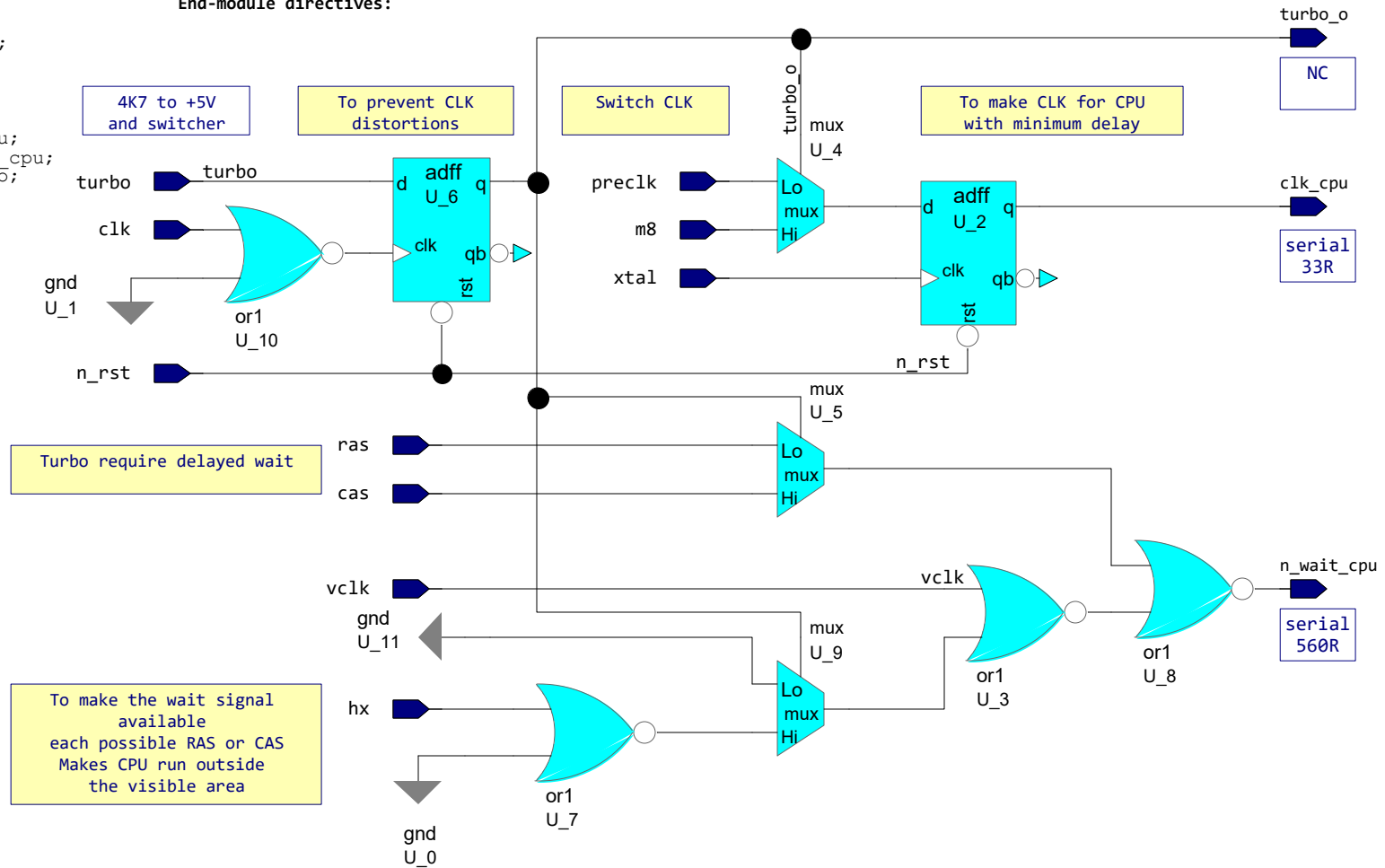
Compiler Directives
Pre-module directives:
`resetall
`timescale 1ns/10ps
Post-module directives:
End-module directives:

turbo_o

NC

4K7 to +5V
and switcher

To prevent CLK
distortions

Switch CLK

To make CLK for CPU
with minimum delay

turbo   turbo

clk

gnd
U_1

or1
U_10

n_rst

Turbo require delayed wait

To make the wait signal
available
each possible RAS or CAS
Makes CPU run outside
the visible area

mux
U_4

d   adff
     U_6
        q

clk   qb

        rst

preclk

m8

xtal

Lo
mux
Hi

d   adff
     U_2
        q

clk   qb

        rst

clk_cpu

serial
33R

mux
U_5

ras

cas

Lo
mux
Hi

n_rst

mux
U_9

vclk

gnd
U_11

hx

Lo
mux
Hi

or1
U_7

gnd
U_0

vclk

or1
U_3

or1
U_8

n_wait_cpu

serial
560R

Aleste Team	Project:	AlesteOrig	VAP	VVT	VMB
	Simple version. Use switcher with pullup resistor to enable or disable turbo mode.				
Title:	Turbo Mode Board Design (Simple)				
Path:	AlesteOrig_lib/turbo_simple/struct		SAP		AVM
Edited:	by valery on 11 Nov 2017				VPB