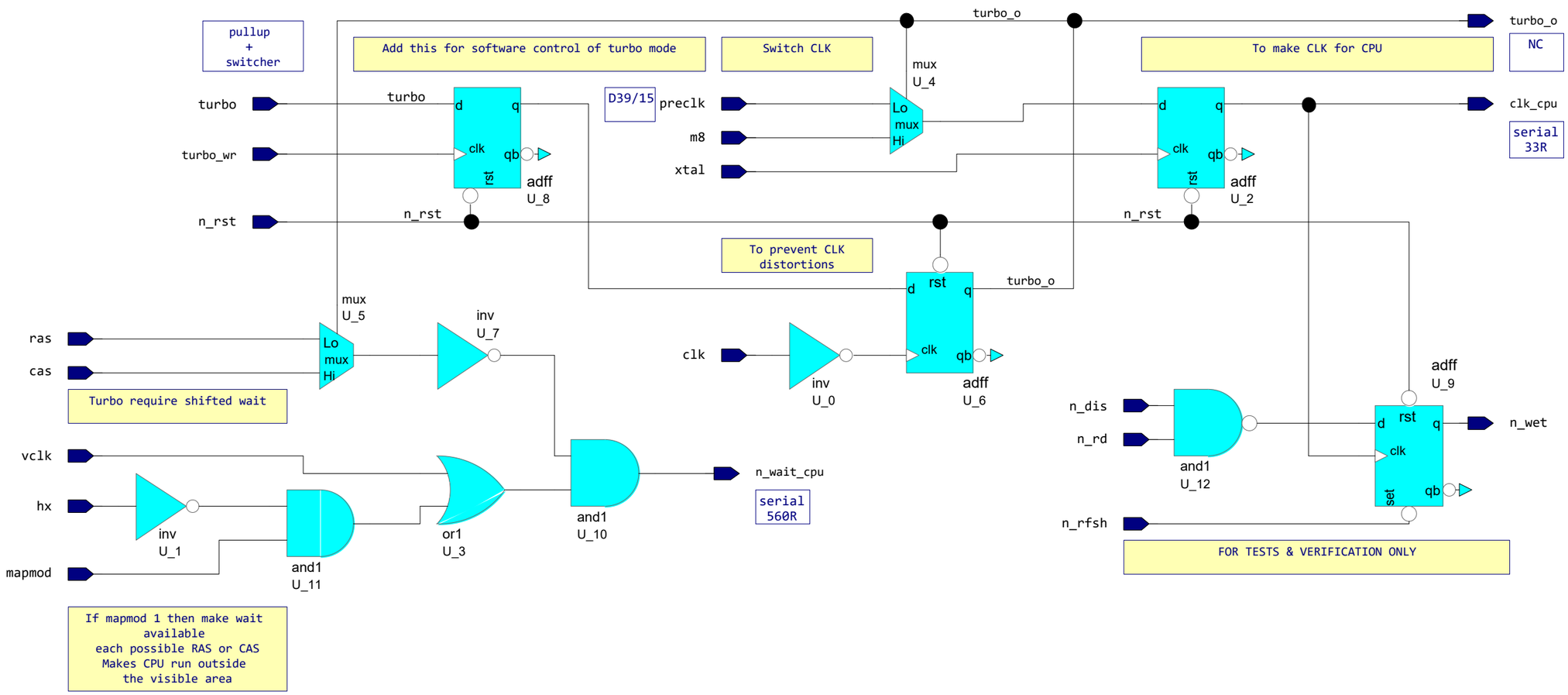
Compiler Directives
Pre-module directives:
`resetall
`timescale 1ns/10ps
Post-module directives:
End-module directives:



Declarations
Ports:

```
wire cas;
wire clk;
wire hx;
wire m8;
wire mapmod;
wire n_dis;
wire n_rd;
wire n_rfsh;
wire n_rst;
wire preclk;
wire ras;
wire turbo;
wire turbo_wr;
wire vclk;
wire xtal;
wire clk_cpu;
wire n_wait_cpu;
wire n_wet;
wire turbo_o;
```

Diagram Signals:

```
wire din;
wire dout;
wire dout1;
wire dout2;
wire dout3;
wire dout4;
wire dout5;
wire dout6;
wire q;
```

Aleste Team		Project: AlesteOrig	VAP	VVT	VMB
		Turbo mode extension for original Aleste 520ex			AVM
Title:	Turbo Mode Board Design		SAP		
Path:	AlesteOrig_lib/turbo/struct				VPB
Edited:	by valery on 11 Nov 2017				