Architecture: DE10-Lite/MAX10 based RL Emulator

USER interface + LEDs

RAM

MICRO SD-card

Serial I/O Debug console

WLAN

NIOS II CPU

Interface , RL I/O bus , 12 differential signals

Command Sequencer

PORT #2

**Dual Ported RAM(DPR)
5760 words = 1 RL track**

PORT #1

MFM DECODER

Data-Sequencer
+
Clock Manager
+
Sector-Puls-generator

MFM ENCODER