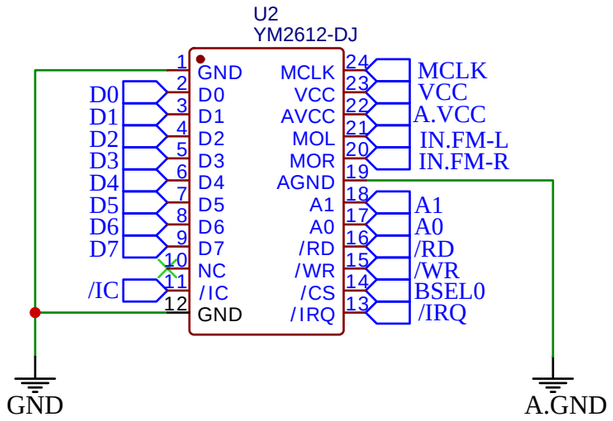

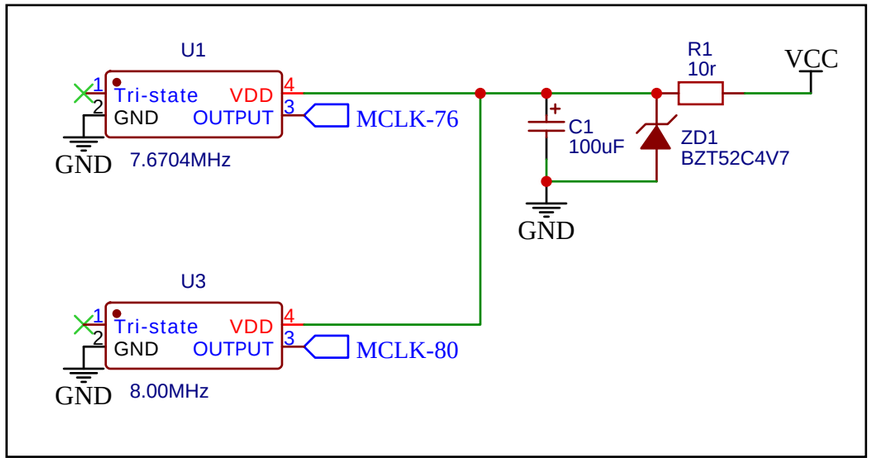

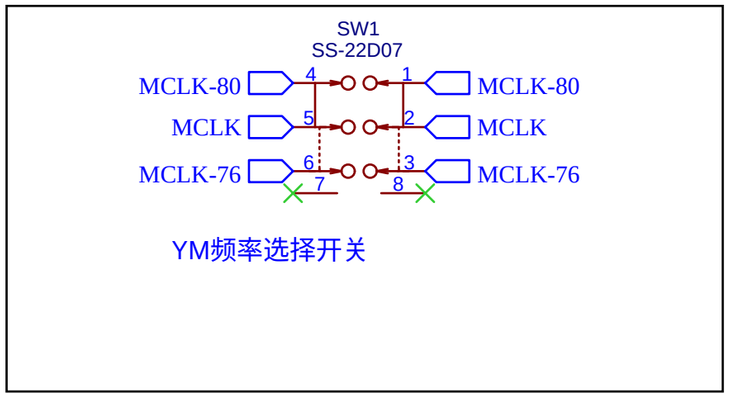

2024.8.13

1.使用旧版本混音电路，已成功

2.单晶振拔插座，因为DCSG时钟不引入Mod

3.取消一切累赘电容

2024.8.18

1.删除BSEL切换开关，默认BSEL0是FM

2.增加贴片晶振

3.优化布局

2024.8.18

1.针对 RE2e总线，增加SN片选开关

2.SN片选固定为b1或b3

3.增大YM3438音量

2024.9.21

1.单OPN2设计

2024.10.29

1.晶振供电降压

2.恢复IRQ

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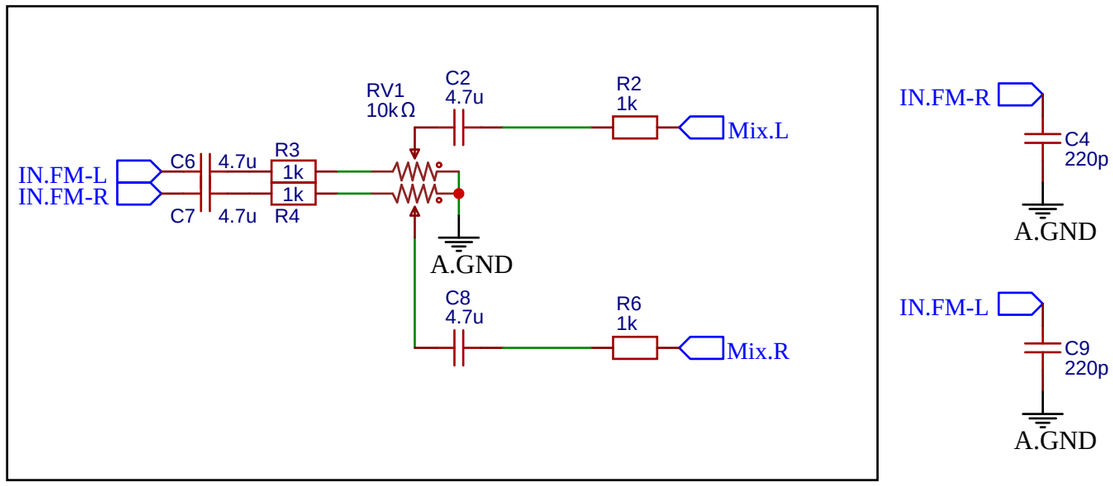
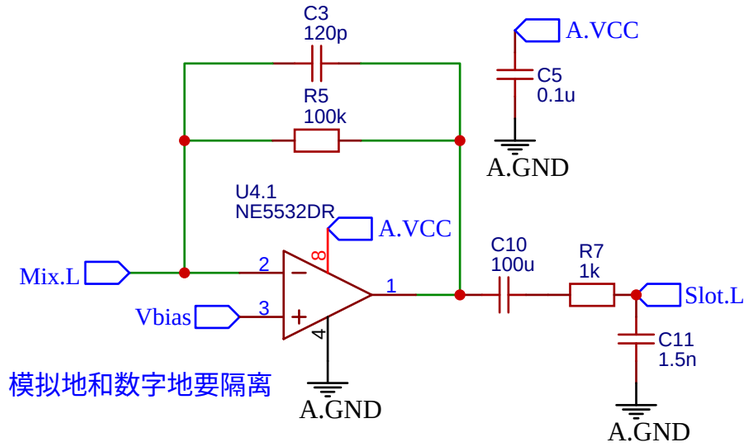
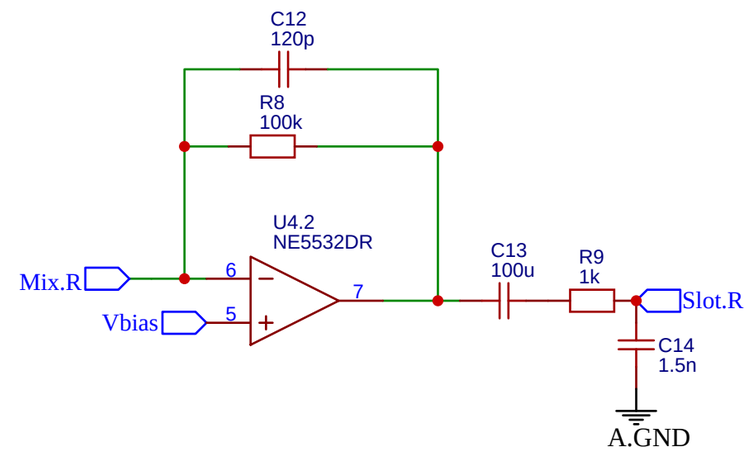
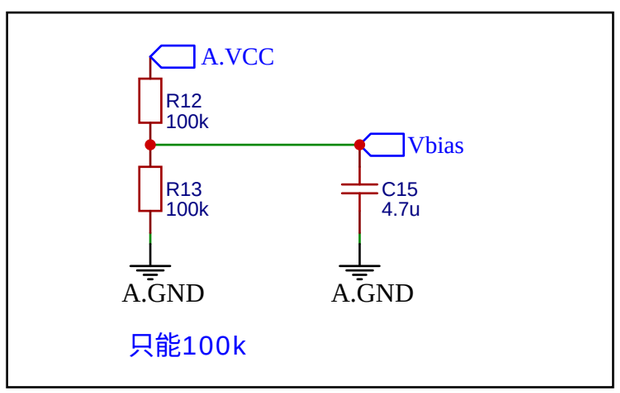


输入模式可能要改小电阻

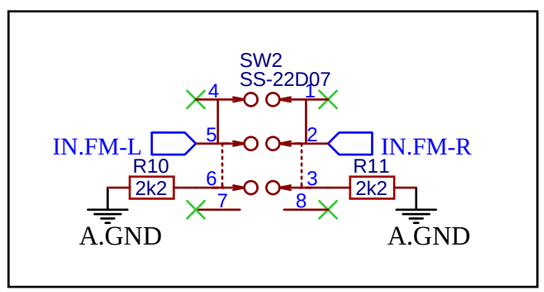


模拟地和数字地要隔离





只能100k



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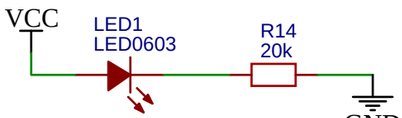

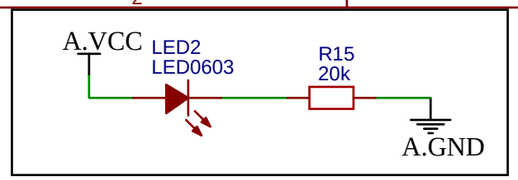

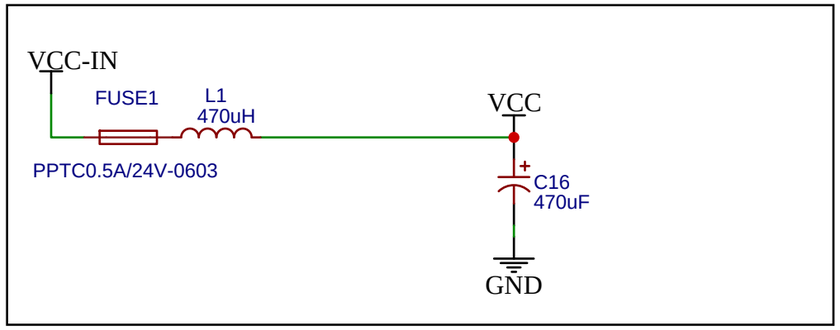

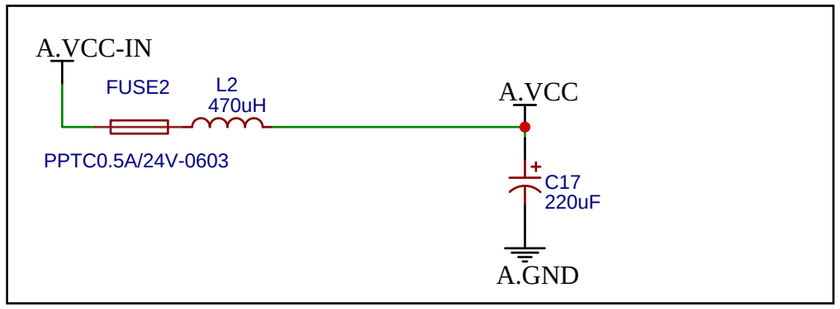

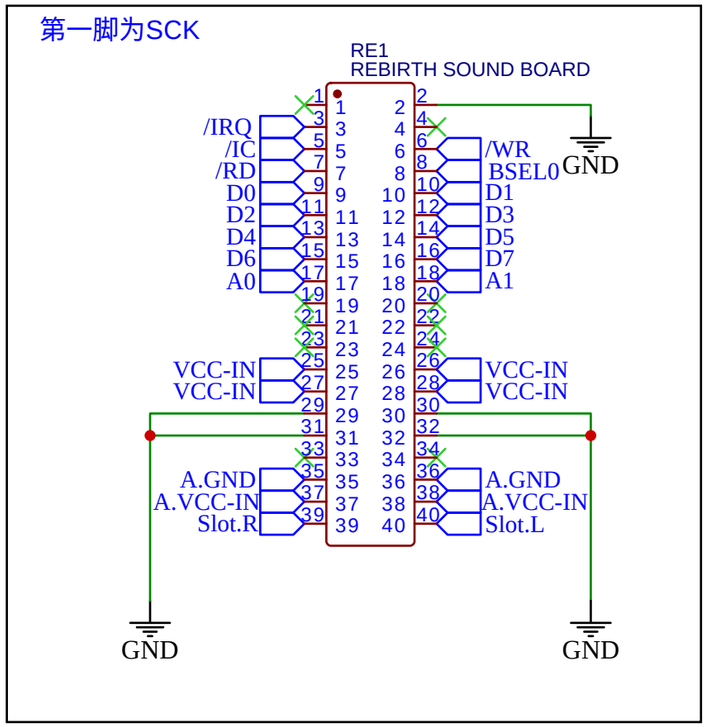

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