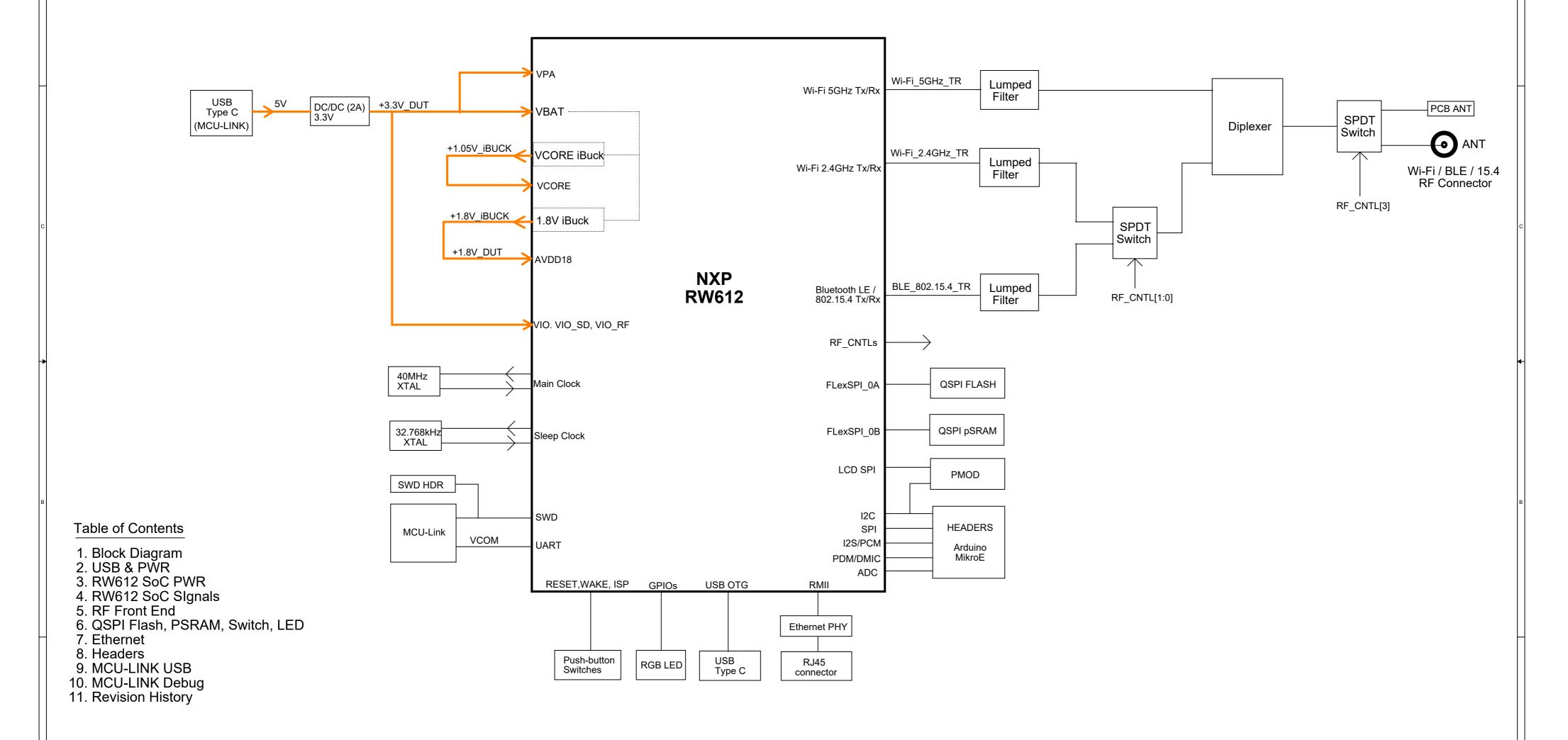
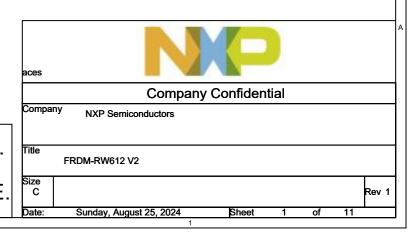
# NXP SEMICONDUCTORS COMPANY CONFIDENTIAL

# **Block Diagram**



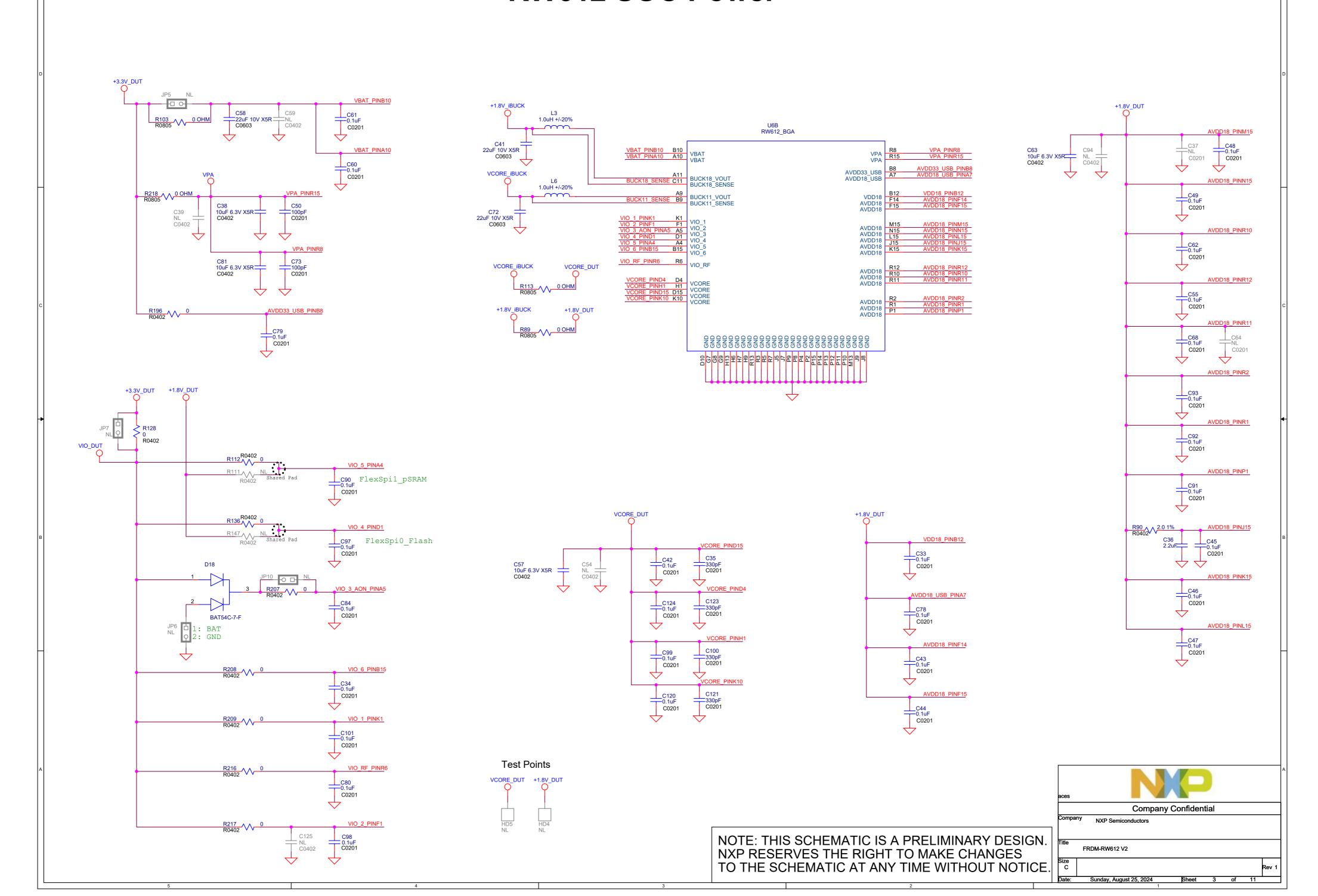
# FRDM-RW612

Wireless MCU with Integrated Tri-radio Wi-Fi 6 + Bluetooth Low Energy 5.4 / 802.15.4 (RW612)



#### **POWER 3.3V DC-DC POWER LED** U8 MP1605GTF 5V\_USB\_MCU\_LINK 5V\_HDR\_IN C105 = 22uF 10V X5R = C0805 R126 200K 1% = R0402 C82 NL C0402 C0805 R125 100k R0402 MSS1P3L MHT192DGCT R114 44.2k 1% R0402 Vout = 0.6 (1 + R1/R2)3.315 V = 0.6 (1 + 200 K / 44.2 K)**USB\_OTG HIGH SPEED USB2.0 Type C** VBUS Control USB\_OTG\_VBUS\_5V 5V\_USB\_OTG C115 4.7uF 10V X5R R171 NL R0402 330 OHM +/-25% 10uF 10V X5R 0.22uF 10V X5R USB4085-GF-A C0603 NX5P3090UK L9 DLW21SN900SQ2I C107 0.1uF C0402 R133 NL R0402 GPIO\_20\_USB\_OTG\_PWR\_FLT <<-VBUS4 90ohm differential pair GND4 Layout Note: GPIO\_12\_USB\_OTG\_PWR >> 900hms differential impedance RClamp0854P.TCT CC Logic Control **GND Test Points** Mounting Holes USB\_OTG\_VBUS\_5V C111 0.22uF 10V X5R C0402 R155 R149 R154 0.22uF 10V X5R C0402 R0402 R0402 R0402 Fiducials U10 R143 R167 R142 R164 10k NL R0402 R0402 R0402 R0402 PTN5150A SHIELD FD6 FD4 FD1 FD3 FD5 FD2 SDA/OUT1 VBUS\_DET R144 \ 0 R0402 \>> USB\_ID [5,6] SCL/OUT2 INTB/OUT3 ADR/CON DET EXT\_SEL PORT D10 PESD5V0F1BL 👗 PESD5V0F1BL R166 > NL R0402 Layout Note: R0402 Place TVS and resistors close to USB connector ADR/CON\_DET: When Power-up, ADR(input) function: ADR=1: I2C Address: 0x7A(ADR) ADR=0: I2C Address: 0x3A(ADR) EXT\_SEL: External selection High = CC1 orientation or no valid CC1/CC2 detection Company Confidential Low = CC2 orientation ADR=MID/FLOATING:(Pin 6/7/8) configured as OUT1/2/3 in non-I2C mode NXP Semiconductors After TINPUTLATCH, CON\_DET(output) function: NOTE: THIS SCHEMATIC IS A PRELIMINARY CON\_DET=1: Connection Detected CON\_DET=0: No Connection DESIGN. NXP RESERVES THE RIGHT TO FRDM-RW612 V2 MAKE CHANGESTO THE SCHEMATIC AT ANY TIME WITHOUT NOTICE. Sunday, August 25, 2024

# **RW612 SOC Power**



#### **RW612 SOC Signals** GPIO\_1\_LED\_RED ( SJ3 1 2 GPIO\_1 SJ4 1 2 GPIO\_1\_ME\_PWM << GPIO 2 FC0 I2S DATA ((SJ5 1) 2 (GPIO\_2 GPIO\_2\_FC0\_UART\_RXD\_ME (\( \lefta \) SJ6 1 2 **STRAP CONFIG** 5V\_USB\_OTG U6A RW612\_BGA GPIO\_3\_FCO\_I2S\_WS R192 4.7k R0402 CON[11] GPIO\_3\_FCO\_UART\_TXD\_ME (\( \sigma \sum \text{SJ8} 1 \sigma \text{2} \) USB DM GPIO[0 N2 GPIO[0] F10 GPIO[1] C13 GPIO[2] F8 GPIO[3] L7 GPIO[5] USB\_DP USB\_ID +3.3V\_BRD R219 NL R0402 GPIO\_3 GPIO\_4\_FC0\_I2S\_SCK GPIO\_5\_MCLK GPIO\_6\_FC1\_SPI\_SSELN0 GPIO\_7 USB\_VBUS GPIO\_7\_FC1\_SPI\_SCK (\( \) SJ9 1 \( \) 2 (\( \) GPIO 7 **−**>>> GPIO\_12 GPIO[4] GPIO[5] GPIO[12] RF\_CNTL\_0 GPIO\_7\_FC1\_I2S\_SCK GPIO[7] GPIO[8] GPIO[9] GPIO[10 GPIOÎ17 GPIO\_10\_FC1\_SPI\_SSELN1 GPIO\_11\_ARD\_D2 GPIO[18] GPI0[11 GPIO\_8\_FC1\_SPI\_MISO GPIO\_13\_SWCLK SPIO\_14\_SWDIO GPI0[14] ->> GPIO\_28\_QSPI\_flash\_SSEL0 ->> GPIO\_29\_QSPI\_flash\_DQS ->> GPIO\_30\_QSPI\_flash\_D0 GPIO[28] GPIO\_21\_ENET\_RST << GPIO[29] GPIO[30] GPIO\_22 GPIO\_23 GPIO\_24 GPIOÎ22 GPI0[23 +1.8V\_DUT +3.3V\_BRD SJ13 GPIOI24 GPIO[32] GPI0[25 GPI0[33] GPIO\_8\_FC1\_UART\_TXD\_ARD\_D1 <<----C5 GPIO[26] GPIO[27] SPIO\_34\_QSPI\_flash\_CLK0 GPIO\_27\_ARD\_D5 R86 GPIOI35 G13 H12 J11 H10 F12 GPIO[42] GPIO[44] GPIO[44] GPIO[46] GPIO\_42\_ARD\_A0 GPIO\_43\_ARD\_A1 GPIO\_44\_LCD\_SPI\_RESETN GPIO\_45\_ARD\_A2 GPIO\_46\_LCD\_SPI\_SDIO GPIO\_39\_GSPI\_SRAM\_CLR\(0) GPIO\_36\_QSPI\_SRAM\_SSL0 GPIO\_37\_QSPI\_SRAM\_DQS GPIO\_38\_QSPI\_SRAM\_D0 GPIO\_39\_QSPI\_SRAM\_D1 GPIO\_40\_QSPI\_SRAM\_D2 VCC GPI0[36] GPIO[37] GPIO[38] GPIO\_9\_FC1\_SPI\_MOSI (\(\sigma \) SJ14 1 \(\sigma \) 2 E13 GPIO[45] D13 GPIO[47] GPIO\_9\_FC1\_I2S\_DATA ( SJ15\_1 2 D14 GPIO[48 K12 GPIO[49 ->>SOC\_RF5G\_TR ->>SOC\_RF2G\_TR ->>SOC\_BLE\_15.4\_TR GPIO[51 GPIO[52 M10 GPIO[54] GPIO[54] GPIO[55] GPIO\_53\_PDM\_CLK01 GPIO\_54\_ME\_INT GPIO\_55\_ENET\_INT GPIO\_56 GPIO\_9\_FC1\_UART\_RXD\_ARD\_D0 <<---GPIO[55] GPIO[56] EXT\_REQ EXT\_GNT STRAP/CONFIG TABLE B13 GPIO[57 GPIO\_57 GPIO\_58 EXT\_FREQ/WCI-2\_SOUT D12 GPIO[58] E11 GPIO[59] **--**-**⟨**⟨GPIO\_8 A13 GPIO[60 B14 GPIO[61 RF CNTL0 **FUNCTION** GPIO\_61\_ADC1\_ME\_AN GPIO\_62\_ENET\_RX\_EN GPIO\_63\_ENET\_RX\_ER RF CNTL1 GPIO\_12\_LED\_GREEN ( SJ17 1 2 GPIO\_12 CONFIG\_DAP\_USE\_JTAG: RF\_CNTL2 E9 PDN 1 : DAP uses JTAG (default) [11] 0: DAP uses SWD ISENSE CLKOUT HD7 GND OUT CONFIG XOSC\_SEL: RF\_CNTL0 1: 40 MHz (Default) 0: 38.4 MHz 6.04k 1% R0201 [5] GPIO\_20\_ARD\_D7 ( SJ19\_1 2 CONFIG HOST BOOT[3:0] : EXT\_FREQ, EXT\_PRI, EXT\_GNT, EXT\_REQ GPIO\_20\_USB\_OTG\_PWR\_FLT (\( \left( \sum\_{SJ20} 1 \right) \) 2 **Reference Clock** [3:0] 40MHz XTAL CON[3:0] GPIO\_22\_ENET\_RX\_DATA0 <<----Boot from QSPI Flash (Default) 1110 ISP boot (UART/I2C/SPI/USB) Serial boot (UART/I2C/SPI/USB) ISP boot (SDIO) 32.7680kHz +/- 20ppm Serial boot (SDIO) GPIO\_23\_ENET\_RX\_DATA1 (\(\sigma \) SJ22 1 +3.3V\_BRD R134 NL R0402 MCU\_AONWAKEUP >>— GPIO\_16\_FC2\_I2C\_SDA\_ARD <<>>— R49 R66 4.7k 4.7k R0402 R0402 GPIO\_16\_FC2\_I2C\_SDA\_ME 〈〈〉〉 GPIO\_16\_FC2\_I2C\_SDA\_TEMPSN3〈〉〉 GPIO\_16\_FC2\_I2C\_SDA\_MLINK 〈〈〉〉 GPIO\_25\_ENET\_CLK \(\( \) R127 33 \( \) R0402 \( \) \(\( \) GPIO\_25 GPIO\_16\_FC2\_I2C\_SDA\_USBOTG\_CC **─⟨**GPIO\_16 GPIO\_17\_FC2\_I2C\_SCL\_ARD GPIO\_17\_FC2\_I2C\_SCL\_PMOV GPIO\_17\_FC2\_I2C\_SCL\_ME GPIO\_17\_FC2\_I2C\_SCL\_TEMPSNS GPIO\_17\_FC2\_I2C\_SCL\_MINK GPIO\_17\_FC2\_I2C\_SCL\_USBOTG\_CC GPIO\_52\_PDM\_DATA23 SJ23 1 2 GPIO\_52 TRGT RESETn >> PDn GPIO 56 ENET MDC ( R31 0 R0402 (GPIO\_56 TP9 GPIO\_14\_SWDIO TP10 GPIO\_13\_SWCLK **Company Confidential** Company NXP Semiconductors GPIO\_59\_ENET\_TX\_DATA1 NOTE: THIS SCHEMATIC IS A PRELIMINARY DESIGN. FRDM-RW612 V2 NXP RESERVES THE RIGHT TO MAKE CHANGES 33 ohm; keep closer to SOC TO THE SCHEMATIC AT ANY TIME WITHOUT NOTICE. Sunday, August 25, 2024

CON[2]

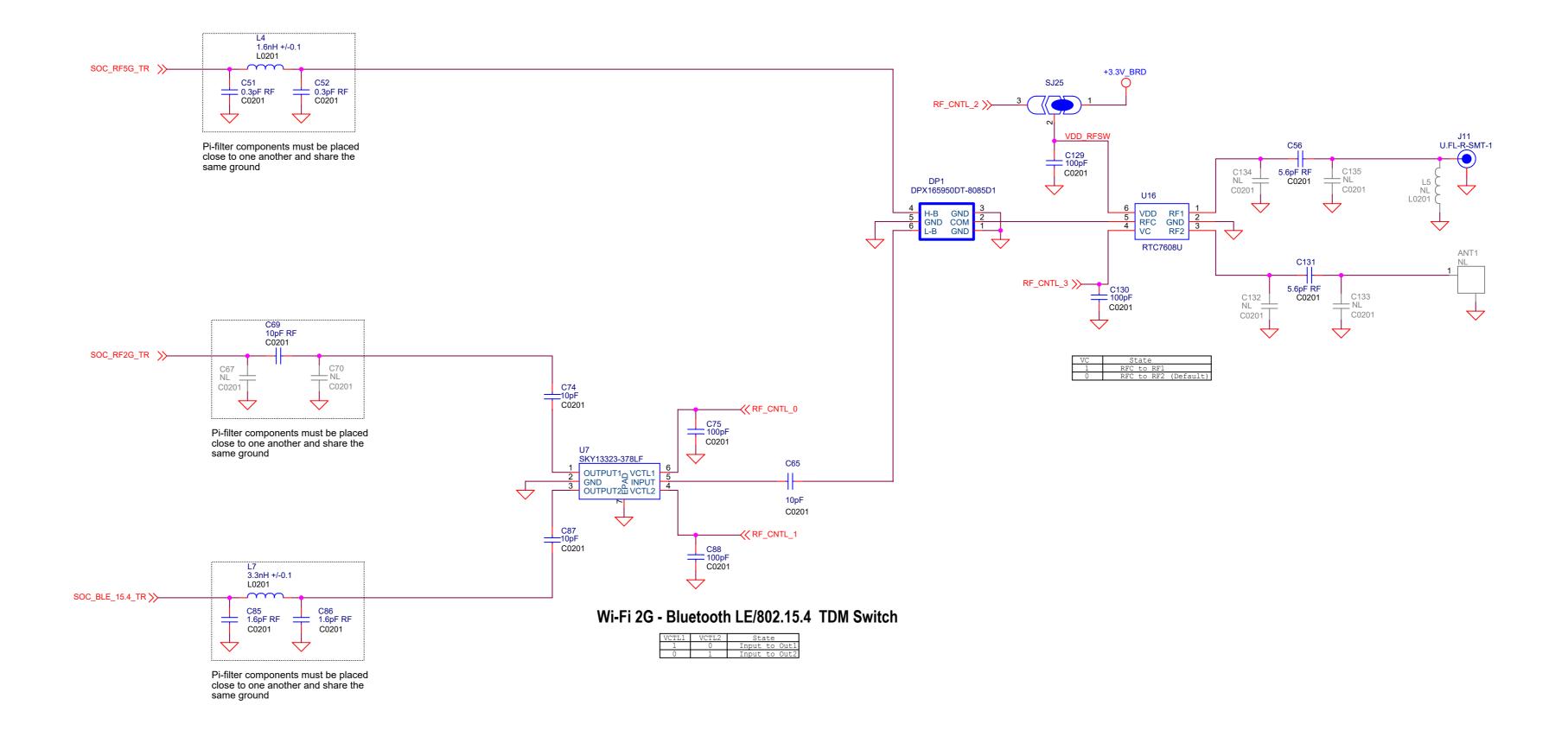
74LVC1G07GV,125

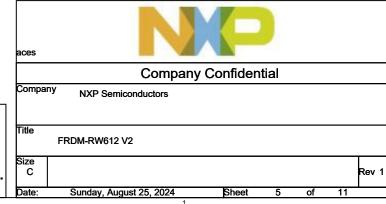
 $\triangle$ A

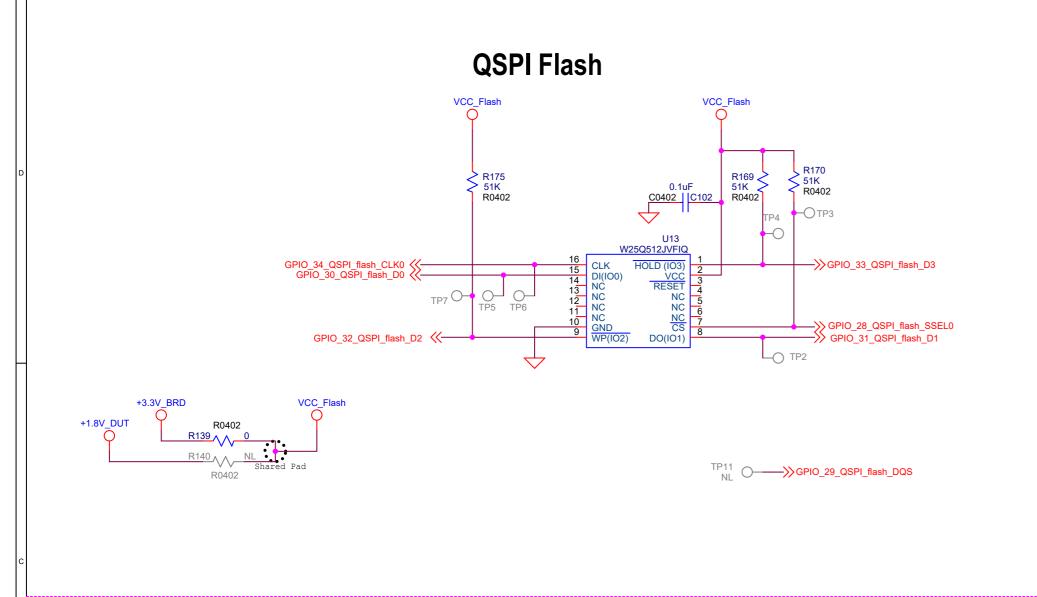
GND

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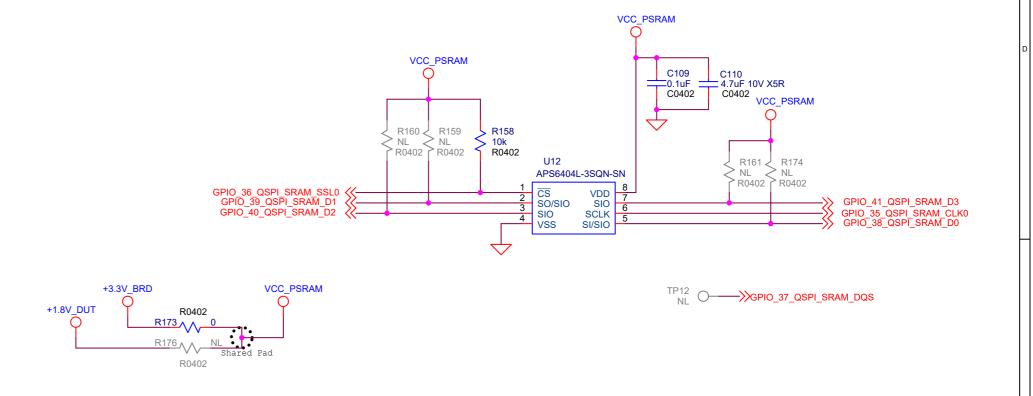
## **RF Front End**



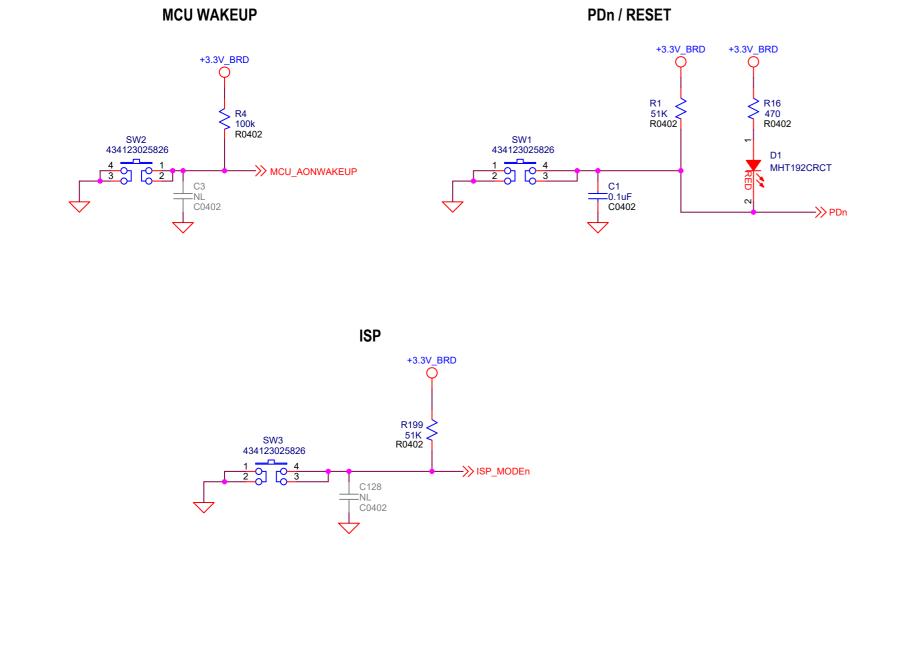




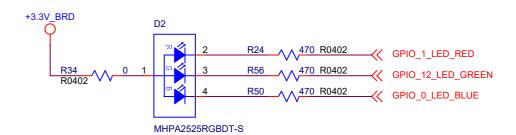
### **PSRAM**



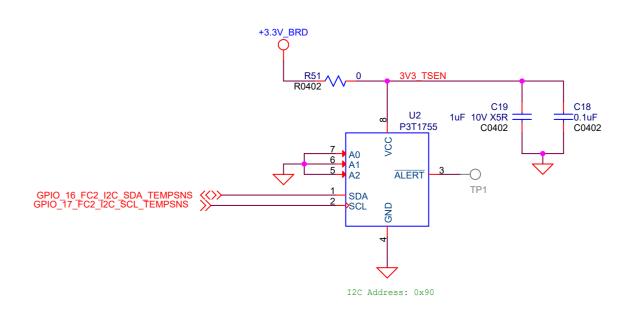
## **Push Buttons**



#### **RGB LED**



#### **TEMPERATURE SENSOR**



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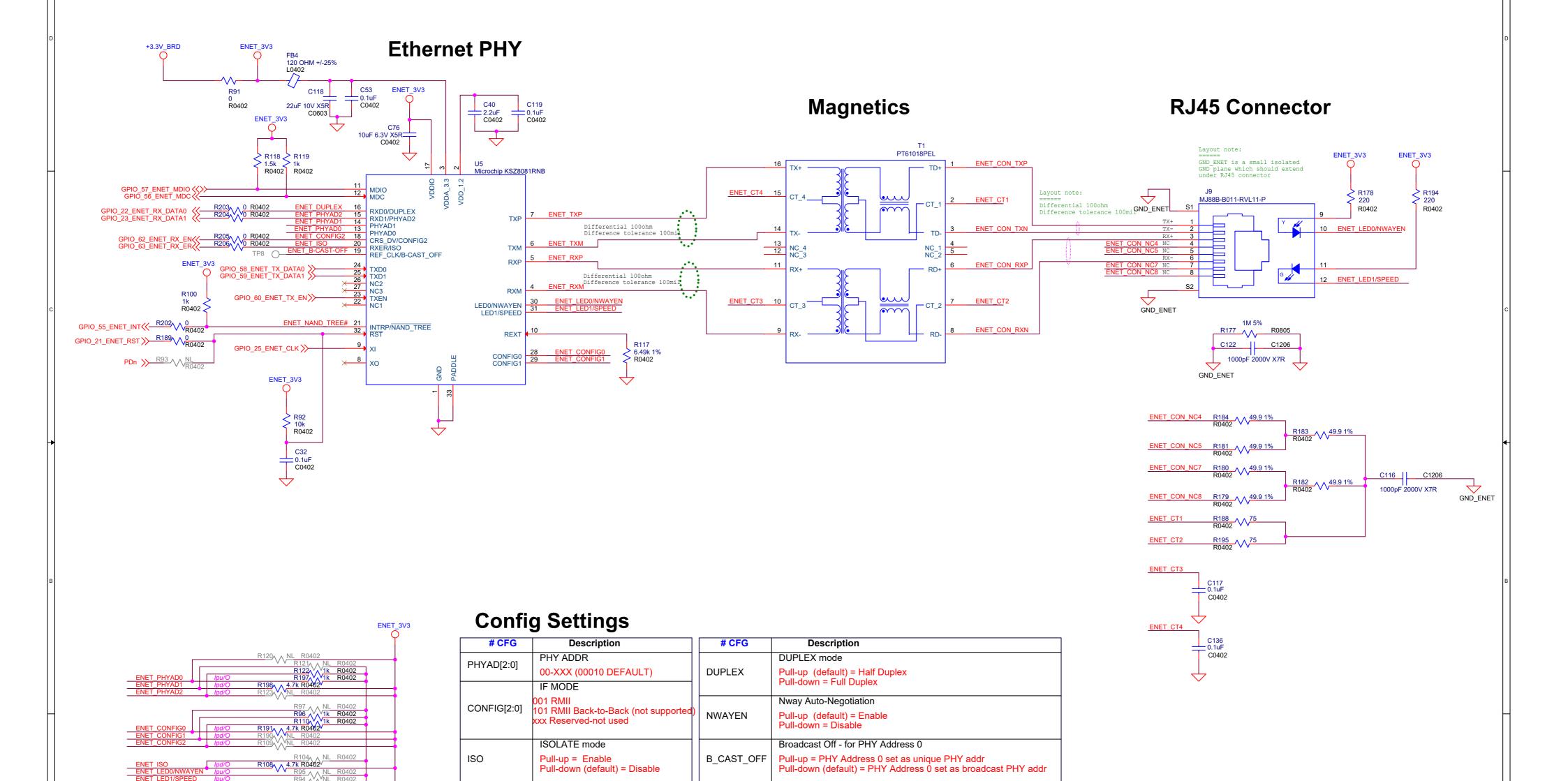
Company NXP Semiconductors

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# 10/100Mbps Ethernet



NAND Tree Mode

Pull-down = Enable

Pull-up (default) = Disable

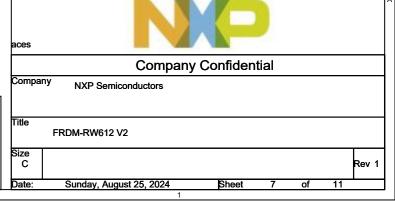
NAND\_TREE#

SPEED mode

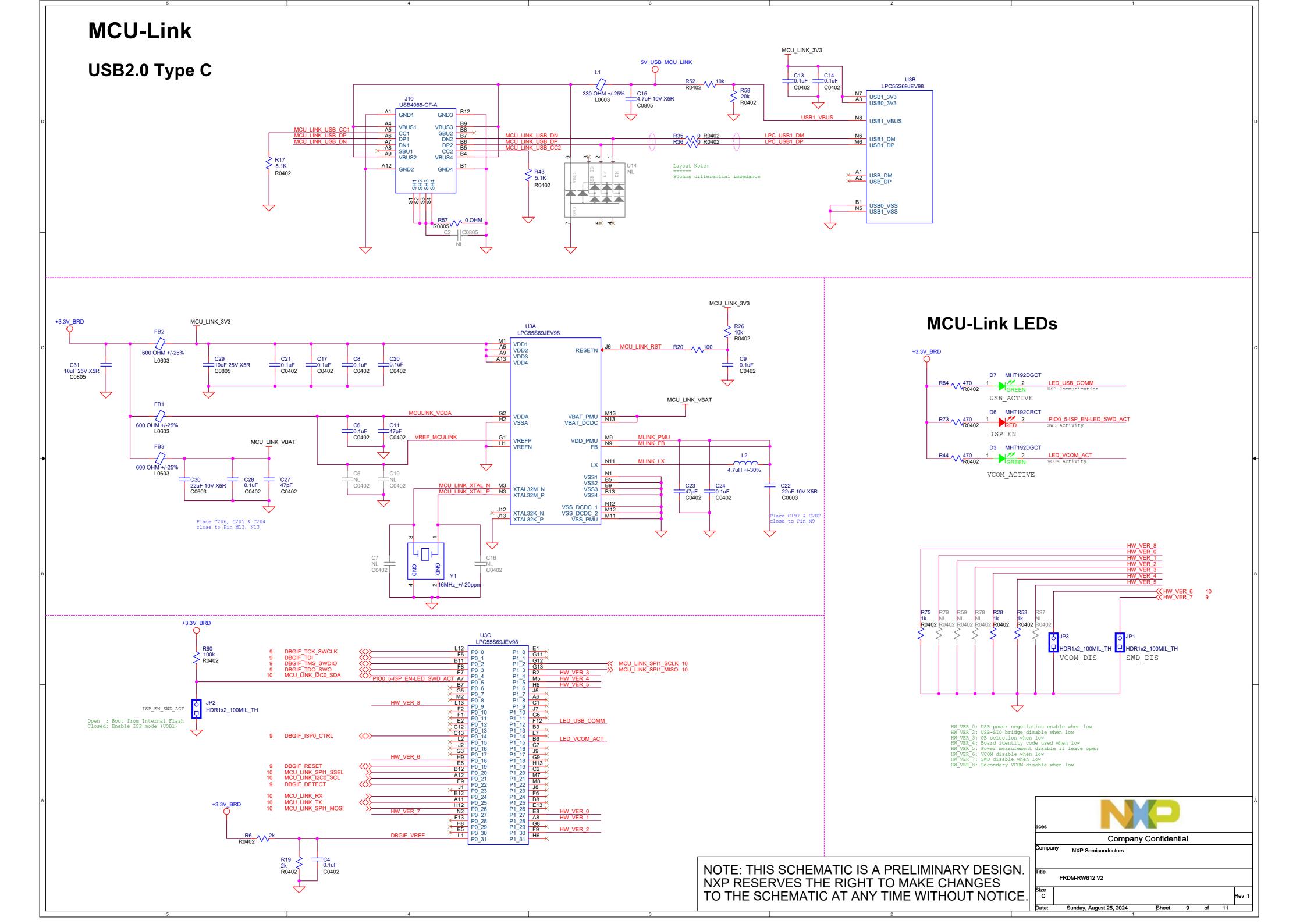
SPEED

R99 1k R0402

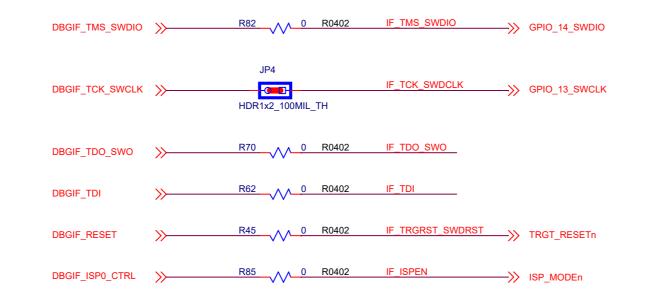
Pull-up (default) = 100Mbps Pull-down = 10Mbps

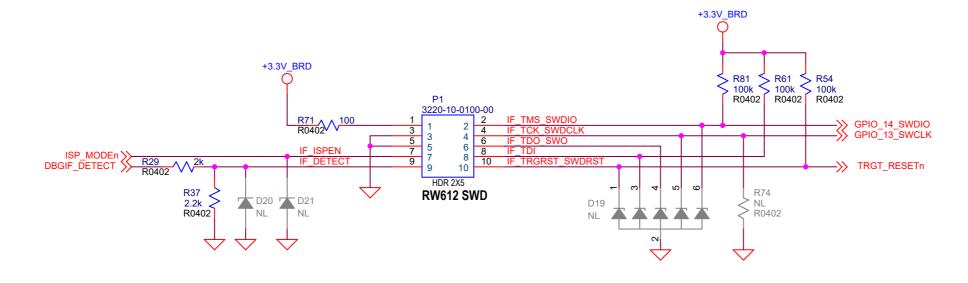


# ARDUINO SHIELD COMPATIBLE HEADERS **PMOD** 10uF 10V X5R GPIO\_16\_FC2\_I2C\_SDA\_PMOD GPIO\_17\_FC2\_I2C\_SCL\_PMOD GPIO\_44\_LCD\_SPI\_RESETn GPIO\_18\_ARD\_D4\_PMOD\_INT C12 | 10uF 10V X5R | C0603 NXP Low Cost LCD (LCD-PAR-S035) SSQ-108-03-G-D Mikro Bus 5VDC VR SUPPORT mikro BUS J5 5V\_HDR\_IN SSW-108-01-G-S SSW-108-01-G-S 3 O RST 2 O AN 2 O RST 4 O CS 5 O MISO 7 O MOSI 7 O MOSI 8 O VDD TGT SKT 1X8 PWM INT RX TX SCL SDA +5V GND C113 NL C0603 C104 NL \_\_\_\_\_ SYS\_5V 10uF 10V X5R C0603 C26 10uF 10V X5R C0603 Layout Notes: 1. mikroBUS™ logo positioned above the socket 2. Pin names corresponding to the routing of the mainboard 3. A line that encloses the socket on all sides except the top. 4. A diagonal notch below the right-hand side pinout (serves as a guideline for add-on board insertion) ARD\_VIN\_5-9V Company Confidential Company NXP Semiconductors NOTE: THIS SCHEMATIC IS A PRELIMINARY DESIGN. FRDM-RW612 V2 NXP RESERVES THE RIGHT TO MAKE CHANGES TO THE SCHEMATIC AT ANY TIME WITHOUT NOTICE.



# **MCU-Link Debug Interface**



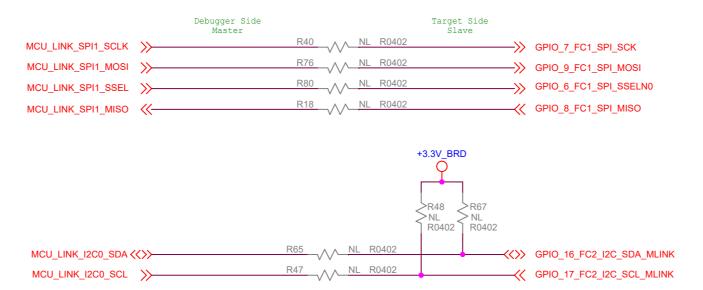


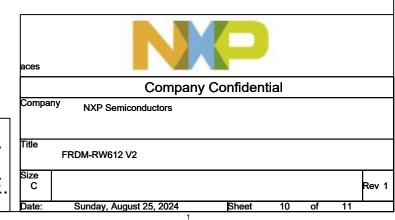
## **MCU-Link UART**

```
        MCU_LINK_TX
        R69
        100
        R0402
        R0402
        GPIO_24_FC3_UART_RXD_MLINK

        MCU_LINK_RX
        R77
        100
        R0402
        GPIO_26_FC3_UART_TXD_MLINK
```

# **USB** Bridge





#### **Revision History**

Design Version	Document revision	Change list
V1.0	Rev. 1	Initial release
V2.0	Rev. 1	- Add R220 (0 ohm) to connect WAKE switch to GPIO11 - R134 changed to No-Load (NL)

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Title

FRDM-RW612 V2

Size

C

Date: Sunday, August 25, 2024