**Shri Shankaracharya Institute of Professional Management & Technology, Raipur**

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**Course:** B.Tech **Semester:** 3rd

**Branch:** Computer Science And Engineering

**Subject Name:** Digital Electronics

**Subject Code:**

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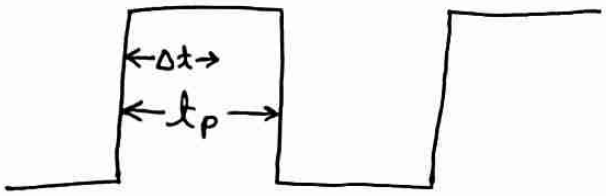
# PART - I

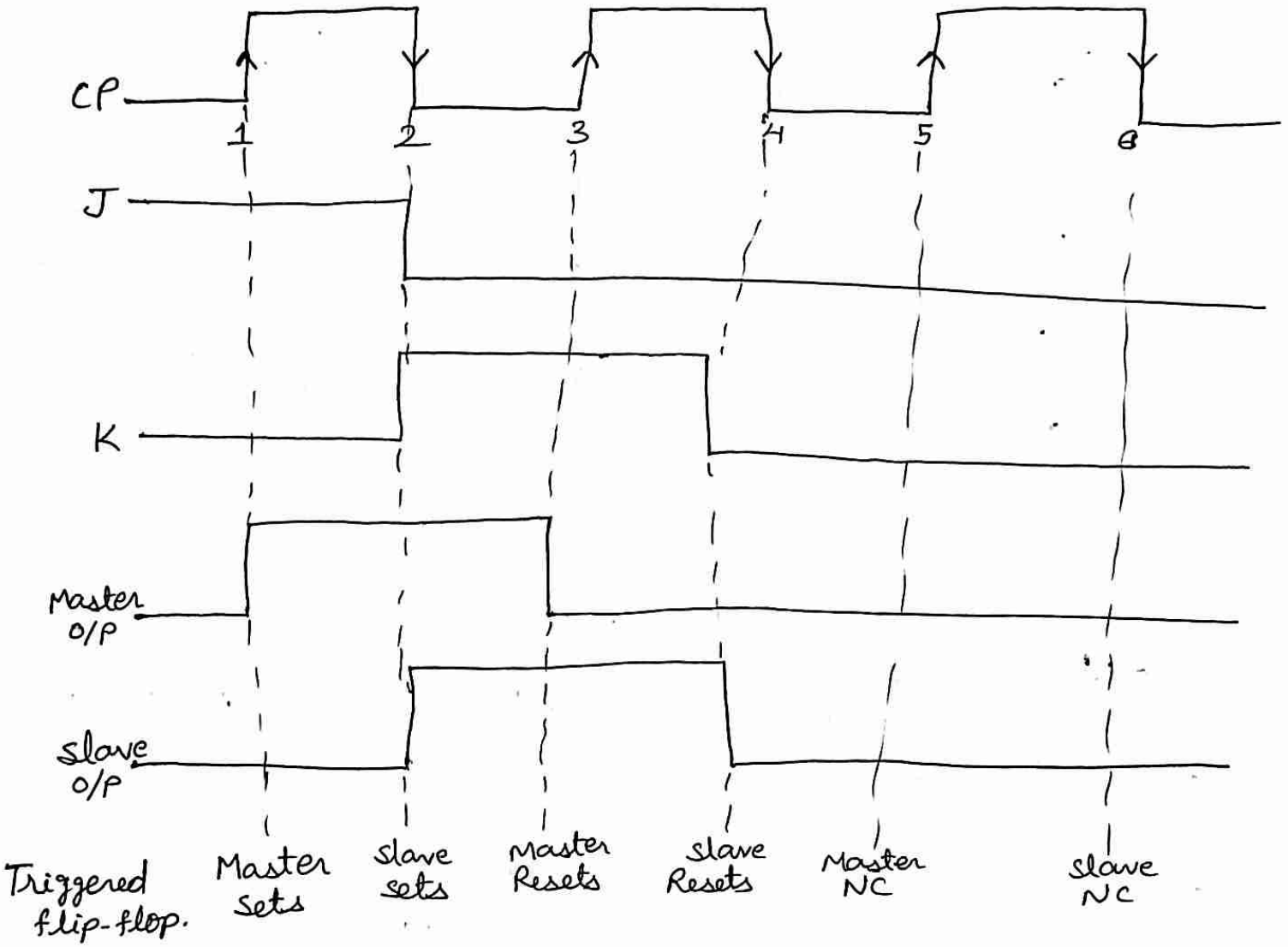
## Q17

Ans => **Race around condition:-** In level triggering triggered J.K. flip-flop when (J=K=1) both the inputs are 1, and without changing the input ~~are 1, and without~~ if output gets changed (toggeled) then this is called race Around condition.

In J.K. flip-flop, The output is feedback to the input, and therefore change in the output results change in the ~~ipud~~ input, if the inputs J=K=1. Assume Q=0. when a clock pulse with a width $t_p$ as shown in below is applied, output will change from 0 to 1 after the time interval $\Delta t$.




Input and Output waveform for master-slave flip-flop: The output state of the master flip-flop is determined by the J and K ~~ipt~~ input at the positive clock pulse. The output state of the master is then transfered as an input to the slave flip-flop. The ~~sct~~ slave flip-flop uses this input at the negative clock pulse to determine output state.




## Truth table for Master output:

| Clock Pulse | J | K | Master Output |
|---|---|---|---|
| 1 | 1 | 0 | 1 (Set) |
| 3 | 0 | 1 | 0 (reset) |
| 5 | 0 | 0 | 0 (NC) |

## Truth table for slave output :

| Clock Pulse | Master Output | Slave output |
|---|---|---|
| 2 | 1 (set) | 1 (set) |
| 4 | 0 (reset) | 0 (reset) |
| 6 | 0 (NC) | 0 (NC |

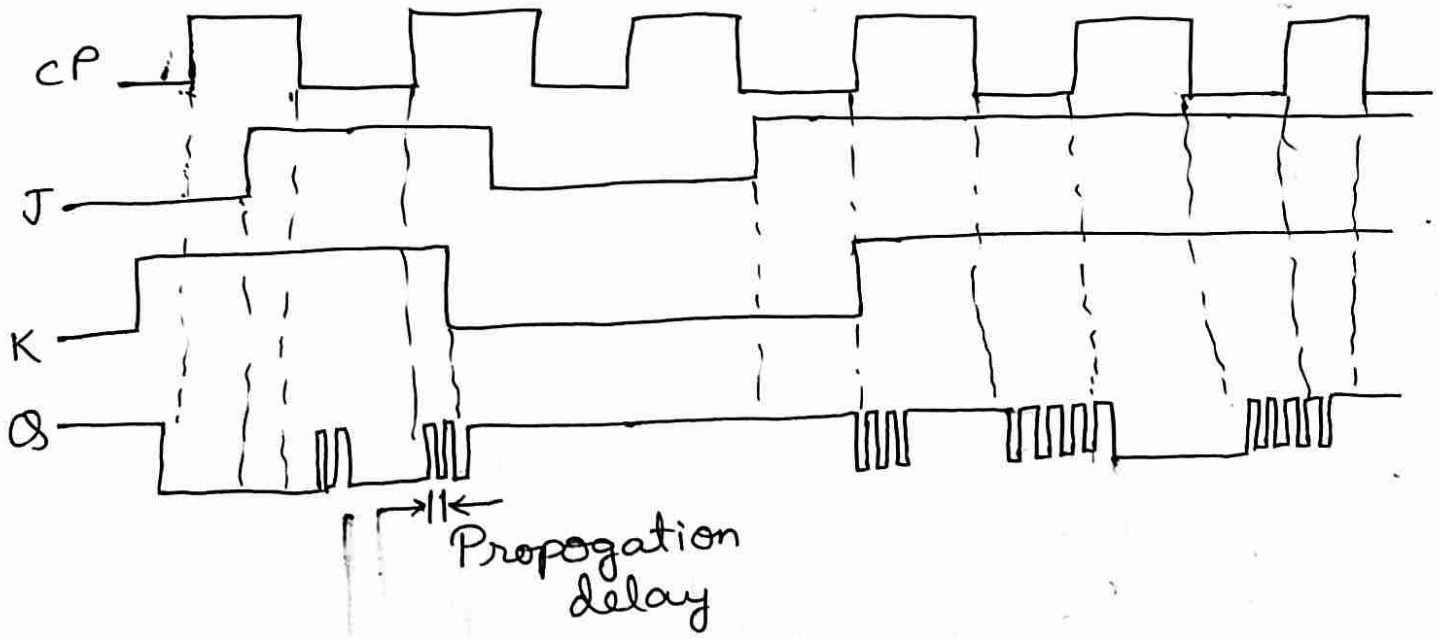
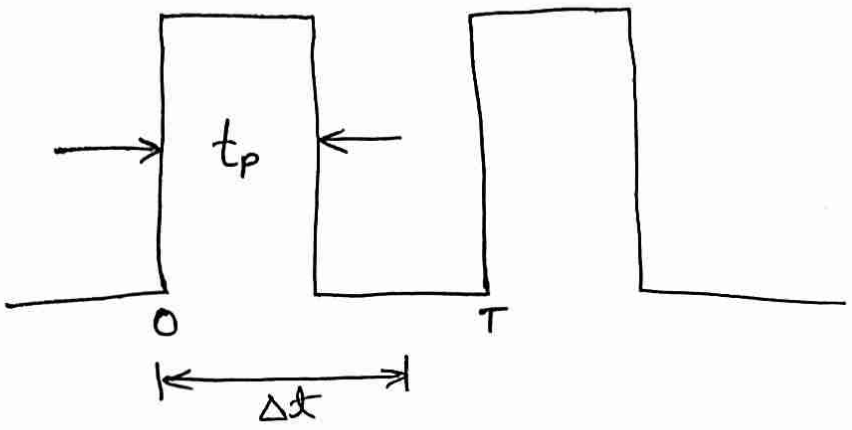


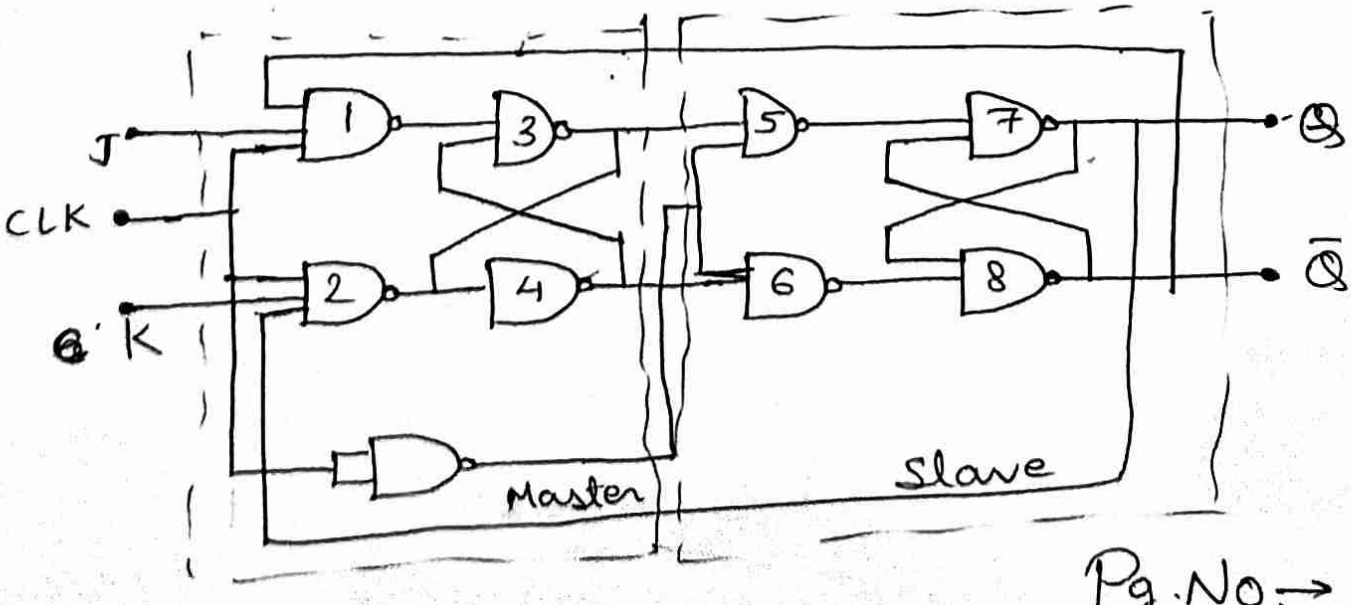

fig: Input and output waveforms for clocked JK flip-flop.

The race around condition can be eliminated when $t_p < \Delta t$.



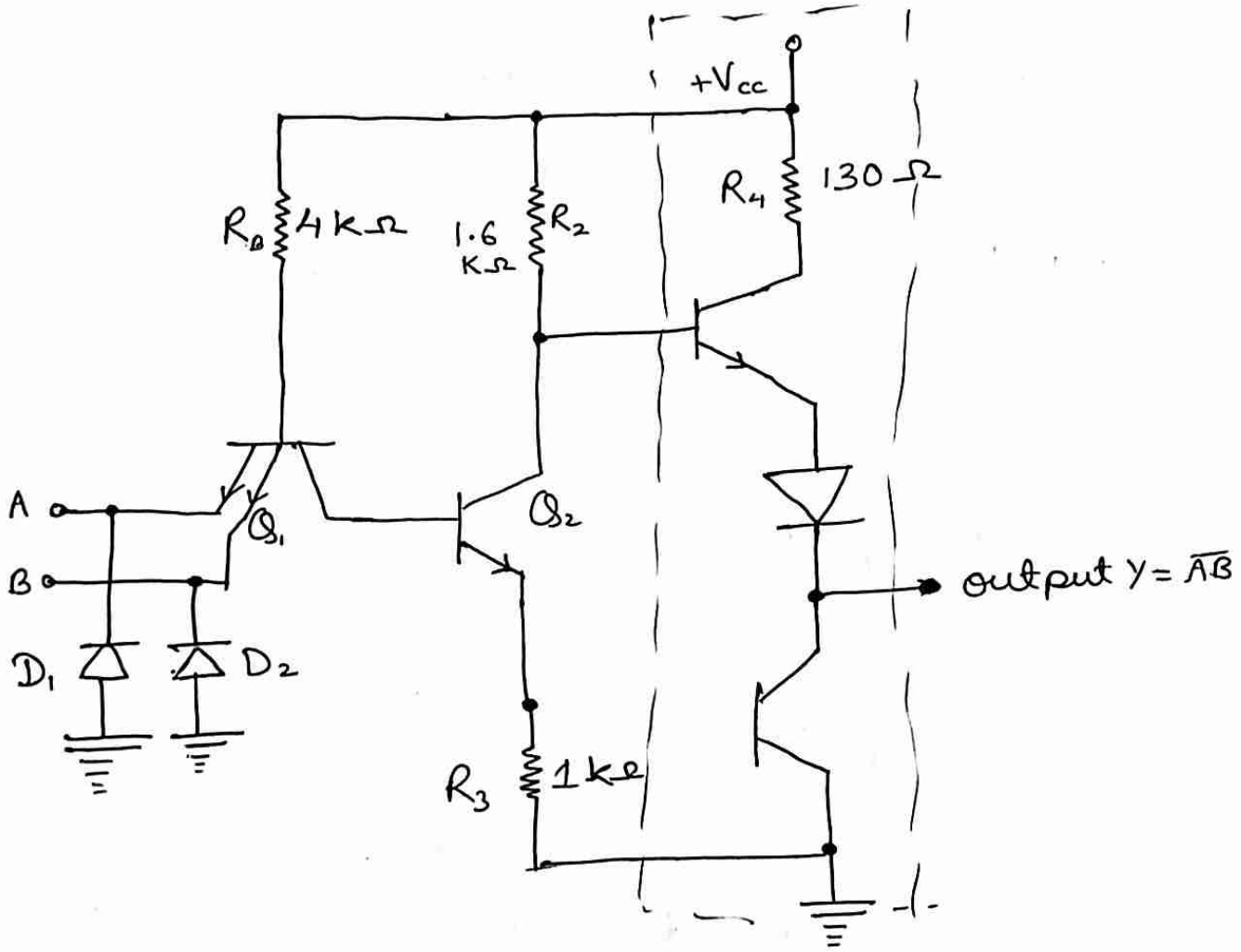

The value of $t_p$ can be reduced by using a pulse generator to produce less pulse width waveform, but it is difficult to get such type of circuit.

The value of $\Delta t$ can be increased by using the lumped delay lines in series with the feedback connection, which is worthless.



Q3>

Ans=> Two Input TTL NAND gate with totem-Pole output:




Truth Table for 2-input NAND gate:

| Input | | Transistor | | Output |
|---|---|---|---|---|
| A | B | $Q_2$ | $Q_4$ | Y |
| 0 | 0 | cutoff | cutoff | 1 |
| 0 | 1 | cutoff | cutoff | 1 |
| 1 | 0 | cutoff | cutoff | 1 |
| 1 | 1 | Saturation | Saturation | 0 |

## Circuit Operation:

1.) The output is taken from the collector of transistor $Q_4$. Each emitter of $Q_1$ acts like a diode. Therefore, transistor $Q_1$ and the 4 KΩ resistor act like a 2-ip input AND gate and the rest of the circuit inverts the signal. Hence, the overall circuit acts like a 2-ip input NAND gate.

2.) When either or all inputs (A and B) are at 0 V (logic 0), the corresponding emitter-base junction of $Q_1$ becomes forward-biased. The value of $R_B$ is selected so as to ensure that $Q_1$ is turned ON. However, the value of current $I_B$ flowing through the base of $Q_4$ are cutoff so that the output voltage is at $V_{cc}$ (logic 1).

3. If all the inputs are high (logic 1), the emitter-base junction of $Q_1$, is reverse-biased so that it has no base current. Hence, $Q_1$ is off. However, its collector-base junction is forward-biased supplying base current $I_{B_1}$ to $Q_1$. The current $I_{B_2}$ will be sufficiently large to saturate $Q_2$. As a result, transistor $Q_2$ is turned ON and the drop across $R_2$ is sufficient to forward bias the base-emitter junction of $Q_4$, therefore turning $Q_4$ ON. Hence, the output at its collector is low (logic 0). The function of diode D is is to prevent both $Q_2$ and $Q_4$ from being ON simultaneously.

4.) In the absence of diode D, the transistor $Q_3$ will conduct slightly when the output is LOW. In order to prevent this, the diode is connected between the emitter of $Q_3$ and the collector of $Q_4$. The voltage drop across the diode keeps the base - emitter junction of $Q_3$ reverse-biased. In this way, transistor $Q_4$ only conducts when the output is Low, which confirms the conditions for NAND operation.

5.) Transi $Q_3$ and $Q_4$ form a Totem-pole transistors are used because they produce a low output impedence. Either $Q_1$, acts as an emitter follower (High output), or Q is saturated (low output).

# Part - II

Q2) 2

Ans => CMOS → The term CMOS stands for complementory metal oxide semiconductor. This is the one of the most popular technology in the computer chip used to form integrated circuits in numerous and varied.

## CMOS NAND Gate:

A 2-input CMOS NAND gate consists of two series NMOS transistors between Y and Ground and two parallel PMOS transistor between Y and VDD.

→ If either input A or B is logic 0, atleast one of the NMOS transistors will be off, breaking the path from y to ground.

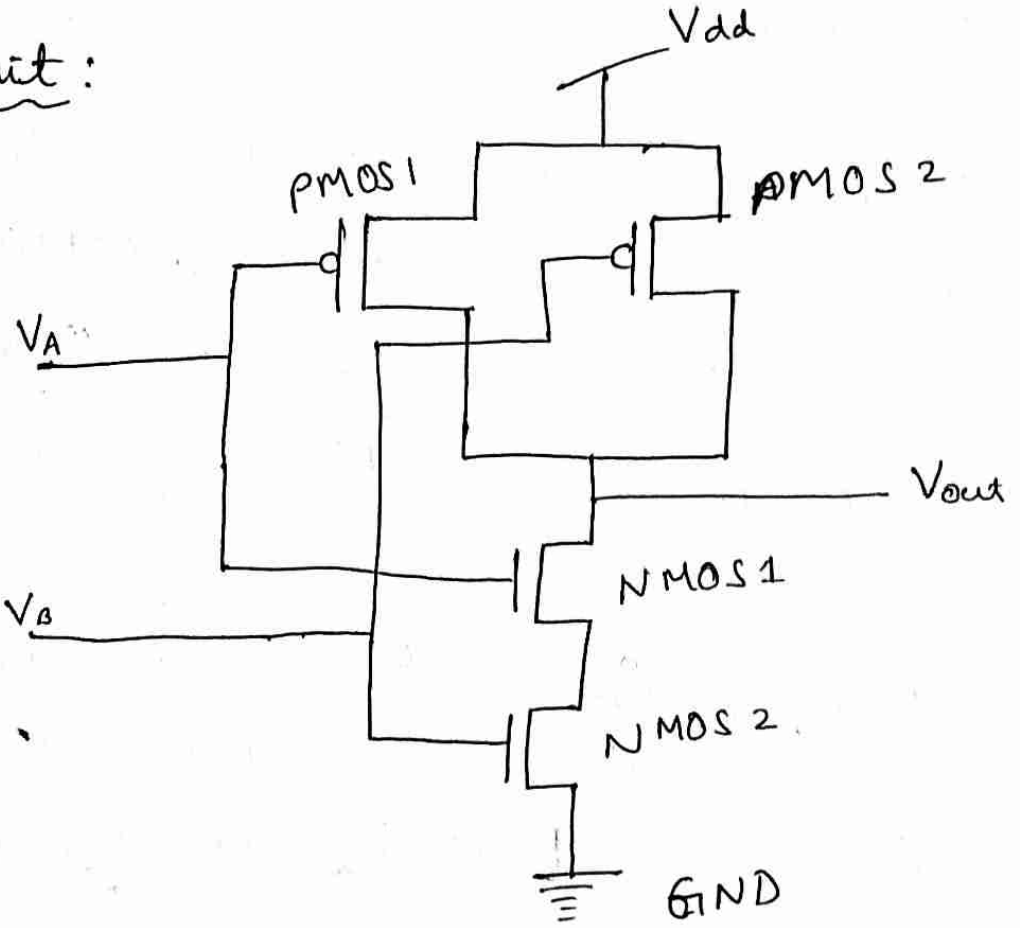
But atleast one of the PMOS transistor is ON, creating a path from Y to VDD.

~~Two input~~

Truth Table:

| $V_A$ | $V_B$ | Vout |
|---|---|---|
| Low | Low | High |
| Low | High | High |
| High | Low | High |
| High | High | LOW |

Cicuit:



Case-1 $V_A$ - Low & $V_B$ = Low

As $V_A$ and $V_B$ both are low, both the pMOS will be ON and both the nMOS will be OFF. So the output Vout will get two paths through two ON pMOS to get connected with Vdd. The output will be charged to the Vdd level. The output line will not get any path to the GND as both the nMOS are off. So, there is no path through which the output line can discharge. The output line will maintain the voltage level at Vdd so high.

Case-2: $V_A$ - Low & $V_B$ - High

$V_A$ - Low: pMOS1 - ON ; nMOS1 - OFF

$V_B$ = High: pMOS2 - OFF ; nMOS2 - ON

pMOS1 and pMOS2 are in parallel. Through pMOS is off, still the output line will get a path through pMOS1 to get connected with Vdd. nMOS1 and nMOS2 are in series. As nMOS1 is OFF, so Vout will not be able to find a path to GND to get discharged. This is turn results the Vout to be maintained at the level of Vdd. so High.

Case-3: $V_A$ - High & $V_B$ - Low

$V_A$ - High: pMOS1 - Off ; nMOS1 - ON

$V_B$ - LOW : pMOS2 - ON; nMOS2 - OFF

The explanation is similar as cas2 Vout level will be High.

Case-4: $V_A$ - High & $V_B$ - High

$V_A$ - High: pMOS1 - OFF ; nMOS1 - ON

$V_B$ - High: pMOS2 - OFF ; n MOS2 - ON

Part - II

Answer = 3

when counter is clocked such that each flip-flop in the counter is triggered at the same time. the counter is called as Synchronous counter.

Below figure shows a two stage synchronous counter

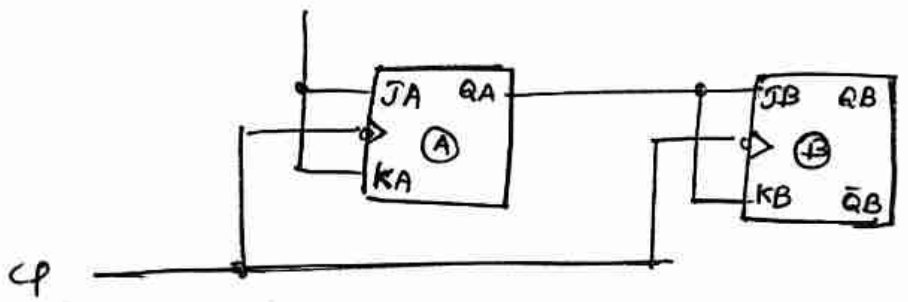



fig 2-bit synchronous binary counter

Here clock signal is connected in parallel to clock inputs of both the flip-flops.

But QA output of first stage is used to drive the J and K inputs of the second stage.

Operation of the circuit

Initially, we asume that the $Q_A = Q_B = 0$.

When positive edge of first clock pulse is applied, flip-flop A will toggle because $J_A = K_A = 1$. whereas flip-flop B output will remain zero because $J_B = K_B = 0$

| CP | $Q_B$ | $Q_A$ |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 2 | 1 | 0 |
| 3 | 1 | 1 |

(b) State Sequence.

fig. Timing diagram (a) and state sequence (b) for 2-bit synchronous counter.