Shri Shankaracharya Institute of Professional Management & Technology, Raipur

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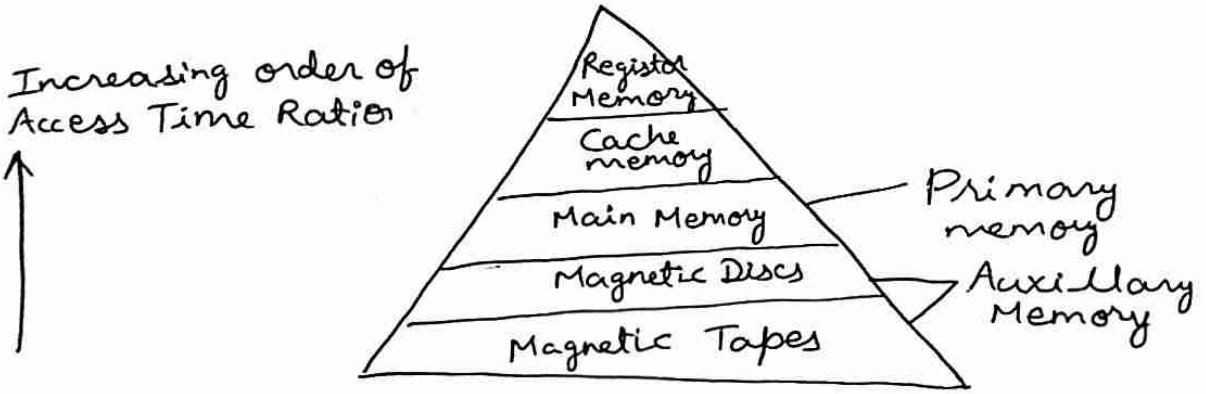
Q2 A

Ans

The memory hierarchy design in a computer system mainly includes different storage devices. Most of the computers were inbuilt with extra storage to run more powerfully beyond the main memory capacity. The following memory hierarchy diagram is a hierarchial pyramid for computer memory. The designing of the memory hierarchy is divided into two types such as primary (or internal) memory and secondary (External) memory.



Primary Memory:

The primary memory is also known as internal memory, and this is accessible by the processor straightly. This memory includes main, cache, as well as CPU registers.

Secondary Memory:

The secondary memory is also known as external memory, and this is accessible by the processor through an input/output module. This memory includes an optical disk, magnetic disk, and magnetic tape.

Registers:

Usually, the register is a static RAM or SRAM in the processor of the computer which is used for holding the data word which is typically 64 or 128 bits. The program counter register is the most important as well as found in all the processors.

Cache Memory:

It can also be found in the processor, however rarely it may be another IC (integrated circuit) which is seperated into levels. The cache holds the chunks of data which are frequently used from main memory. when the processor has a single core then it will have two (or) more cache levels rarely.

Main Memory:

The main memory in the computer is nothing but, the memory unit in the CPU that communicates directly.

Magnetic Disks:

The magnetic disks in the computer are circular plates fabricated of both plastic otherwise metal by magnetized material. Frequently, two faces of the disk are utilized as well as many disks may be stacked on one spindle by read or write heads obtainable on every plane.

Magnetic Tape:

This tape is a normal magnetic recording which is designed with a slender magnetizable covering on an extended, plastic film of the thin strip. This is mainly used to backup huge data. Whenever the computer requires to access a strip, first it will mount to access the data.

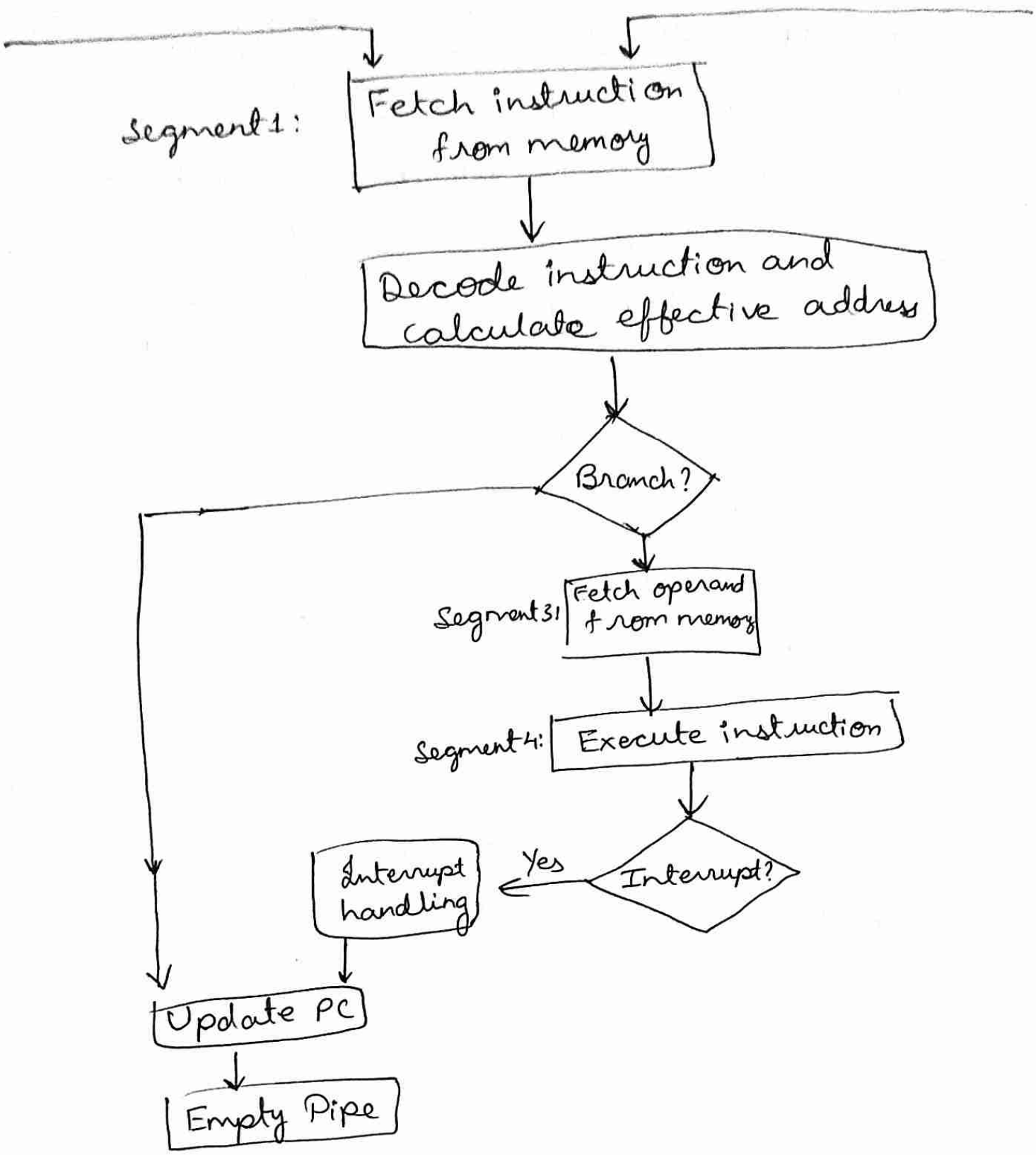
Advantages of Memory Hierarchy:

The need for a memory hierarchy includes the following.

1. Memory distributing is simple and economical.
2. Removes external destruction.
3. Data can be spread all over
4. Permit demand paging & pre-paging.
5. Swapping will be more profficient.

Q8 B)

Ans


Segment 1:
Fetch instruction from memory
Decode instruction and calculate effective address
Branch?
Segment 3:
Fetch operand from memory
Segment 4:
Execute instruction
Interrupt?
Yes
Interrupt handling
Update PC
Empty Pipe

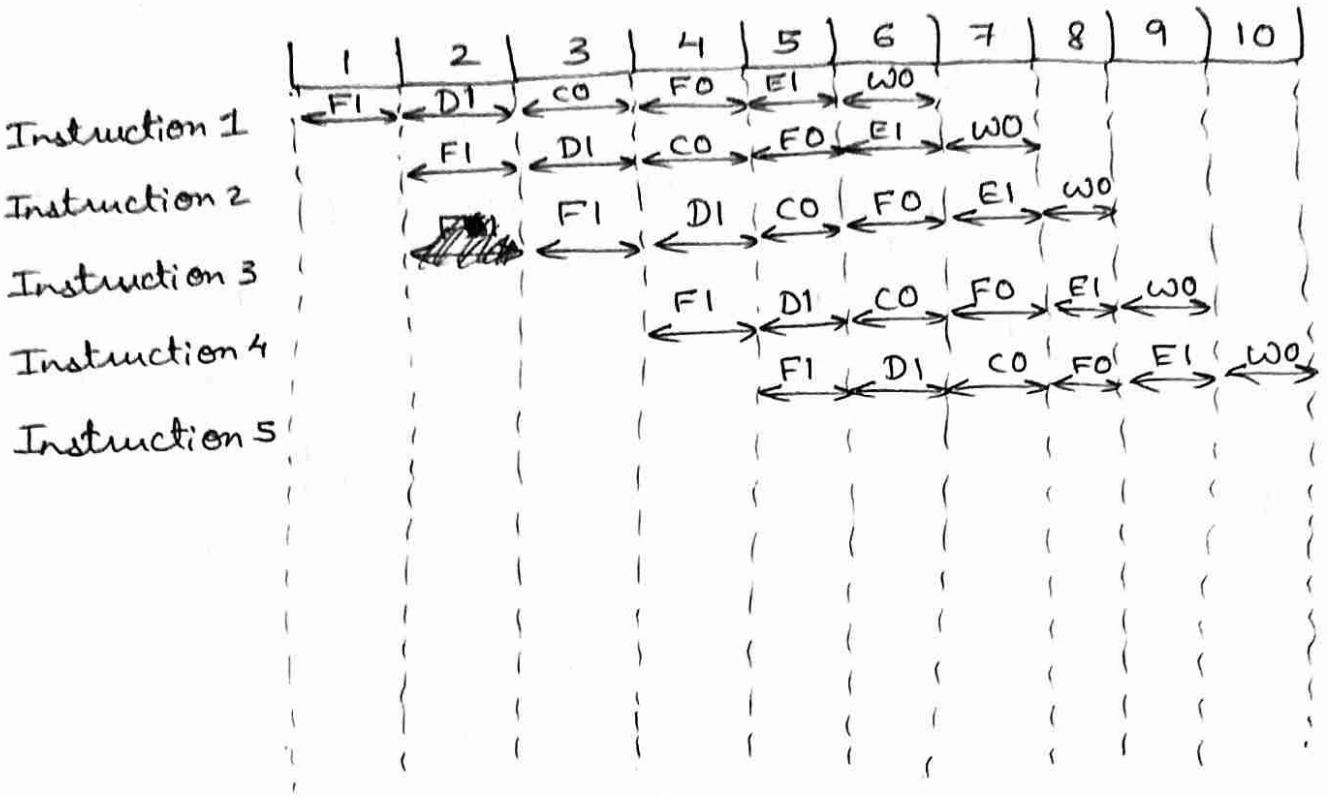
Segment 1:
The instruction fetch segment can be implemented using first in, first out (FIFO) buffer.

Segment 2:
The instruction fetched from memory is decoded in the second segment, and eventually, the effective address is calculated in a seperated arithmetic circuit.

segment 3:
An operand from memory is fetched in the third segment.

Segment 4:
The instructions are finally executed in the ~~third~~ last segment of the pipeline orgnaization.

Timming Diagram for instruction pipeline operation:



Q C>

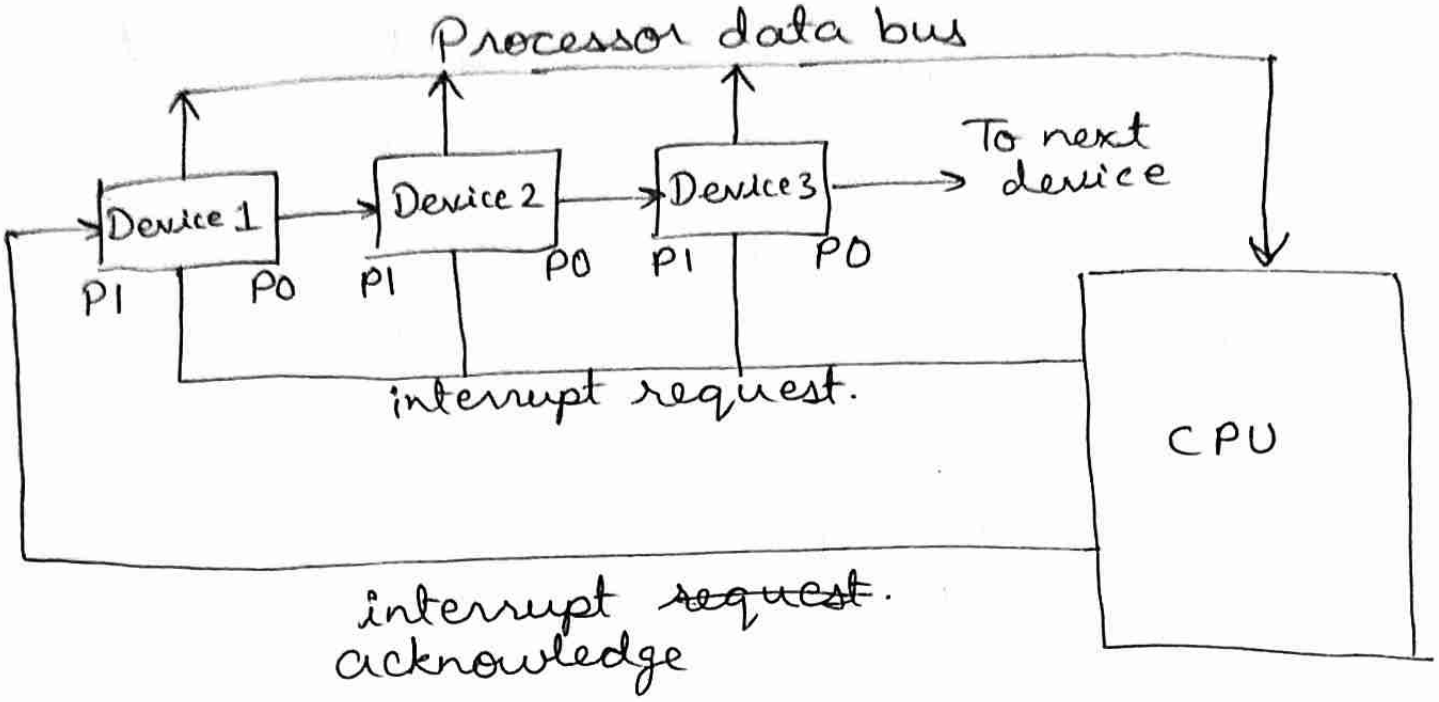
Ans

Priority Interrupt: A priority interrupt is a system which decides the priority at which various devices, which generates the interrupt signal at the same time, will be serviced by the CPU. The system has authority to decide which conditions are allowed to interrupt the CPU, while some other interrupt is being serviced. Generally, ~~div~~ devices with high speed transfer such as magnetic disks are given high priority and ~~slow~~ slow devices such as keyboards are given low priority.

Daisy Chaining Priority:

This way of deciding the interrupt priority consists of several connection of all the devices which generates an interrupt signal. The device with the highest priority is placed at the first position followed by lower priority devices and the device which has lowest priority among all is placed at the last in the chain.

In daisy chaining system all the devices are connected in a serial form. The interrupt line request is common to all devices. If any device has interrupt signal in low level state then interrupt line goes to low level state and, enables the interrupt input into the CPU.


Processor data bus
Device 1
Device 2
Device 3
To next device
P1
P0
P1
P0
P1
P0
interrupt request.
CPU
interrupt request.
acknowledge

Q 5)

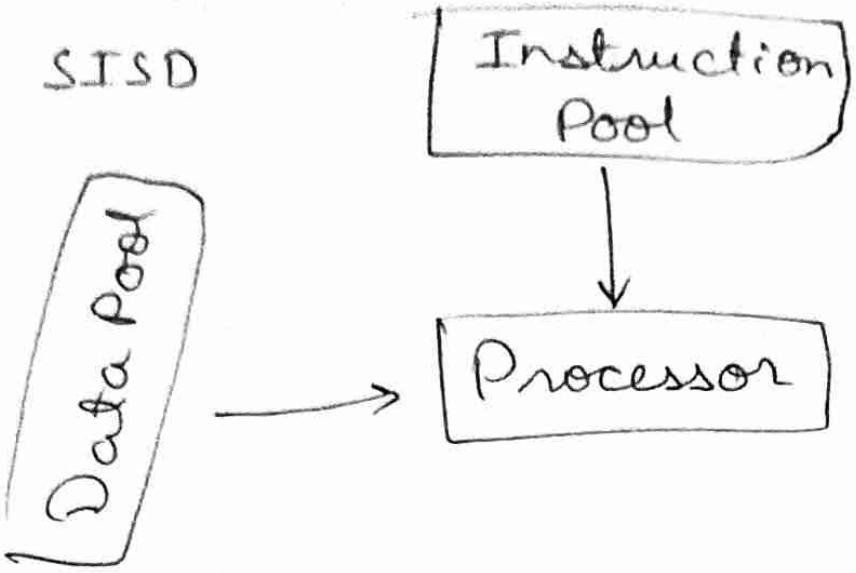
Ans

Parallel computing is a computing where the jobs are broken into discrete parts that can be executed concurrently. Parallel systems deal with the simultaneously on different CPU's. Parallel systems are more difficult to program than computers with a single processor.

Flynn's classification -

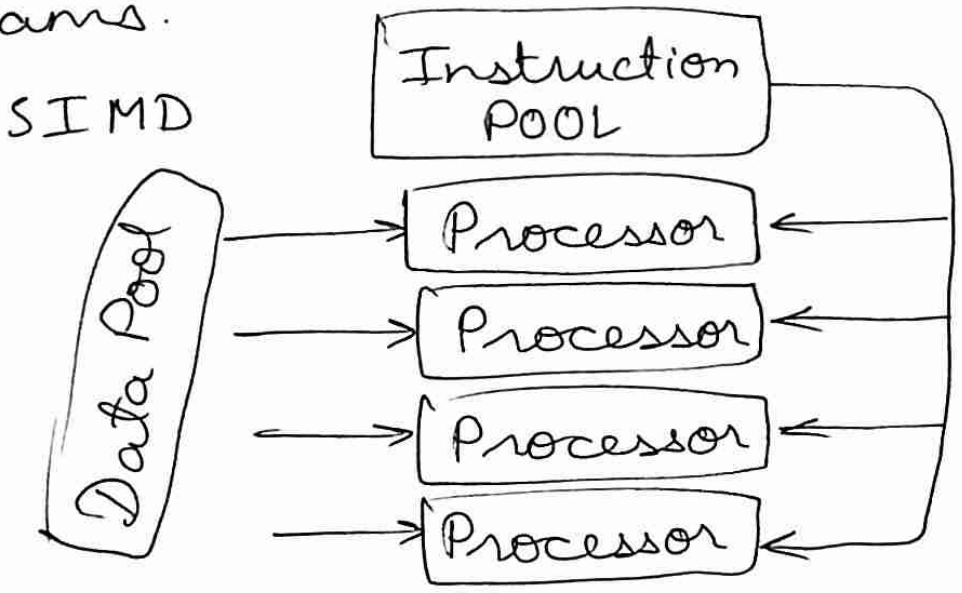
1.) Single - instruction, single - data (SISD) systems -

An SISD computing system is a uniprocessor machine which is capable of executing a single instruction, operating on a single data stream.



2.) Single-instruction, multiple-data (SIMD) systems -

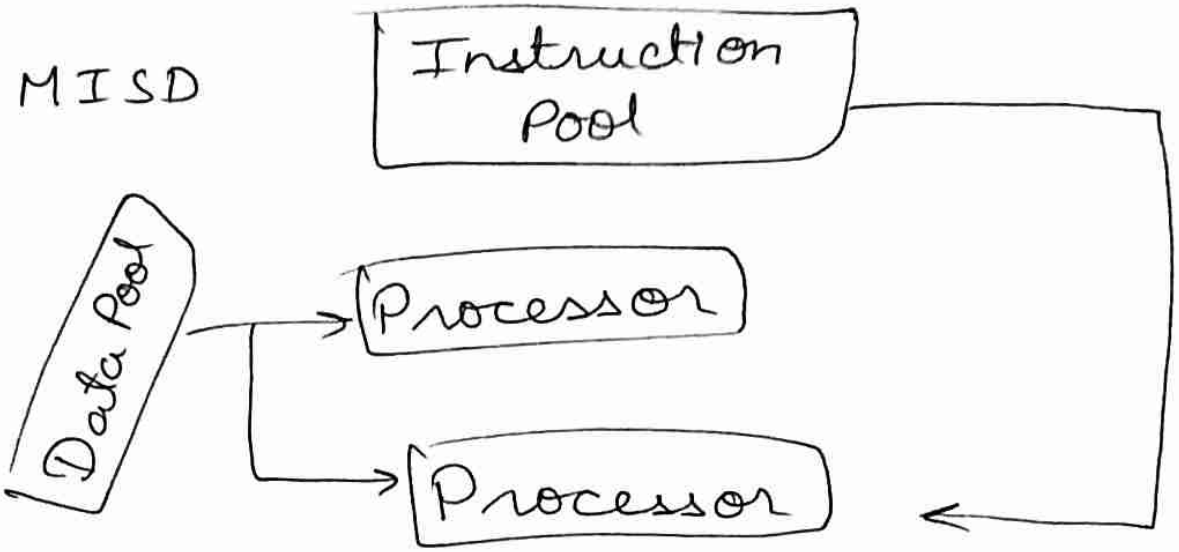
An SIMD system is a multiprocessor machine capable of executing the same instruction on all the CPUs but operating on different data streams.



3.) Multiple - instruction, single - data (MISD) systems -

An MISD computing system is a multiprocessor machine capable of executing different instructions on different PEs but all of them operating on the same dataset.

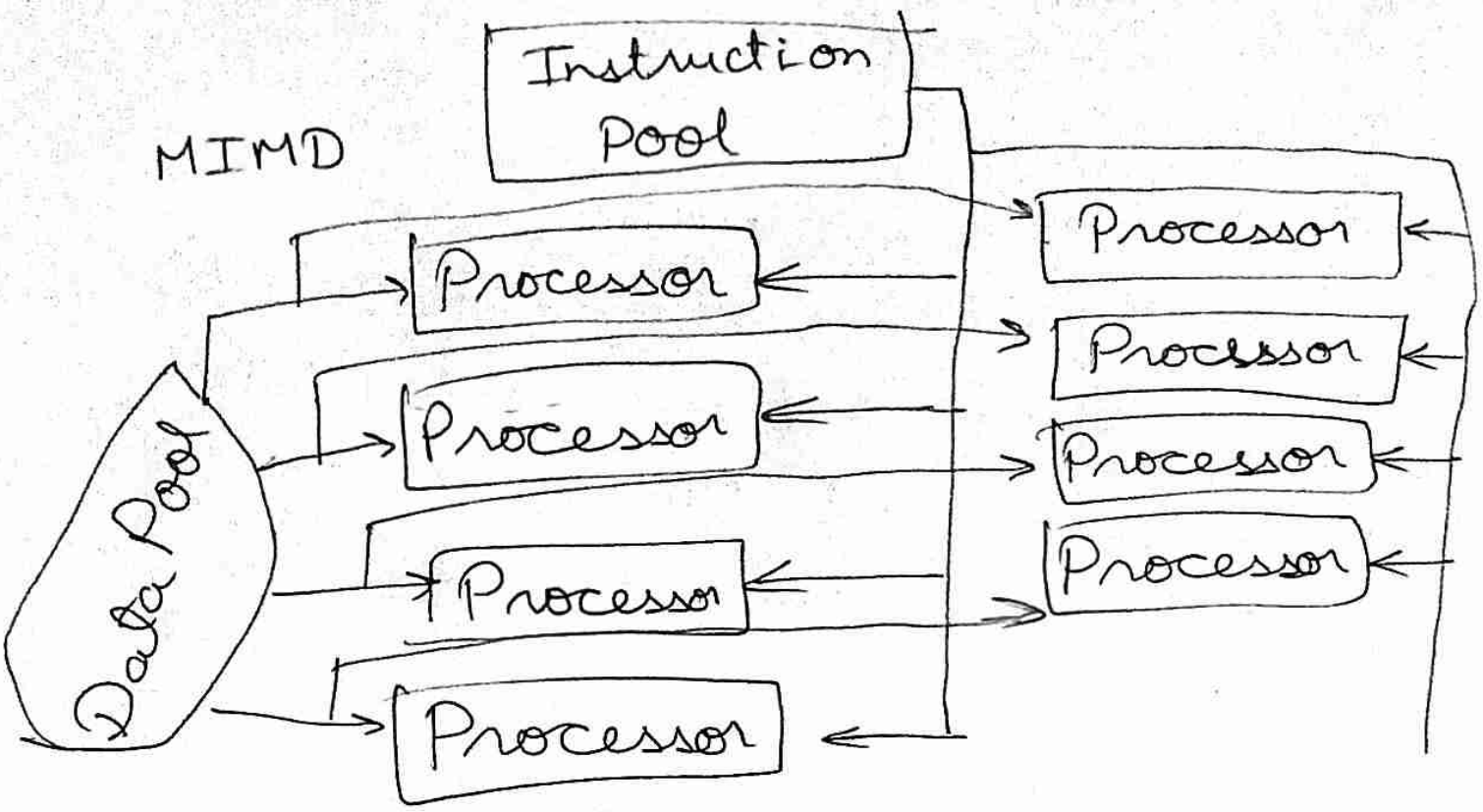
MISD



4.) Multiple - instruction, multiple - data (MIMD) systems -

An MIMD system is a multiprocessor machine which is capable of executing multiple instructions on multiple data sets.

MIMD


Instruction Pool
Data Pool
Processor
Processor
Processor
Processor
Processor
Processor
Processor
Processor

OSDE>

Ans

DMA controller is a hardware device that allows I/O devices to directly access memory with less participation of the processor. DMA controller needs the same old circuits of an interface to communicate with the CPU and Input/output devices.

→ Hold - hold signal
→ HLDA - hold acknoledgment.
→ DREQ - DMA request.
→ DACK - DMA acknowledgment.

Suppose a ~~fdd~~ floppy drive that is connected at input - output port wants to transfer data to memory, the following steps are performed:

→ Step 1: First of all the floppy drive will send a DMA request (DREQ) to the DMAC, it means the floppy drive wants its DMA service.

→ Step-2: Now the DMAC will send a HOLD signal to the CPU.

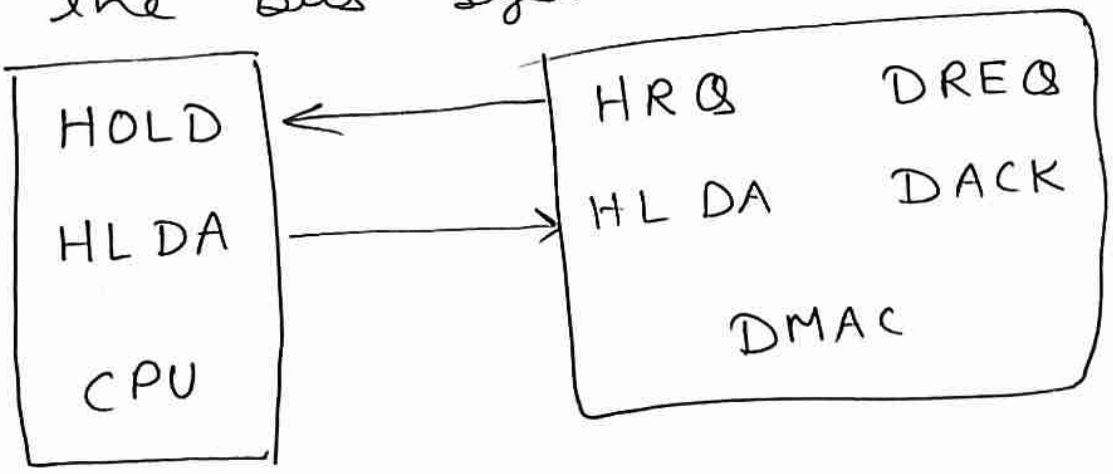
→ Step-3: After accepting the DMA service request from the DMAC, the CPU will send hold acknowledgment (HLDA) to the microprocessor has released control of the address bus the data bus to DMAC and the microprocessor / computer is bypassed during DMA service.

Step-4> Now the DMAC will send one acknowledgment (DACL) to the floppy drive which is connected at the input-output port. It means the DMAC tells the floppy drive be ready for its DMA service.

Step-5> Now with the help of input-output read and memory write signal the data is transfered from the floppy drive to the memory.

Modes of DMAC:

1.) single Mode: In this only one channel is used, means only a single DMAC is connected to the bus system.



2.) Cascade Mode :

In this multiple channels are used, we can further cascade more number of DMACs.