CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, BHILAI

For Practical Examination Only

Session: Nov-Dec 2021 Examination

Name of Examination: B.tech, Regular **Semester:** 3rd **Date:** 06./.04/2022

Subject Code: B022322(022) **Subject Name:** DELD Laboratory

Name of Student: V Om Sai Nageshwar Sharma

Roll No. of Student: 303302220020 **Enroll No:** BJ4599

Name of the Institution: SSIPMT, Raipur **Institute Code:** 033

Name of Experiment Allotted: Q) To realize full subtractor by using basic gates and NAND gates (construction of full substractor)

Signature of Student


CHHATTISGARH SWAMI VIVEKANAND
TECHNICAL UNIVERSITY
Bhilai, Durg, Chhattisgarh
Admit Card for Session Nov-Dec 2021
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3 SEMESTER
V Somshekhar Sharma
B Tech
B Tech Computer Science Engineering
SUBJECT DETAILS
Subject Type
Subject Code
Subject Name
Exam Session
Exam Type
ToAppear
Date & Time of Exam
B000311(022) Data structure & Algorithms
B000312(014) Mathematics - III
B000313(022) Principles of Programming Languages
B000314(022) Digital Electronics& Logic Design
B000315(022) Operating Systems
B000321(022) Data structure & Algorithms Laboratory
B000322(022) Digital Electronics& Logic Design Laboratory
B000323(022) Operating Systems Laboratory (UNIX)
B000324(022) Software Laboratory (Sci Lab/MATLAB)
Nov-Dec 2021
Regular
23/03/22 10:00 am
21/03/22 10:00 am
25/03/22 10:00 am
28/03/22 10:00 am
30/03/22 10:00 am
05/04/22 10:00 am
06/04/22 10:00 am
01/04/22 10:00 am
04/04/22 10:00 am
Signature of the Candidate (while receiving)
Signature of the Principal
Signature of COE
INSTRUCTION FOR WRITTEN EXAMINATION

Aim: To realise full subtractor by using basic gates and NAND gates.

Apparatus Required: Patch cords, IC trainer kit, IC 1408, IC 1486.

Theory: It is a 3-bit arithmatic substractor. Substracting two single bit binary values B, C in form of a single bit value, A, produces a difference bit, D, and a borrow out, B, bit, this is called full substractor. The boolean function describing the full substractor are -

$$D = A \oplus B \oplus C$$

$$B = \bar{A}B + \bar{A}C + BC$$

Procedure :

(i) Switch on the power supply.

(ii) Check the components for their working.

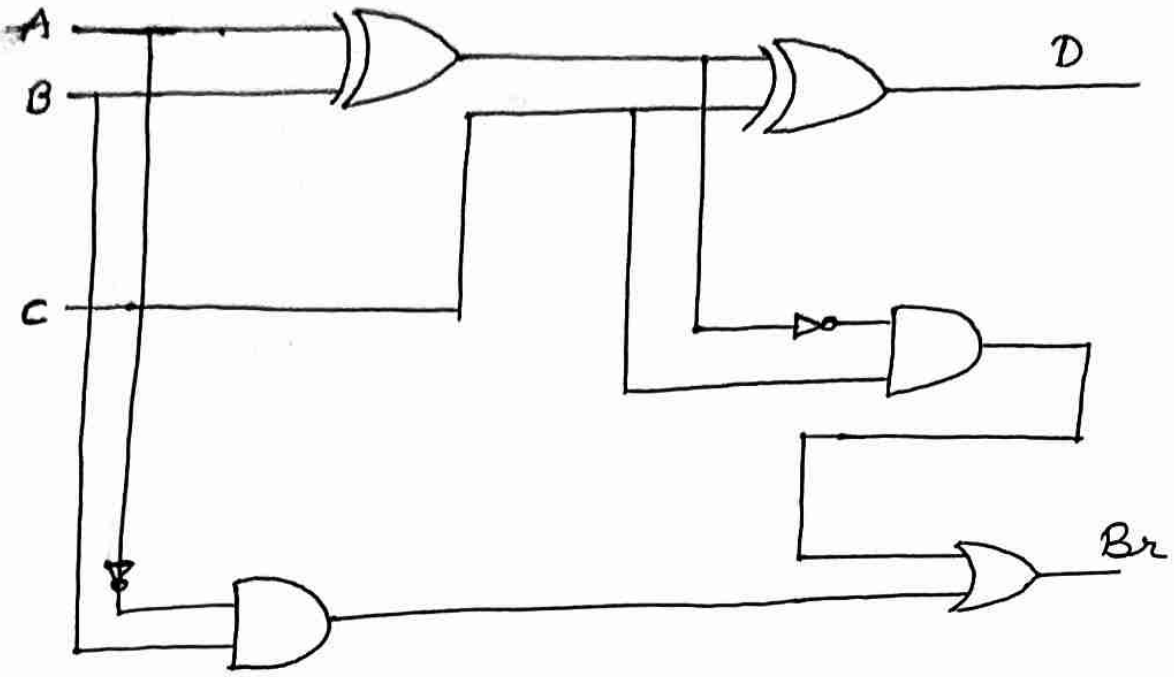
(iii) Insert the appropriate IC into the IC base.

(iv) Make connection as per the circuit ~~diagnose~~ diagram.

(v) Verify the truth table & observe the output.

Observation :

INPUT			OUTPUT	
A	B	C	D	Br
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



Circuit Diagram