ICS Homework 13

May 11, 2023

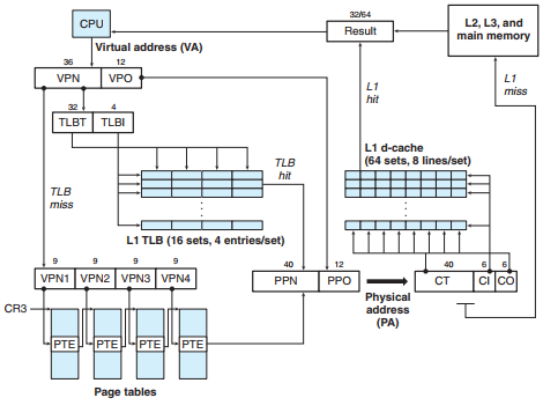


Figure 9.22 **Summary of Core i7 address translation.** For simplicity, the i-caches, i-TLB, and L2 unified TLB are not shown.

1 Organization

1.1 Virtual Memroy 1

Which type of address is used in each of following scenarios, **virtual** or **physical** address?

The address of variables in C program	V
The address stored in a C pointer	V
The address of a C pointer	V
The address used in looking up L1 cache	P
The value in CR3	P
The address in L2 PTE	P
The address in L4 PTE	P
The value in PC register	V

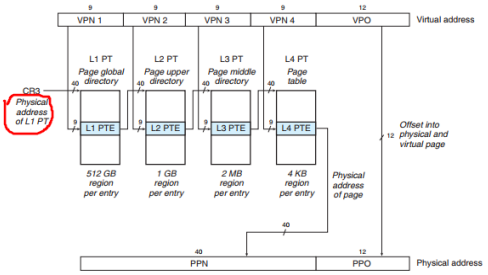


Figure 9.25 **Core i7 page table translation.** PT: page table; PTE: page table entry; VPN: virtual page number; VPO: virtual page offset; PPN: physical page number; PPO: physical page offset. The Linux names for the four levels of page tables are also shown.

1.2 Virtual Memory 2

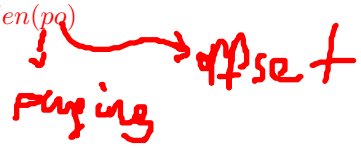
The lookup of L1 cache usually consists of three steps:

1. locating the set
2. comparing the tag of each cache line in the set
3. returning bytes from cache or loading 1 value from next level memory system.

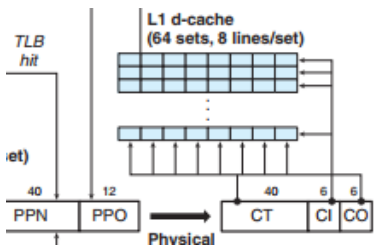
As the lookup uses physical address, the hardware can only start the cache lookup after address translation is completed. How to make cache lookup and address translation parallelized?

Show the requirements to the parameters of your paging and cache system.

ANS: Make sure the set bits of cache are in the page offset bits, so the hardware could locate the set and do address translation simultaneously. This requires $s + b \leq len(po)$



a Core i7 with 4 KB pages has 12 bits of VPO, and these bits are identical to the 12 bits of PPO in the corresponding physical address. Since the 8-way set associative physically addressed L1 caches have 64 sets and 64-byte cache blocks, each physical address has 6 ($\log_2 64$) cache offset bits and 6 ($\log_2 64$) index bits. These 12 bits fit exactly in the 12-bit VPO of a virtual address, which is no accident! When the CPU needs a virtual address translated, it sends the VPN to the MMU and the VPO to the L1 cache. While the MMU is requesting a page table entry from the TLB, the L1 cache is busy using the VPO bits to find the appropriate set and read out the eight tags and corresponding data words in that set. When the MMU gets the PPN back from the TLB, the cache is ready to try to match the PPN to one of these eight tags.



2 System Software

2.1

Which level would the following data being shared? Answer with **not shared**, **threads**, or **processes**.

For example, if X is shared between threads but not shared between processes, answer **threads**.

File descriptor table	threads
File table	processes
Stack	not shared
Heap	threads
Program counter	not shared
Condition code	not shared
Installed handler	threads
V-node table	processes