ICS Homework 5

March 16, 2021

1 Pipeline

Suppose we add a new instruction *rjmp rB* to Y86 instruction sets. It will jmp to the address stored in *rB*.
1. Fill in the function of each stage for *rjmp rB* instructionin Y86 sequential implementation. (NOTE: use *valB* to update PC)

2. As shown in the new PIPE logic figure, we add a forwarding logic from *E_valB* to *f_pc* to support *rjmp* instruction, since the target address require read from register file. Please describe all possible hazards due to new instruction *rjmp*. You need provide detail explanation and list detection conditions like Figure 4.64 and control action like Figure 4.66. (Do not consider the hazard combinations here.)

3. Please list all hazard combinations (arise simultaneously) including *rjmp* instruction. You need draw pipeline states figures like Figure 4.67 and list pipeline control action like tables after Figure 4.67 for each combination.

4.The original PIPE implementation of Y86 should be modified to support the *rjmp* instruction. Please describe the modification and provide HCL of *f_pc* and *D_bubble* logic. (NOTE: Only need to write the code about *rjmp* instruction)

2 Signal

```
1  int counter = 2;
2
3  void handler1(int sig) {
4      counter = counter + 1;
5      printf("%d\n", counter);
6      exit(0);
7  }
8
9  int main() {
10     signal(SIGINT, handler1);
11     printf("%d\n", counter);
```

```
12      if ((pid = fork()) == 0) {
13          while(1) {};
14      }
15      kill(pid, SIGINT);
16
17      counter = counter -1;
18      printf("%d\n", counter);
19      waitpid(-1, NULL, 0);
20      counter = counter + 1;
21      printf("%d\n", counter);
22      exit(0);
23  }
```

1. Please rewrite the *handler* according to the guidelines in section 8.5.5 (HINT: you can use *Sio_puts* as thread safe *printf* if needed).

2. Please write down all the possible outputs of the original programs.