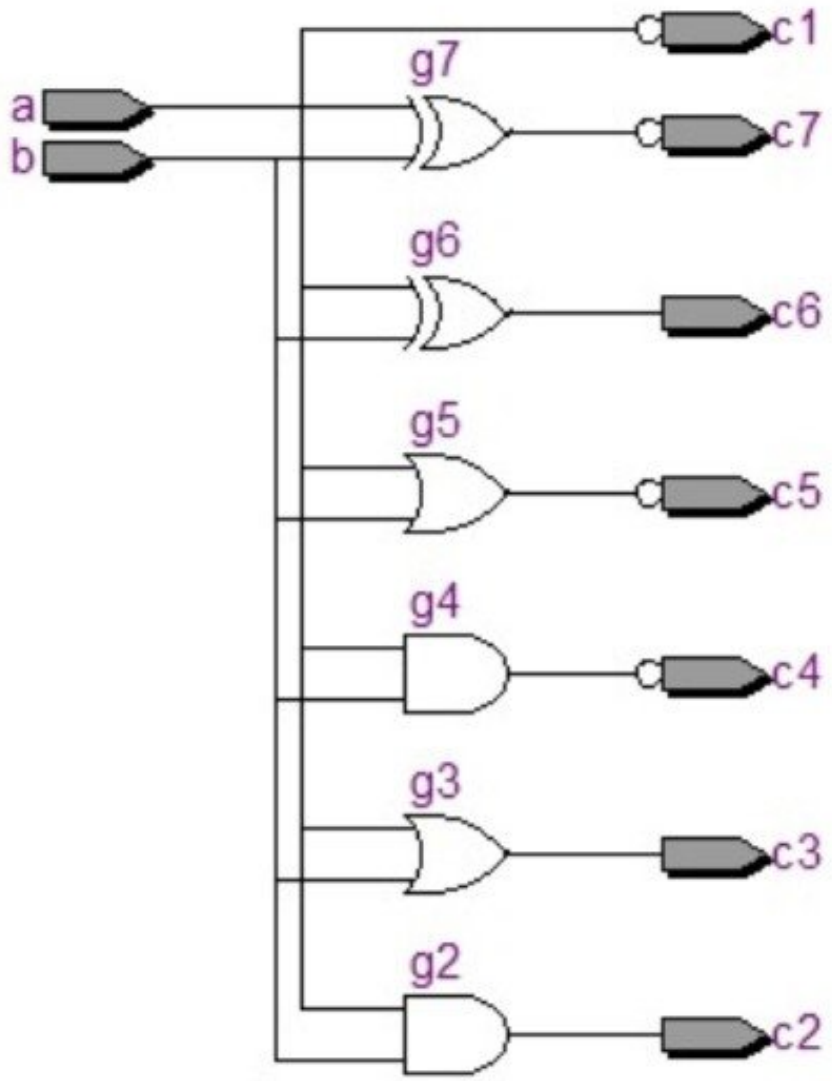
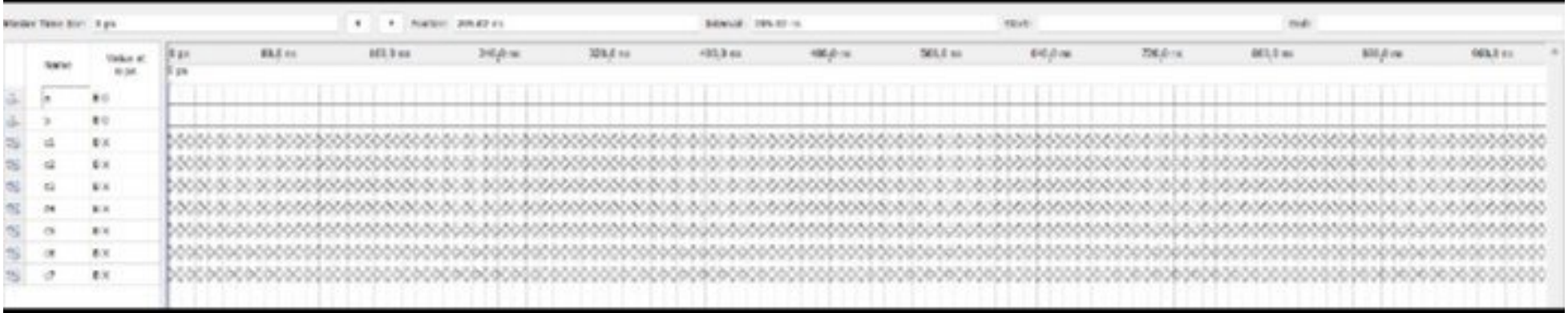

a
b
g7
c1
c7
g6
c6
g5
c5
g4
c4
g3
c3
g2
c2



```
1   module exp1(a,b,c1,c2,c3,c4,c5,c6,c7);
2   input a,b;
3   output c1,c2,c3,c4,c5,c6,c7;
4   not g1(c1,a);
5   and g2(c2,a,b);
6   or g3(c3,a,b);
7   nand g4(c4,a,b);
8   nor g5(c5,a,b);
9   xor g6(c6,a,b);
10  xnor g7(c7,a,b);
11  endmodule
```