

RL78 Microcontrollers

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Flash Data Library Type 04

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Introduction

This application note is written for users who want to understand the flash data library type 04 functions of the RL78 microcontrollers to design application systems using the products.

The purpose of this application note is to provide an understanding of how to use the flash data library type 04 used to rewrite the data flash memory of the RL78 microcontroller.

Target Devices

RL78/G12, RL78/G13, RL78/F12, RL78/I1A

Flash Data Library Type 04

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CHAPTER 1 OVERVIEW

1.1 Overview

The flash data library is a software library to perform operations to the data flash memory with the firmware installed on the RL78 microcontroller.

The flash data library performs rewriting and reading of the data flash memory when called from the user program. Use this application note with the user's manual of the target RL78 microcontroller

Terms The meanings of the terms used in this application are described below.

Flash data library

Library for data flash memory operations with the functions provided by the RL78 microcontroller.

It cannot perform operation to the code flash memory.

· Flash self-programming library

Library for code flash memory operation with the functions provided by the RL78 microcontroller.

Operation to the data flash memory cannot be done.

• EEPROM emulation library

Library that provides functions to store data to the built-in flash memory like an EEPROM.

· Block number

Number that shows a block of the flash memory. It is the unit of erasure operation in the Flash Data Library Type 04.

· Internal verification

To check if the signal level of the flash memory cell is appropriate after writing to the flash memory. If an error occurs in internal verification, the device is determined as failed. However, if data erasure, data writing, and internal verification are performed and completed normally after the internal verification error, the device is determined as normal.

• FDL

Abbreviation of "Flash Data Library."

Sequencer

The RL78 microcontroller has a dedicated circuit for controlling the flash memory. In this document, this circuit is called the "sequencer."

· BGO (background operation)

State in which rewriting of the flash memory can be done while operating the user program by letting the sequencer to control the flash memory. For the overview and details, refer to "2.1 Hardware Environment" and "3.4 BGO (background operation)."

Status check

When the sequencer is used, the processing to check the state of the sequencer (state of control for the flash memory) with the program controlling the flash memory is required. In this document, the processing to check the state of the sequencer is called "status checking."

1.2 Calling Flash Data Library Type 04

To perform rewriting of the data flash memory with the Flash Data Library Type 04, the initialization processing for the Flash Data Library Type 04 and the functions corresponding to the functions used need to be executed from the user program by using the C language or assembly language.

Figure 1-1 shows the state transition diagram of the Flash Data Library Type 04. Figure 1-2 shows an example of the code flash memory rewriting flow by using the Flash Data Library Type 04.

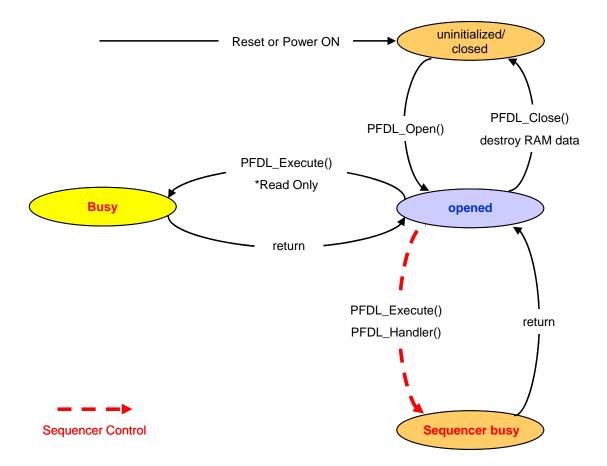


Figure 1-1. State Transition Diagram of Flash Data Library Type 04

[Overview of the state transition diagram]

To operate the data flash memory by using the Flash Data Library Type 04, the provided functions need to be executed sequentially to perform processing.

(1) uninitialized/closed

State at Power ON and Reset. To execute the flash self-programming library, EEPROM emulation library, flash data library other than Type 04, STOP command, or HALT command, execute PFDL_Close from the opened state to cause a transition to this state.

(2) opened

State in which the PFDL_Open() function has been executed from the uninitialized / closed state and the flash data library can be executed. In the period from the execution of PFDL_Close to the transition to the uninitialized / closed state, the flash self-programming library, EEPROM emulation library, flash data library other than Type 04, STOP command, or HALT command cannot be executed.

(3) busy

State in which the specified processing is being executed. The control does not return to the user program until the processing is completed.

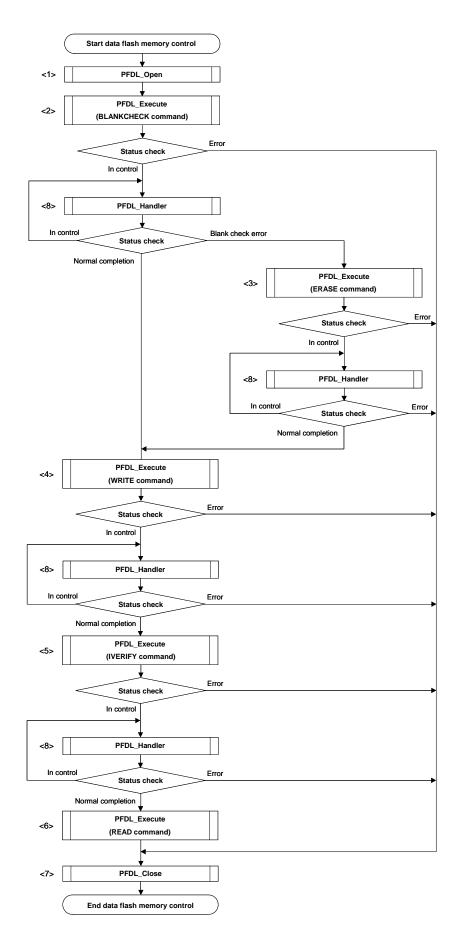
(4) sequencer busy

State in which the specified processing is being executed with the sequencer. The PFDL_Execute function specifies the details of control to the data flash memory, and the PFDL_Hander function performs a status check. The executed function returns to the user program without waiting for the completion of sequencer operation. The code flash memory cannot be referred to while the sequencer is being used.

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4 Operation

Figure 1-2. Example of Flow of Flash Data Library Type 04 Operation



- <1> Initializing and starting the RAM used for the Flash Data Library Type 04
 The PFDL_Open function is called to initialize the RAM used for the Flash Data Library Type 04 to enable the Flash Data Library Type 04.
- <2> Blank checking 1 to 1024 bytes for the specified address (PFDL_CMD_BLANKCHECK_BYTES command)
 The PFDL_Execute function (with the PFDL_CMD_BLANKCHECK_BYTES command specified) is called to
 perform blank checking of 1 to 1024 bytes for the specified address. The processing cannot be executed
 across blocks.
- <3> Erasing the specified block (1 KB) (PFDL_CMD_ERASE_BLOCK command)
 The PFDL_Execute function (with the PFDL_CMD_ERASE_BLOCK command specified) is called to erase the specified block (1 KB).
- <4> Writing 1 to 1024-byte data to the specified address (PFDL_CMD_WRITE_BYTES command)
 The PFDL_Execute function (with the PFDL_CMD_WRITE_BYTES command specified) is called to write 1 to 1024 bytes to the specified address. The processing cannot be executed across blocks.
- <5> Internal verification of 1 to 1024 bytes for the specified address (PFDL_CMD_IVERIFY_BYTES command)
 The PFDL_Execute function (with the PFDL_CMD_IVERIFY_BYTES command specified) is called to perform internal verification of 1 to 1024 bytes for the specified address. The processing cannot be executed across blocks.
- <6> Reading 1 to 1024 bytes for the specified address (PFDL_CMD_READ_BYTES command)
 The PFDL_Execute function (with the PFDL_CMD_READ_BYTES command specified) is called to read 1 to 1024 bytes for the specified address. All the processing of reading is executed within the PFDL_Execute function. The processing cannot be executed across blocks.
- <7> Ending the Flash Data Library Type 04
 The PFDL_Close function is called to end the Flash Data Library Type 04.
- <8> Status checking

The PFDL_Handler function is called to perform status checking. Status checking must be performed until the control to the data flash memory by the sequencer is finished.

CHAPTER 2 PROGRAMMING ENVIRONMENT

This chapter describes the hardware environment and software environment required to rewrite the data flash memory using the Flash Data Library Type 04.

2.1 Hardware Environment

The Flash Data Library Type 04 of the RL78 microcontroller uses the sequencer to execute rewrite control of the data flash memory. Because the sequencer performs the control to the data flash memory, the user program can be operated during data flash memory control. This is called BGO (background operation).

During rewriting of the data flash memory, the data flash memory cannot be referred to. However, the code flash memory can be referred to, so interrupt processing, user program, and Flash Data Library Type 04 can be allocated in the ROM for operation as usual.

Figure 2-1 shows the state during a rewrite of the data flash memory. Figure 2-2 shows an example of execution of the flash data library function to perform rewriting of the data flash memory.

On-chip RAM

Data flash memory

Reading cannot be executed during data flash memory control.

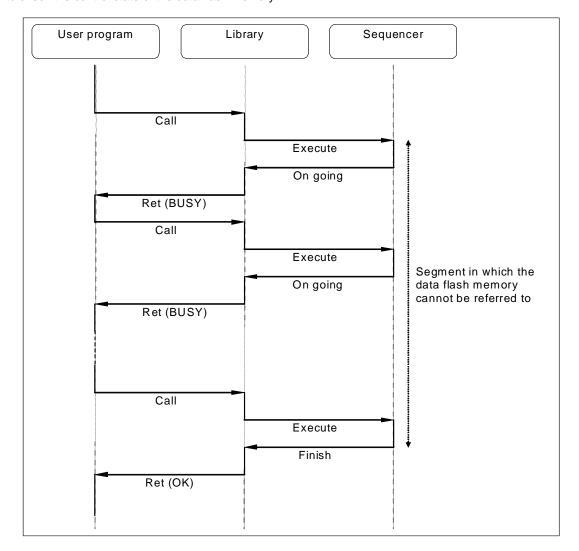
Code flash memory

Interrupts can be used as usual.

Figure 2-1. State During Rewrite of Data Flash Memory

Figure 2-2. Example Rewrite Control of Data Flash Memory

•After an execution request of the corresponding processing is made to the sequencer of the RL78 microcontroller, the control is immediately returned to the user program. For the result of the control to the data flash memory, the status check function (PFDL_Handler function) must be called from the user program to check the control state of the data flash memory.



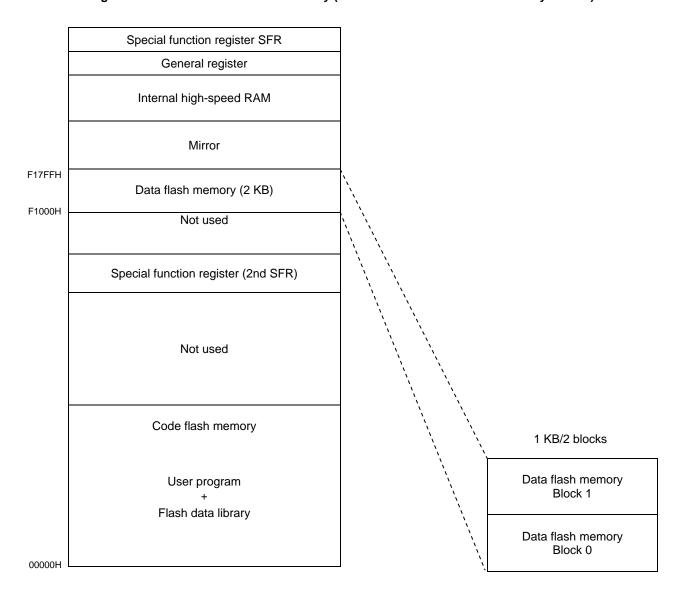
2.1.1 Blocks

The flash memory of the RL78 microcontroller is divided into 1-KB blocks. In the flash data library, erasure processing is performed for the data flash memory in the units of the blocks.

For reading, writing, blank checking or internal verification, specify the start address and execution size for execution.

Figure 2-3 shows an example of block positions and block numbers of the data flash memory.

Figure 2-3. Blocks of Data Flash Memory (RL78/G12: When Data Flash Memory Is 2 KB)



2.2 Software Environment

In the Flash Data Library Type 04, a program area of the size of the library used is consumed because the program is allocated in the user area. The Flash Data Library Type 04 itself uses the CPU, stack, and data buffer.

For the required software resources, refer to the document "Precautions for use" attached to the installer.

2.2.1 Self-RAM

The Flash Data Library Type 04 may use a RAM area of 1 KB as the working area. If it is used, the area is called the "self-RAM." It is defined within the library, so no user setting is required.

When the Flash Data Library Type 04 function is called, the data in the self-RAM area is rewritten

The availability of the self-RAM area and its size used for the Flash Data Library Type 04 vary depending on the product. For details, refer to the document "Precautions for use" attached to the installer.

2.2.2 Register bank

The Flash Data Library Type 04 uses the general register, ES/CS register, SP, and PSW of the register bank selected by the user.

2.2.3 Stack and data buffer

The Flash Data Library Type 04 uses the sequencer to write to the code flash memory, but it uses the CPU for pre-setting and control. Therefore, to use the Flash Data Library Type 04, the stack specified by the user program is also required.

Remark To allocate the stack and data buffer to the user-specified address, the link directive is used.

Stack

In addition to the stack used by the user program, the stack space required for flash functions must be reserved in advance, and they must be allocated so that the RAM used by the user will not be destroyed in stack processing during Flash Data Library Type 04 operation. The available range for stack specification is the self-RAM and the built-in internal ROM except for FFE20H to FFEFFH.

For stack space required for the flash data library functions, refer to the document "Precautions for use" attached to the installer.

· Data buffer

The uses of the data buffer are as follows.

- Work area for internal processing of the Flash Data Library Type 04
- Area in which data to be written is located during the execution of writing
- Area in which data to be obtained is located during the execution of reading

The available range for the beginning address of the data buffer is the self-RAM and the built-in internal ROM except for FFE20H to FFEFFH, as in the stack.

2.2.4 Flash Data library

Not all the flash data library functions are linked. Only the flash data library functions to be used are linked. Only the flash data library functions to be used are linked.

•Memory allocation of the Flash Data Library Type 04

Segments are assigned to the functions and variables used in the Flash Data Library Type 04. Areas used in the Flash Data Library Type 04 can be specified to the specific locations.

For details, refer to "3.2 Segments of Flash Data Library Functions," or refer to the document "Precautions for use" attached to the installer.

Note For the assembly language, linking can be done only for the flash data library functions to be used by deleting unnecessary functions from the include file.

2.2.5 Program area

This is the area in which the Flash Data Library Type 04 and the user program using the Flash Data Library Type 04 are allocated.

In the Flash Data Library Type 04 of the RL78 microcontroller, the user program can be operated during rewriting of the data flash memory because the data flash memory is rewritten by using the sequencer (background operation).

For details, refer to the sections of CHAPTER 3 "FLASH DATA LIBRARY FUNCTIONS", or refer to the document "Precautions for use" attached to the installer.

2.3 Cautions on Programming Environment

- (1) Do not execute the flash self-programming library, EEPROM emulation library, or flash data library other than Type04 during the execution of the Flash Data Library Type 04. When using the flash self-programming library, EEPROM emulation library, or flash data library other than Type04, always execute to PFDL_Close to close the flash data library.
- (2) Do not execute the STOP command mode or HALT command mode during the execution of the Flash Data Library Type 04. If the STOP command or HALT command needs to be executed, always execute to the PFDL_Close function to close the flash data library.
- (3) The watchdog timer does not stop during the execution of the Flash Data Library Type 04.
- (4) The data flash memory cannot be read during data flash memory operation by the Flash Data Library Type 04.
- (5) Do not allocate the argument (data buffer) or stack used in the flash data library function to an address over 0xFFE20 (0xFE20).
- (6) When using the data transfer controller (DTC) during the execution of the Flash Data Library Type 04, do not allocate the RAM area used by the DTC to the self-RAM or an address over 0xFFE20 (0xFE20).
- (7) Do not use the RAM area (including self-RAM) used by the Flash Data Library Type 04 until flash data library is complete.
- (8) Do not execute a flash data library function within interrupt processing because the Flash Data Library Type 04 does not support multiple executions of a flash data library function.
- (9) When executing the Flash Data Library Type 04 on the operating system, do not execute a flash data library function from multiple tasks because the Flash Data Library Type 04 does not support multiple executions of a flash data library function.
- (10) Before starting the Flash Data Library Type 04, the high-speed on-chip oscillator (high-speed OCO) needs to be started.
- (11) Note the following regarding the operating frequency of the RL microcontroller and the operating frequency value set with the initialization function (PFDL_Open).
 - When a frequency below 4 MHz^{Note} is used as the operating frequency of the RL78 microcontroller, 1 MHz, 2 MHz, or 3 MHz can be used (a frequency such as 1.5 MHz that is not an integer value cannot be used). Also, set an integer value such as 1, 2, or 3 as the operating frequency value set with the initialization function.
 - When a frequency over 4 MHz^{Note} is used as the operating frequency of the RL78 microcontroller, a frequency with decimal places can be used. However, set a rounded up integer value as the operating frequency set with the , initialization function (PFDL_Open).

(Example: For 4.5 MHz, set "5" with the initialization function.)

Note For the range of the maximum operating frequency, refer to the user's manual of the target RL78 microcontroller.

(12) The Flash Data Library Type 04 does not perform error checking of the parameters set in the argument of a flash data library function. Therefore, make sure to set a correct value to the parameter after checking the specifications of the target RL78 microcontroller. If parameter checking is required to set a correct value, perform it in the user program.

CHAPTER 3 FLASH DATA LIBRARY FUNCTION

This chapter describes the details of the flash data library functions.

3.1 Type of Flash Data Library Functions

The Flash Data Library Type 04 consists of the following flash functions.

Table 6-1. List of Flash Data Library Functions

Function name	Description
PFDL_Open	Initialization and starting of the RAM used for the Flash Data Library Type 04
PFDL_Close	Ending of the Flash Data Library Type 04
PFDL_Execute	Execution of control to the data flash memory
PFDL_Handler	Checking of the control state to the data flash memory and setting of continuous execution (status check processing)
PFDL_GetVersionString	Acquisition of the version information of the Flash Data Library Type 04

3.2 Segments of Flash Data Library Functions

The flash data library functions consist of the following segment.

•PFDL_COD: Segment of the flash data library function. They can be allocated to the ROM or RAM.

3.3 Commands

The details of operation of the Flash Data Library Type 04 to the data flash memory can be specified with a command in the argument of the PFDL_Execute function. The commands specified in the PFDL_Execute function are shown below. For details on the execution method, refer to the section on the PFDL_Execute function.

Table 3-3. List of Commands Specified in PFDL_Execute Function

Definition	Value	Command name
PFDL_CMD_READ_BYTES	0x00	Read command
PFDL_CMD_BLANKCHECK_BYTES	0x08	Blank check command
PFDL_CMD_ERASE_BLOCK	0x03	Erasure command
PFDL_CMD_WRITE_BYTES	0x04	Write command
PFDL_CMD_IVERIFY_BYTES	0x06	Internal verification command

3.4 BGO (Background Operation)

The flash data library functions can be divided into functions that do not use the sequencer and functions that use the sequencer Note. For the functions that use the sequencer BGO (background operation) can be performed.

The following figures show examples of operation of the Flash Data Library Type 04 during BGO. The table shows a list of the functions with the presence of sequencer control.

Note Not during the execution of the PFDL_CMD_READ_BYTES command.

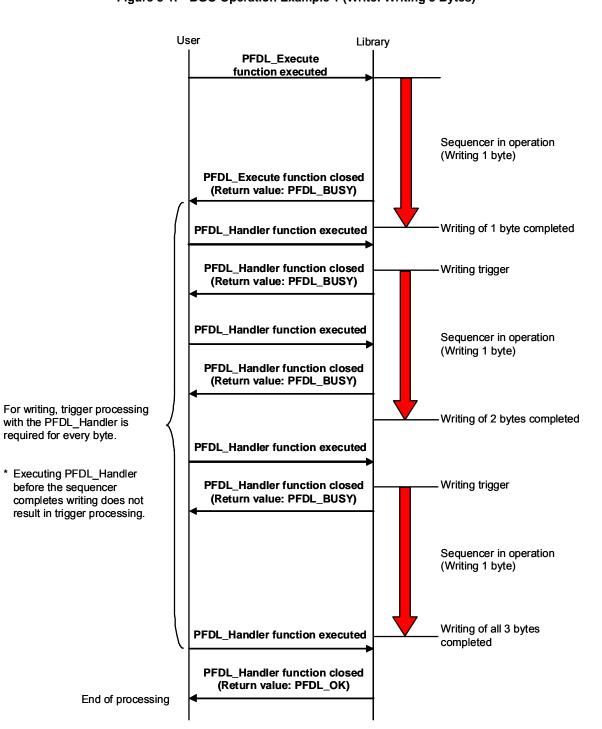


Figure 3-1. BGO Operation Example 1 (Write: Writing 3 Bytes)

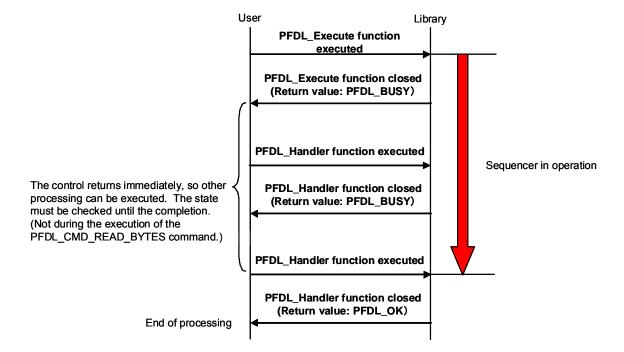


Figure 3-2. BGO Operation Example 2 (Erase, Iverify, BlankCheck)

Table 3-4. List of Interrupt Reception and BGO of Flash Data Library Functions

Function name	Sequencer control/BGO function	Interrupt reception
PFDL_Open	No	
PFDL_Close	INO	
PFDL_Execute	Yes ^{Note}	Allowed
PFDL_Handler	168	
PFDL_GetVersionString	No	

Note Not during the execution of the PFDL_CMD_READ_BYTES command.

3.5 List of Data Types, Return Values, and Return Types

The data types are as follows.

Table 3-5. List of Data Types

Definition	Data type	Description
pfdl_u08	unsigned char	1-byte (8-bit) unsigned integer
pfdl_u16	unsigned int	2-byte (16-bit) unsigned integer
pfdl_u32	unsigned long int	4-byte (32-bit) unsigned integer

The meaning of each return value is as follows.

Table 3-6. List of Return Values

Definition	Return	Description
	value	
PFDL_OK	0x00	Normal completion
PFDL_ERR_ERASE	0x1A	Erasure error
		- Erasure of the target area failed.
PFDL_ERR_MARGIN	0x1B	Blank check error or Internal verification error
		- The target area is not in the blank state.
		- An error occurred during internal verification processing of the
		target area.
PFDL_ERR_WRITE	0x1C	Writing error
		- Writing to the target area failed.
PFDL_IDLE	0x30	Idle state
		- No command is executed in the PFDL_Execute function.
PFDL_BUSY	0xFF	Execution start of the PFDL_Execute function command, or in
		execution
		- The command specified in the PFDL_Execute function is in
		execution.
Other than above	Other	Other error
	than	- An abnormal return value. Check the specified command or
	above	resource allocation again.

The return types are as follows.

Table 6-8. List of Return Types

	Return value		
	C language	Assembly language	
RENESAS Small and medium model	pfdl_u08	С	
RENESAS Large model			

3.6 Description of Flash Data Library Functions

The flash functions are described in the following format.

Flash data library function name

[Overview]

Describes the function overview of this function.

[Format]

<C language>

Describes the format to call this function from a user program described in the C language.

<Assembler>

Describes the format to call this function from a user program described in the assembly language.

[Presetting]

Describes the presetting of this function.

[Function]

Describes the function details and cautions of this function.

[Register State After Call]

Describes the register state after this function is called.

[Argument]

Describes the argument of this function.

[Return Value]

Describes the return values from this function.

PFDL_Open

[Overview]

Initialization and starting of the RAM used for the flash data library

[Format]

<C language>

```
pfdl_status_t __far PFDL_Open( __near pfdl_descriptor_t* descriptor_pstr )
```

<Assembler>

```
CALL !_PFDL_Open or CALL !!_PFDL_Open
```

Remark Call with "!" when the flash data library is allocated at 00000H to 0FFFFH, or call with "!!" otherwise.

[Presetting]

- The flash self-programming library, program and flash data library to operate the data flash memory, and EEPROM emulation library are not executed or have been ended.
- The high-speed on-chip oscillator (high-speed OCO) is running.

[Function]

- Reserves, initializes and starts processing of the self-RAM used for the Flash Data Library Type 04. If a self-RAM^{Note 1} exists, do not use it until the Flash Data Library Type 04 is finished.
- Define the voltage mode Note 2 of the Flash Data Library Type 04 in the pfdl_flash_voltage_u08, a structure member of the argument pfdl descriptor t.

00H: Full-speed mode

Other than above: Wide voltage mode

• Set the operating frequency of the CPU in the pfdl_frequency_u08, a structure member of the argument pfdl_descriptor_t. The setting value is used for the calculation of timing data in the Flash Data Library Type $04^{\text{Note 3}}$.

For the value of the operating frequency of the CPU (pfdl_frequency_u08), note the following.

- When a frequency below 4 MHz^{Note 4} is used as the operating frequency of the RL78 microcontroller, 1 MHz, 2 MHz, or 3 MHz can be used (a frequency such as 1.5 MHz that is not an integer value cannot be used). Also, set an integer value such as 1, 2, or 3 as the operating frequency value set with the initialization function.
- When a frequency over 4 MHz^{Note 4} is used as the operating frequency of the RL78 microcontroller, a frequency with decimal places can be used. However, set a rounded up integer value as the operating frequency set with the initialization function (PFDL_Open).

(Example: For 4.5 MHz, set "5" with the initialization function.)

- **Notes 1.** For the self-RAM, refer to the document "Precautions for use" attached to the installer, or refer to the user's manual of the target RL78 microcontroller.
 - 2. For details of the voltage mode, refer to the user's manual of the target RL78 microcontroller.
 - **3.** It is a required parameter for timing calculation in the flash self-programming library. This setting does not change the operating frequency of the RL78 microcontroller.
 - 4. For the range of the maximum operating frequency, refer to the user's manual of the target RL78

microcontroller.

[Register State After Call]

Development tool	Return value	Destructed register
RENESAS	С	AX

[Argument]

Argument	Description		
near pfdl_descriptor_t* descriptor_pstr	Initial setting value of the Flash Data Library Type 04 (voltage mode, CPU		
	frequency)		

The content of __near pfdl_descriptor_t*

Structure member	Description
pfdl_u08 pfdl_flash_voltage_u08	Setting of the voltage mode
pfdl_u08 pfdl_frequency_u08	CPU frequency during the execution of the Flash Data Library Type 04

	Argument Type/Register		
	C language	Assembly language	
RENESAS Small and medium model	pfdl_descriptor_t *descriptor_pstr	AX (0 to 15)	
RENESAS Large model	pfdl_descriptor_t *descriptor_pstr	AX (0 to 15)	

State	Description
0x00(PFDL_OK)	Normal completion
	- Initial setting is complete (there is no parameter other than normal completion)

PFDL_Close

[Overview]

Ending of the flash data library

[Format]

<C language>

void PFDL_Close(void)

<Assembler>

CALL !_PFDL_Close or CALL !!_PFDL_Close

Remark Call with "!" when the flash self-programming library is allocated at 00000H to 0FFFFH, or call with "!!" otherwise.

[Presetting]

Before the execution of this function, the PFDL_Open function must be completed normally.

[Function]

Ends operation to the data flash memory.

[Register State After Call]

The register is not destructed.

[Argument]

None

[Return Value]

None

PFDL_Execute

[Overview]

Execution of control to the data flash memory

[Format]

<C language>

pfdl_status_t __far PFDL_Execute(__near pfdl_request_t* request_pstr)

<Assembler>

CALL !_far PFDL_Execute Of CALL !!_far PFDL_Execute

Remark Call with "!" when the flash data library is allocated at 00000H to 0FFFFH, or call with "!!" otherwise.

[Presetting]

Before the execution of this function, the PFDL_Open function must be completed normally.

[Function]

Executes the control to the data flash memory according to the specified command.

[Register State After Call]

Development tool	Return value	Destructed register	
RENESAS	С	AX	

[Argument]

Argument	Description		
near pfdl_request_t* request_pstr	Specify the details of control to the data flash memory (command and setting		
	value).		

The content of __near pfdl_request_t *

Structure member	Description		
pfdl_u16 index_u16	Beginning address of the target area or block number Note		
	- Erasure: Block number		
	- Other than erasure: Beginning address of the target area		
near pfdl_u08* data_pu08	Pointer to the data buffer for acquisition of data to be written or read ^{Note}		
	Not used for processing other than writing/reading		
pfdl_u16 bytecount_u16	Execution range of the command (byte specification) ^{Note}		
	- Erasure: No specification is required.		
	- Other than erasure: Range from the specified beginning address to the target area		
pfdl_command_t command_enu	Command to execute		

Note Specify it only for commands requiring the target parameter. Provide the data buffer size for the number of bytes of the data to be written or read.

List of Execution Commands (pfdl_command_t)

Command	Value	Description		
PFDL_CMD_READ_BYTES	0x00	Reads the data of the read size from the specified starting address of the data		
		flash memory to the read data input buffer.		
		*The following arguments must be set for execution.		
		•pfdl_request_t.index_u16: Reading start address		
		•pfdl_request_t.bytecount_u16: Read size ^{Note}		
		•pfdl_request_t.data_pu08: Address of the read data input buffer		
PFDL_CMD_BLANKCHECK_BYTES	0x08	Performs blank checking from the specified beginning address of the data		
		flash memory for the area in the execution range.		
		*The following arguments must be set for execution.		
		•pfdl_request_t.index_u16: Start address		
		•pfdl_request_t.bytecount_u16: Execution range from the start address ^{Note}		
PFDL_CMD_ERASE_BLOCK	0x03	Performs erasure for the block of the specified number in the data flash		
		memory.		
		*The following arguments must be set for execution.		
		•pfdl_request_t.index_u16: Block number		
PFDL_CMD_WRITE_BYTES	0x04	Writes the data inputted in the write data input buffer to the data flash memory		
		from the specified starting address for the write size.		
		*The following arguments must be set for execution.		
		•pfdl_request_t.index_u16: Write start address		
		•pfdl_request_t.bytecount_u16: Write size ^{Note}		
		•pfdl_request_t.data_pu0: Address of the write data input buffer		
PFDL_CMD_IVERIFY_BYTES	0x06	Performs internal verification from the specified beginning address of the data		
		flash memory for the area in the execution range.		
		*The following arguments must be set for execution.		
		•pfdl_request_t.index_u16: Start address		
		•pfdl_request_t.bytecount_u16: Execution range from the start address ^{Note}		

Note It cannot be specified across blocks. Specify it within one block

State	Description		
0x00(PFDL_OK)	Normal completion		
0x1A(PFDL_ERR_ERASE)	Erasure error		
	- An error occurred during erasure processing.		
0x1B(PFDL_ERR_MARGIN)	Blank check error or internal verification error		
	- The target area is not in the blank state.		
	- An error occurred during internal verification processing of the target area		
0x1C(PFDL_ERR_WRITE)	Writing error		
	- An error occurred during write processing.		
0xFF(PFDL_BUSY)	Execution start of the specified command		
	- The execution of the specified command has been started.		
	(Check the execution state with the PFDL_Handler function.)		

PFDL_Handler

[Overview]

Checking of the control state to the data flash memory and setting of continuous execution (status check processing)

[Format]

<C language>

```
pfdl_status_t __far PFDL_Handler( void )
```

<Assembler>

```
CALL !_PFDL_Handler or CALL !!_PFDL_Handler
```

Remark Call with "!" when the flash data library is allocated at 00000H to 0FFFFH, or call with "!" otherwise.

[Presetting]

Before the execution of this function, the PFDL_Open function must be completed normally.

[Function]

Checks the control state of the command specified in the PFDL_Execute function just executed and performs required settings for continuous execution.

[Register State After Call]

Development tool	Return value	Destructed register	
RENESAS	С	_	

[Argument]

None

State	Description		
0x00(PFDL_OK)	Normal completion		
0x1A(PFDL_ERR_ERASE)	Erasure error		
	- An error occurred during erasure processing.		
0x1B(PFDL_ERR_MARGIN)	Blank check error or internal verification error		
	- The target area is not in the blank state.		
	- An error occurred during internal verification processing of the target area		
0x1C(PFDL_ERR_WRITE)	Writing error		
	- An error occurred during write processing.		
0x30(PFDL_IDLE)	Idle state		
	- No command is executed in the PFDL_Execute function.		
0xFF(PFDL_BUSY)	Command in execution		
	- The command specified in the PFDL_Execute function is being executed.		

PFDL_GetVersionString

[Overview]

Acquisition of the version information of the Flash Data Library Type 04

[Format]

<C language>

```
__far pfdl_u08* __far PFDL_GetVersionString( void )
```

<Assembler>

```
CALL !_PFDL_GetVersionString Of CALL !!_PFDL_GetVersionString
```

Remark Call with "!" when the flash data library is allocated at 00000H to 0FFFFH, or call with "!!" otherwise.

[Presetting]

None

[Function]

Obtains the version information of the Flash Data Library Type 04.

[Register State After Call]

Development tool	Return value	Destructed register	
RENESAS	BC (0 to 15), DE (16 to 31)	_	

[Argument]

None

Data type	Description			
pfdl_u08*	Beginning address of the area where the version information of the Flash Data Library Type 04 is stored (24-byte area) Example: Flash Data Library Type 04 "DRL78T04R110GVxxx" Version information: Example: V104 → V1.04 Supported tool: RENESAS Type name: Type 04 Supported device: RL78 Target library: FDL			

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Revision Record

		Description		
Rev.	Date	Page	Summary	
1.00	Jun 30, 2011	_	First edition issued	

NOTES FOR CMOS DEVICES

- (1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) INPUT OF SIGNAL DURING POWER OFF STATE: Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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