CS2160 Computer Organisation Laboratory

Lab6 Report

Vaibhav B. Nagrale 112001046
Thogata Jagadeesh 112001045

The configurations of the caches are as follows:

Cache size	:	4B / 8B / 32B / 128B / 1kB
Latency	:	1 cycle / 2 cycles / 4 cycles / 8 cycles / 12 cycles
Line Size	:	4B
Associativity	:	1
Write Policy	:	Write Through

Observation :

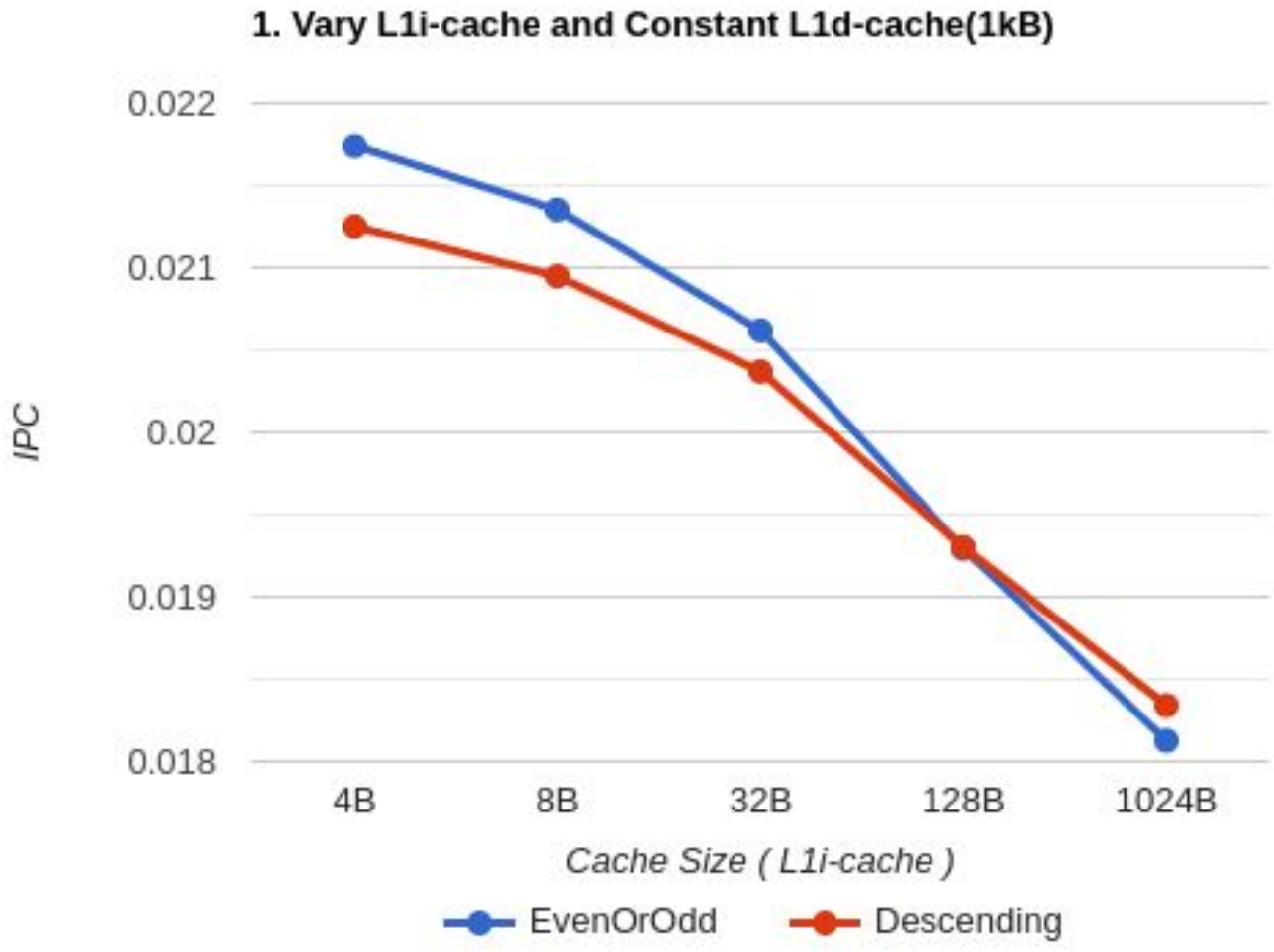
Cache Size ——————>

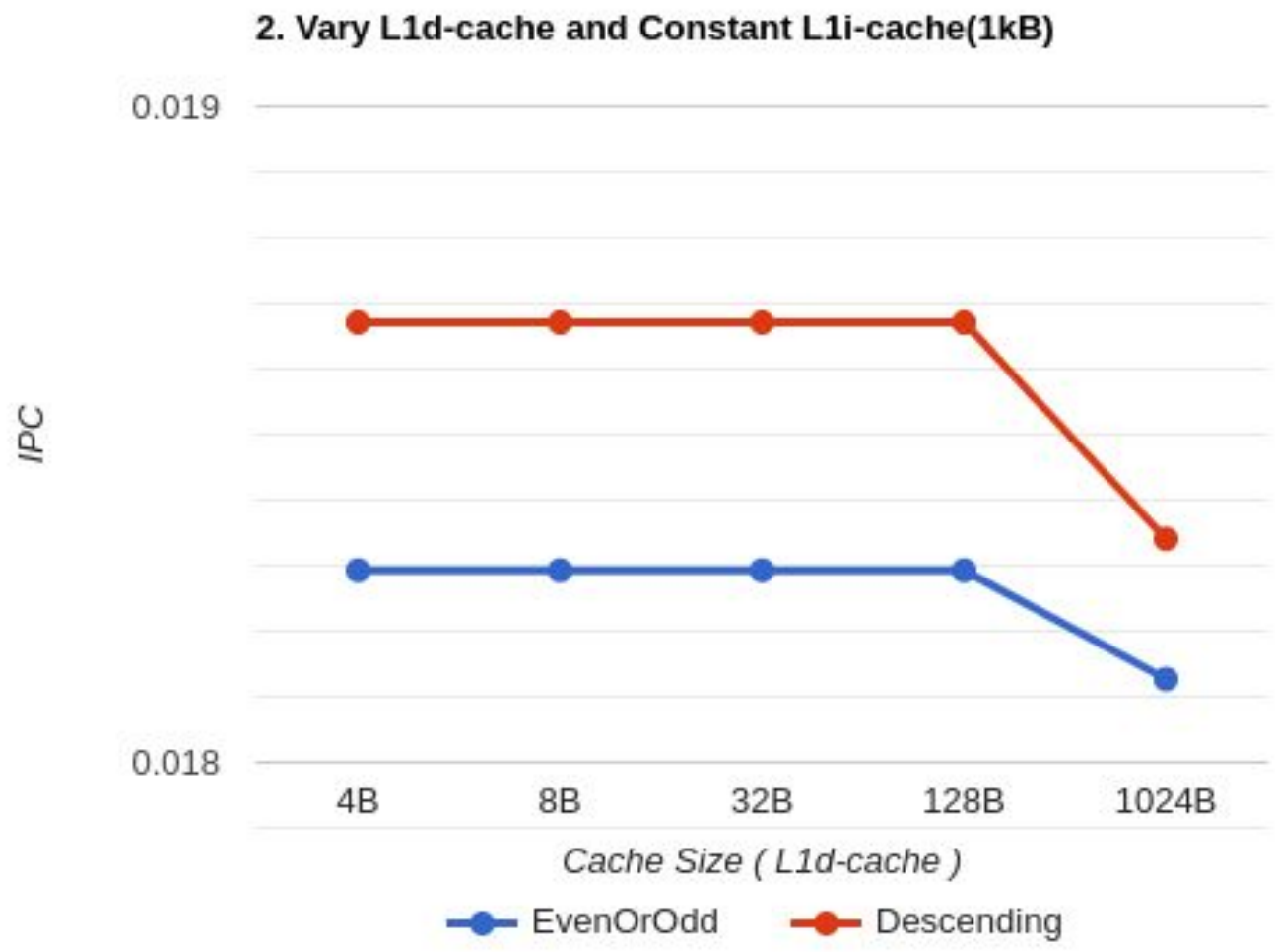
Fix L1d(1kB) Vary L1i

Fix L1i(1kB) Vary L1d

	4B	8B	32B	128B	1kB
EvenOrOdd	0.02173913	0.021352313	0.020618556	0.019292604	0.018126888
Descending	0.021250479	0.020948347	0.020369144	0.01930179	0.018340727
EvenOrOdd	0.018292682	0.018292682	0.018292682	0.018292682	0.018126888
Descending	0.018670801	0.018670801	0.018670801	0.018670801	0.018340727

IPC for different Cache Size


1. Vary L1i-cache and Constant L1d-cache(1kB)
0.022
0.021
0.02
0.019
0.018
IPC
4B
8B
32B
128B
1024B
Cache Size (L1i-cache)
EvenOrOdd
Descending


2. Vary L1d-cache and Constant L1i-cache(1kB)
0.019
0.018
IPC
4B
8B
32B
128B
1024B
Cache Size (L1d-cache)
EvenOrOdd
Descending

Observation :

- When we vary L1i-Cache and fix L1d-Cache(1kB) IPC was decreasing for all given observations.
- When we vary L1d-Cache and fix L1i-Cache(1kB) IPC was constant and decreased by small amount for larger(L1d = 1kB) .
- On increasing cache size the latency of the cache increases and hence the IPC will decrease.