PUNE INSTITUTE OF COMPUTER TECHNOLOGY
DHANKAWADI, PUNE – 43.
Department of Computer Engineering

Academic Year: 2018-19 (Semester-I)

UNIT TEST II

Year: S.E.

Subject: Digital Electronics & Logic Design

Time: - 1 Hour Max. Marks: - 30

Instructions to the candidates:-

All Questions are compulsory.

Q. No.	Sub. Q. No.	Question	Marks	Unit No.	Cos Covered	CO Mapping
1.	A	Design 3-bit synchronous counter using T filp-flop.	6	2	CO1, CO2	H H
	B	Design a sequence detector logic circuit using MS- JK flip flop for the pattern 101. (use melay model)	4	2	CO1, CO2, CO3	H H H
2.	A	State and explain basic components of ASM chart. Draw ASM chart for MOD 3 UP counter.	6	3	CO2	H
	B	Write VHDL code for full adder using data flow modeling style..	4	3	CO2, CO4	H H
3.	A	Implement 3 bit binary to gray code converter using PLA.	6	4	CO1, CO2	H H
	B	A combinational Circuit is defined by the following F1(A,B,C) = m Σ (0,1,3,7) F2(A,B,C) = m Σ (1,2,5,6) Implement this circuit with PLA.	4	4	CO1, CO2	H H

*****ALL THE BEST*****