GROUP OF INSTITUTIONS			
	Stud	eriment No Date	
		Assignment-1	
		Introduction	
	>	VMC-850x series kit (VMC-8501/VMC-8502)	
	>	VMC-250X communicates with the outside	
		world through a key board having 28 keys 4	
_	>	Seven segment hexadecional display. VMC-850x provides & Kb / 32kb of RAMS.	
		can be very easily expanded to 64 Kb in an	
		appropriate Combination of RAII & Colo	
	7	poulrful software commands like to	
		INSERT, DELETE, MOVE etc.	
		adopted STD Bus which is the most populare bus for process control and real time applications.	
		bus for process who are and real time applications.	
		System Specification.	
		CPU -> 8 bit pl, 8085	
		MEMORY > 64Kb.  RAM > 8Kb/32Kb and space for further expansion	
		ROM -> 8Kb. of EPRUM. loaded with pourris prig.	
		TIMER -> 16 bit programmable counter using 8253.  I/O -> 24 I/O lines using 8255	
		Domer Supply >. + 5 V, 1.5 A for Rit.  ±12V+5%, 250mA for CRT/PC interface.	
		, of the	

JIET GROUP OF INSTITUTIONS		
	Ident Name	
	periment NoDate	
	Hardware Description.	
	General	
	The system has got 8085 as the CPV. The clock frequency for the system is 3.07MHz and is generated from as crystal of 6.14 MHz.	
	Memory	
	VMC-850x provides 8 Kb / 32 Kb of RAM using	
	VMC-850x provides 8 Kb/32 Kb of RAM using 6264/62256 Chip and 8 Kb of EPROM for monitor. Total onloard memory can be extended to 64 Kb.	
	I/O devices.	
	The various 40 chips used in VMC-8501 are 8279, 8255 & 8253 and VMC-8502 are 8279,	
	8255, 8253 & 8155 ···	
	8279 (Keyboard & Display Controller).	
	8279 is general purpose programmable klyboard	
	8279 (Keyboard & Display Controller). 8279 is general purpose programmable keyboard and display I/O interface device designed for use. With the 8085 M.	
	8255 (Programmable Peripheral Interface) (PPI)	
	This basically act as a algoral purpose I/Oderic	
	8255 (Programmable Peripheral Interface) (PPI) 8255 is a PPI designed to use with 8085 M. This basically act as a general purpose I/Odewic to interface peripheral equipments to the systems	

Page No. ....

# JIET GROUP OF INSTITUTIONS

dent Name
Rest of the generation of accurate and can be used for the generation of accurate time delays under software control.  BIS 5. (Programmable I/O port of timer interface).  BIS 5 is a programmable I/O ports and timer interface designed to use with 8085 µl. The RIS 5 includes 256 bytes of R/W memory, three I/O ports and a timer.  Display.  VMC - 850x provides six digits of seven segment display. Four digits are for displaying the address of any locations or name of any register, whereas the rest of the two digits are meant for displaying the contents of a memory location or of a register. They are displayed in hexaclumal notation.
Page No

## JIET GROUP OF INSTITUTIONS Keyboard Description: 20 Keys Model Reset -> Reset the system RESET VET VCT INT -> Hardware interrupt via keyboard RST75 SHIFT -> Provides a second level command to all keys 60 - To execute the program 7 SI -> To execute the program in single step mode. 5 SPL EXREG -> Examine register, allows user to examine and modify the contents of different STRING MEMO registers EXMEM > Examine Memory, allows user to examine any nemory location & modify any RAM location. PRE > Previous is used as an intermediate terminator of examine memory. NEXT > Increment is used as a intermediate examine register et command and write the data in data field at the location displayed in address field -> Delete the part of program or data, with relocation by one or more bytes. INS > Inserts the part of the program or data with relocation, by one or more bytes. B.M. ->. Allows user to mane a block of memory to any RAMasea. FILL > . Allows user to fill to RAM arequirth a constant. Page No. .

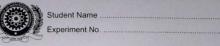
	RFL> Relocates a prog. woitten for some memory area and to be transferred to other memory
	area and to be transferred to other memory
	www.
	INS DATA > Inserts one or more data bytes in the.
	user's program/data area
	DEL DATA > Deletes one or more data bytes from
	the user's prog. I data area.
	STRING >. Finds out the string of data lying at a particular addresses
	MEMC > Memory Compare: compares funo
	blocks of memory for equality
	MEMC > Memory Compare: compares two blocks of memory for equality 0-F > Hexadecimal keys.
NAME OF THE PERSON OF THE PERS	
VIOLED IN	end to the alphable the data of a fine of the
Alexa a 3	white the first of the first of the first of

SHORTHITTAMI NO NUMBER OF INSTITUTIONS	Student Experience	JIET GROUP OF INSTITUTIONS  dent Name Roll No. Date 5/2/20
PACE		Assignment - 2
TRING STAND AND THE STAND OF THE STAND OF THE STAND OF THE STANDS OF THE STAND OF T	Hardvare. Reguirement	Microprocessor training bit
MENC - Minary Son and Employed	Program. Address.	Premonics. Hex (ode.
	2003	INX H 23.
	2006.	STA 3002. 32 HLT 76.
	Result 6	Input data: 3000 (1.  3001 22.  Output data: 3002 33
	Miva:	Q What are LXI, MOV, INX, ADD, STAFKLI Command?
ADD -> It adds the data of a given location with. content of Accumalates and stores the result in Accumalator.		UXI. → It is used to load data from memory location to a given Register pair.  MOV → To copy data from one registes
STA >. Transfer the content accumulator to a given.  Memory location.  HLT > To indicate end of program.		MOV > To copy data from one register to another.  INX > It increments the content of Register pair by 1.

# Viva: What is DAD and SHLD command? DAD > It is used to perform a 16 bit. addition the content of HL pair. SHLD > To store the content of HL pair. at a given location.

## JIET GROUP OF INSTITUTIONS

Date 5 2 / 2 / 2 0



	Assignment -3.			
Objective:	Add a, 16 bit numbers and sond result on another location.			
Hardware.	Micropsocessor training Kit.			
Requirement				
		A Table Ball	Charles and	
Program:			No. of Contract of	
	MNEMONIC.			
Address.	opcode.	operand.	Hex Code.	
2000	L×J	H. 0101.	21	
200			01	
2002			01	
2003	LXI	D 0101	- 11	
200 4.			01	
2005			01.	
2006	DAD SHLD.	D.	1.9.	
2007	SHLD.	2500.	22	
2008			00	
2009			25	
200R.	HLT.		76.	
Result:	Input data:	90101		
		0101		
	Destput data:	0202.		
			Page No	

Result: Input data. 7777

Output data 8.888

Viva: What is ADC command? How is it different from DAD?

It is used to add the content of register and accumalator and also accounts fore carry if generated, which is suid discarded in Case of DAD.

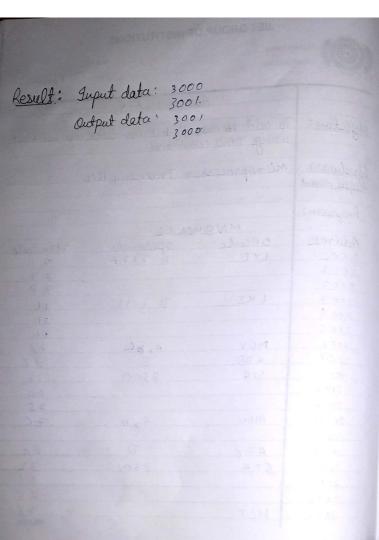
## JIET GROUP OF INSTITUTIONS



Student Name ..

Experiment No.

			· · · · · · · · · · · · · · · · · · ·	
	Assignment-4.			
Objective:	To add #5 two, 16 bit numbers was without using DAD command.			
Hardware. Requirement	Microprocess	or Training Ki	±	
Program:				
	MNE	MONIC.		
Address	OPCode.	operand.	Hex Coole	
2.000	LXI	H 7777	21.	
2001.			77	
2002			77.	
2003	LXI	D 1111	11	
2004			11	
2005			11.	
2006	MOV	A, BL	7.7	
2007	ADD	E	83	
2068	STA	2500	32	
2009			00	
200A			25	
200 B	mou	A , H	70.	
200 C				
200D	ADC.	D.,	8 A.	
200 €	STA	2501	32	
200 F			0!	
2016			25	
2017	HLT		76	
CUT			Page No.	



## **JIET GROUP OF INSTITUTIONS** Roll No. Assignment -5 Objective: To swap the contents of two memory location Hardware. Microprocessor training Kit Roquisement Program: MNEMONIC Of code operand Hex Code. Address LDA. 3 A.. 2000 00 2001 30 2002 B, A 47. 2003 MOV. 2004. 3 A. LDA 3001 2005 01 2006 32 STA 3000 2007 2008 00 2009 30 A,B MOV 78. 200A 200B STA 30001 32 01 200 €. HLT 26.30 200 D. 200'F 76. Page No. ....