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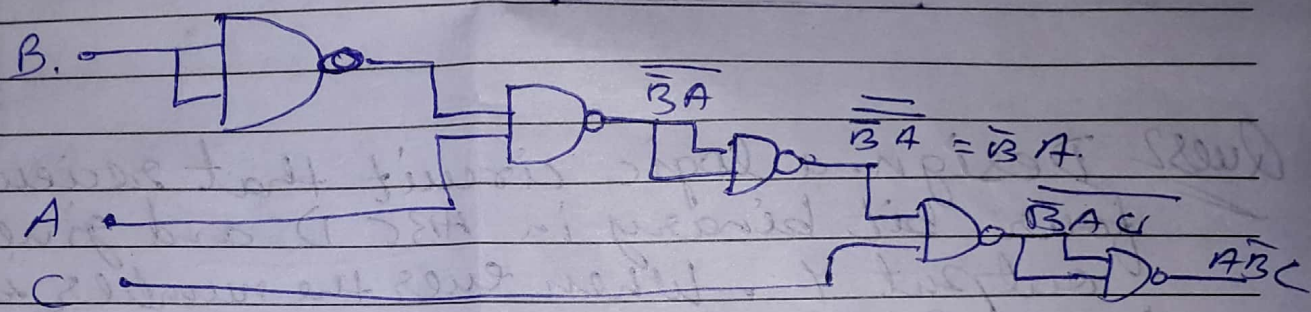
Student Name ..... Vaibhav Saran ..... Roll No.: .....

Experiment No. ..... Date .....

Q1 Implement the following expressions.

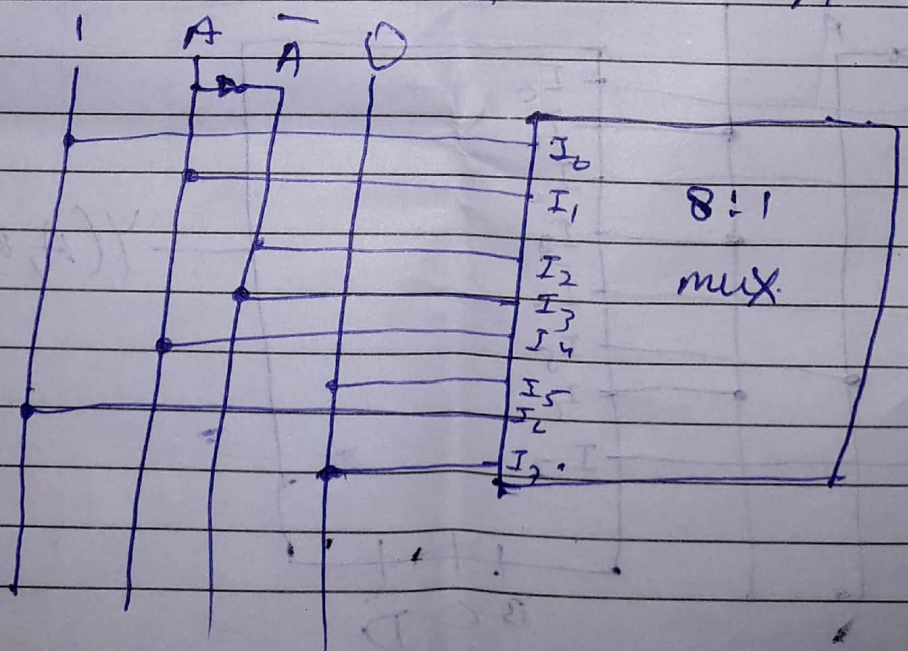
(a) $Y = A\bar{B}C$. using 2 input NAND gate only.



(b) $y = \Sigma m(0, 2, 3, 6, 8, 9, 12, 14)$ using multiplexer.

Here we use B, C, D as input lines and A as.

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	(0)	1	(2)	(3)	4	5	(6)	7
A	(8)	(9)	10	11	(12)	13	(14)	15
	1	A	$\bar{A}$	$\bar{A}$	A	0	0	0



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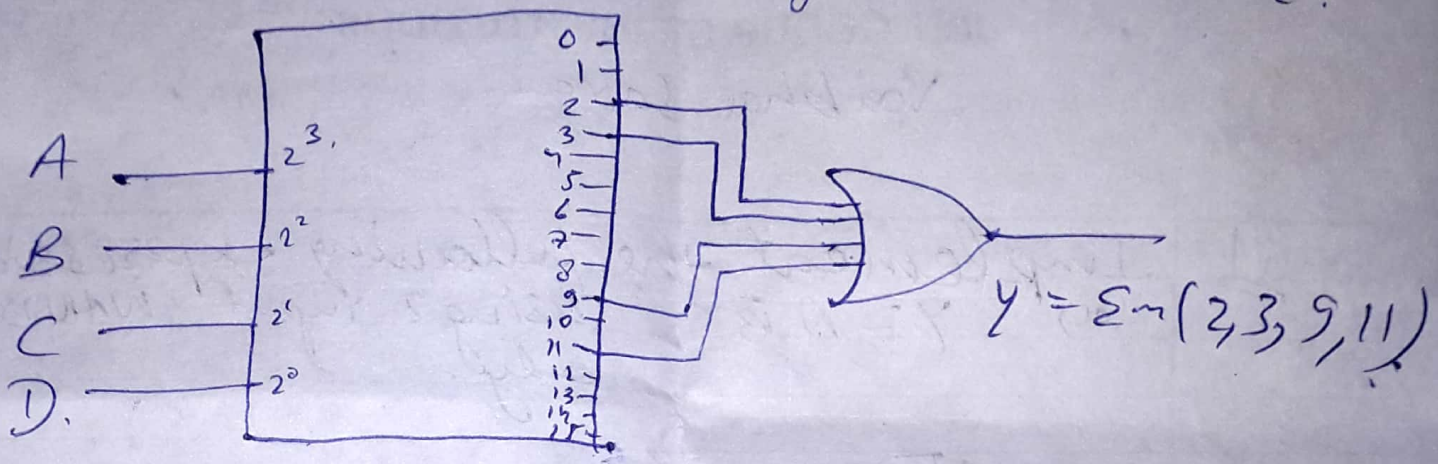
(c.) $Y = \Sigma m(2, 3, 9, 11)$ using 4 to 16 decoder.



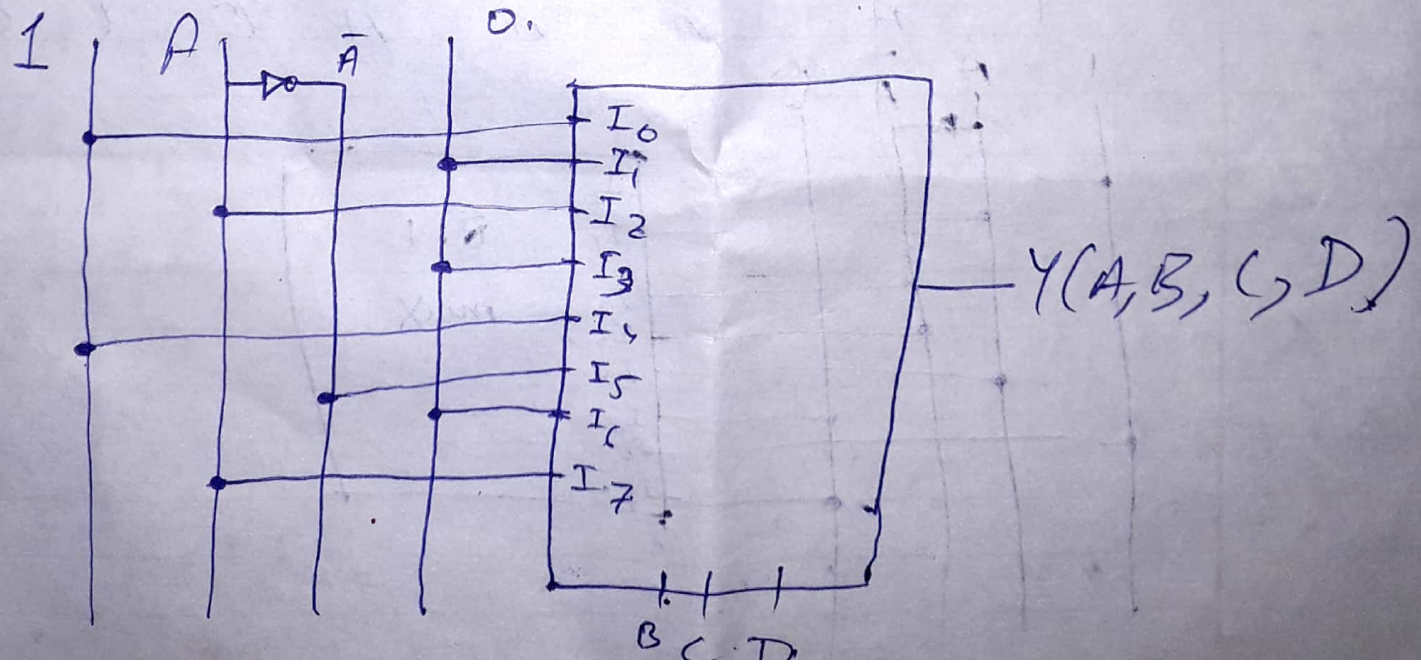
Ques2 Design a logic circuit that recieves a four bit binary in ABC D and gives an output Y. When ever the number is divisible by 4 & 5. Realize it using 8:1 mux.

Sol^n

$Y = \Sigma m(0, 4, 5, 8, 10, 12, 15)$

Taking BCD as supply line 9

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	(0)	1	2	3	(4)	(5)	6	7
A	(8)	9	(10)	11	(12)	13	14	(15)
	1	0	A	0	1	$\bar{A}$	0	A



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Ques 3 Implement the given Boolean $f(A, B, C, D) = \Sigma m(0,1,2,5,8,13,14)$ using

(a) 16 : 1 mux

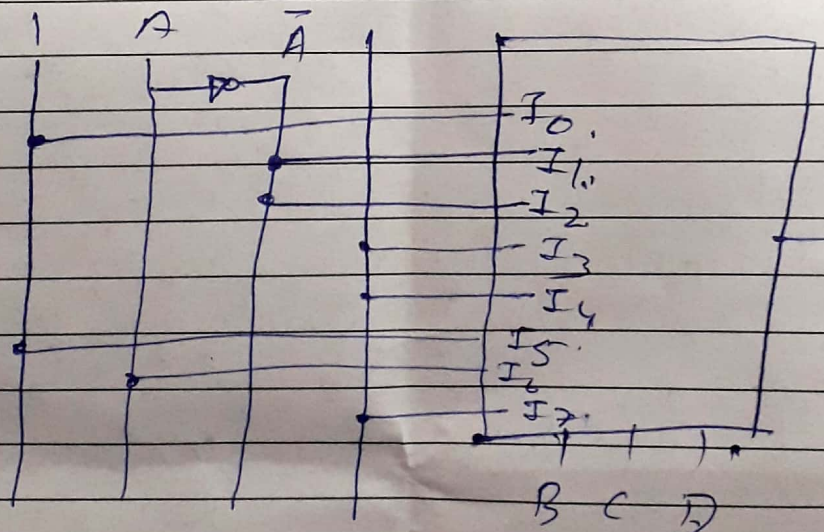
(b) 8 : 1 mux.

(c) 4 : 16 mux

(b) 8 : mux.

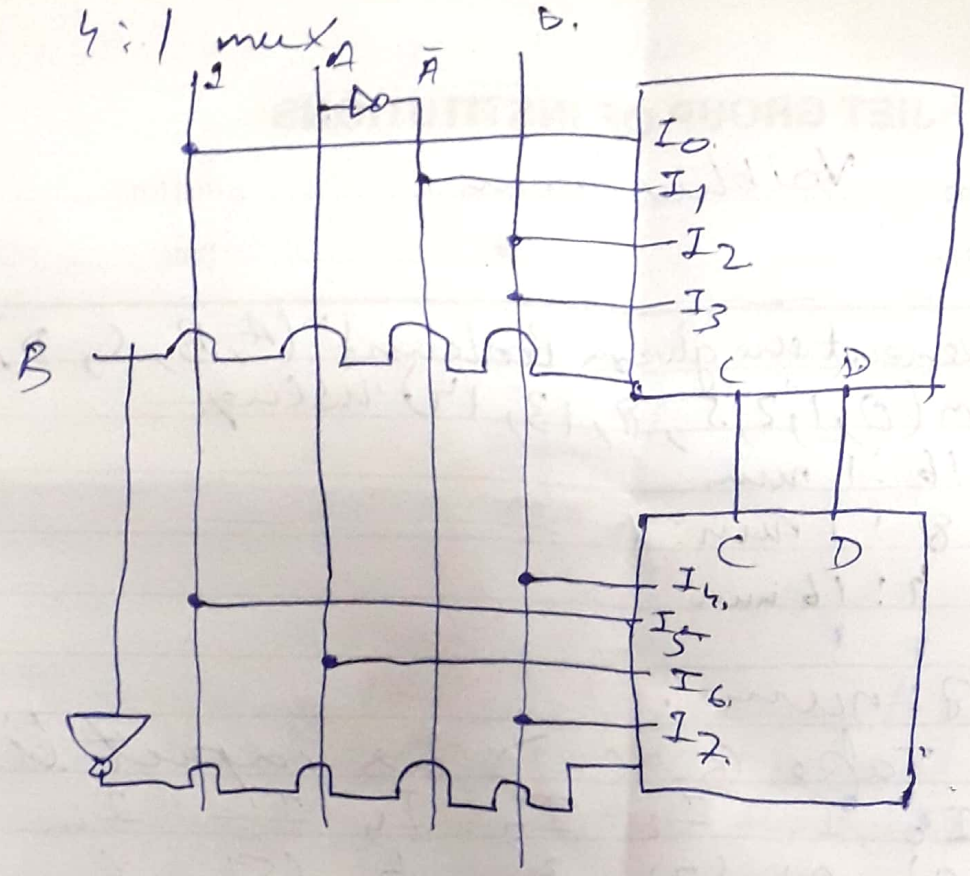
Take B C D as input line.

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	(0)	(1)	(2)	3	4	(5)	6	7
A	(8)	9	10	11	12	(13)	(14)	15
	1	$\bar{A}$	$\bar{A}$	0	0	1	A	0



$Y = \Sigma m(0,1,2,5,8,13,14)$

(c) 4:1 mux



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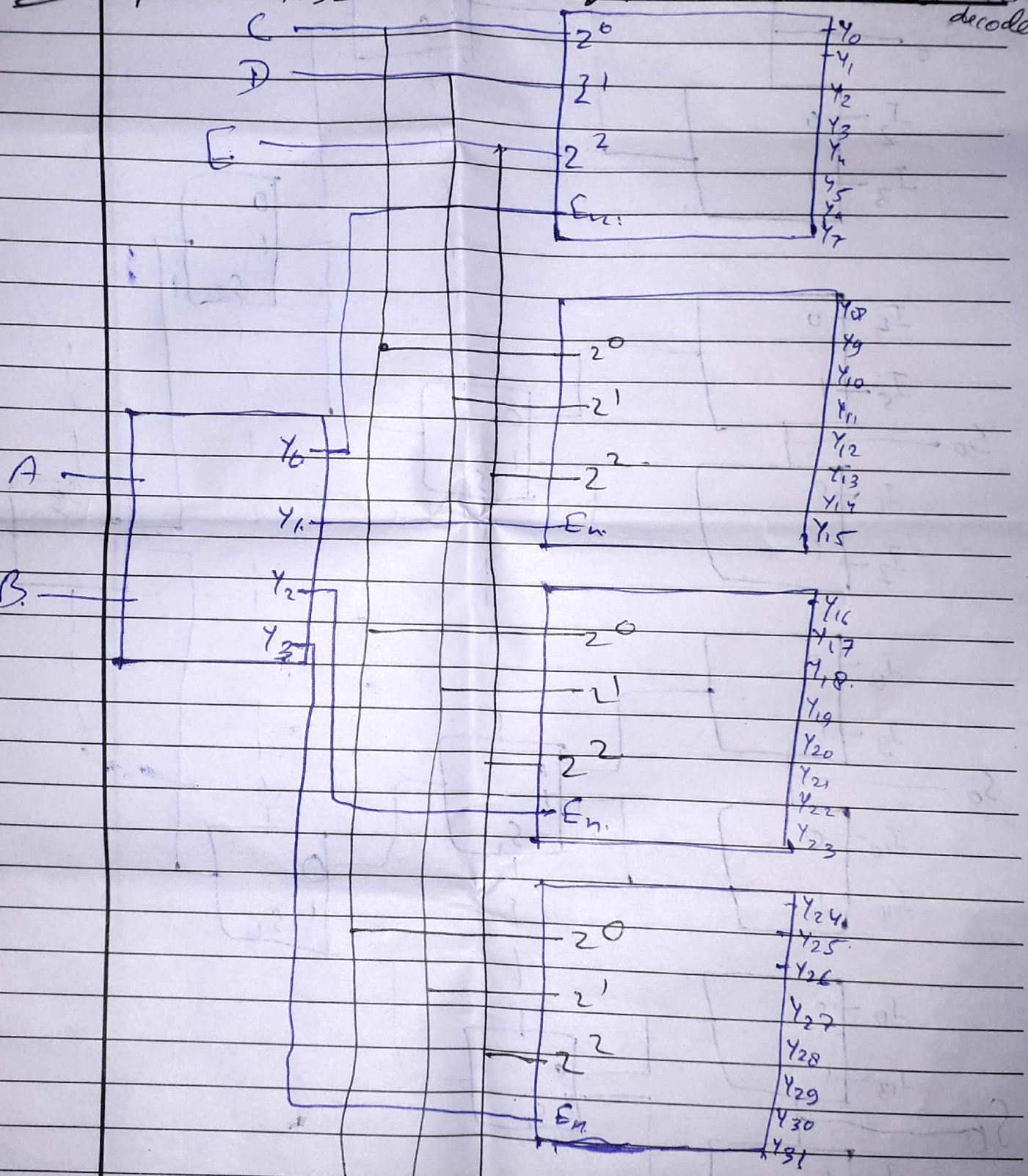
Q4 Implement 5×32 decoder using four 3×8 decoder & 2×4 decoder



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Implement 16 x 1 mux using 2x1 mux