10/10/19

Digital Electronics

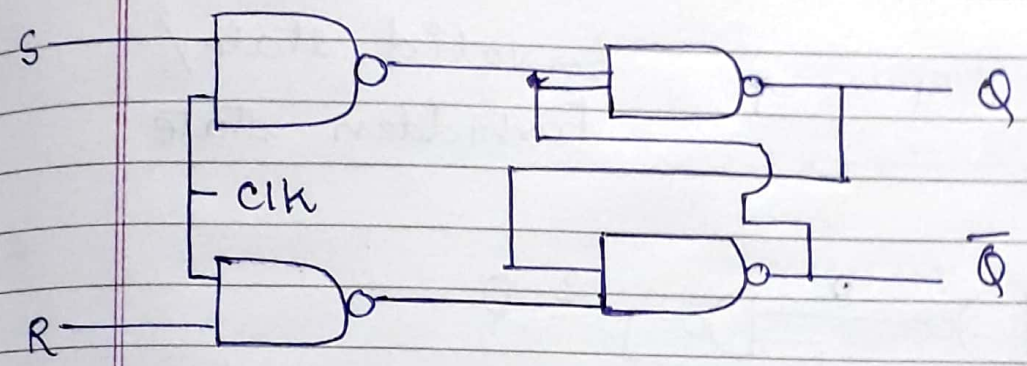
Sequential Circuits

→ to hold a value 0/1

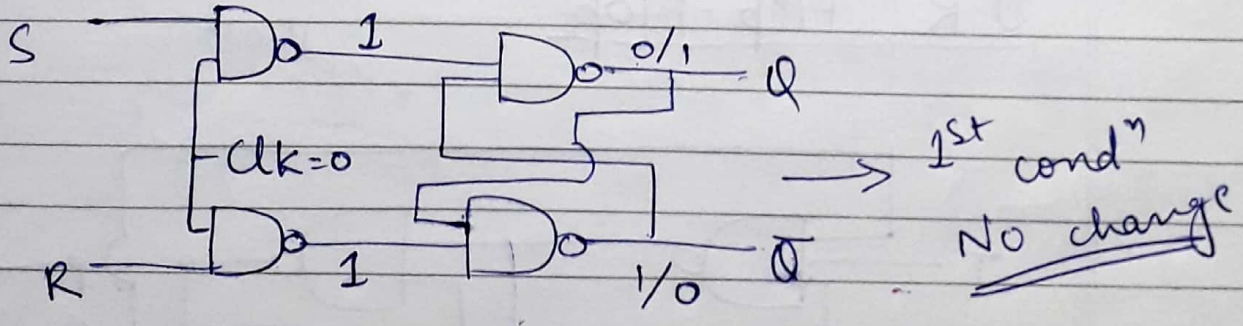
- SR Latch → NAND
  NOR

Clk = clock (digital signal)

- SR Flip Flop

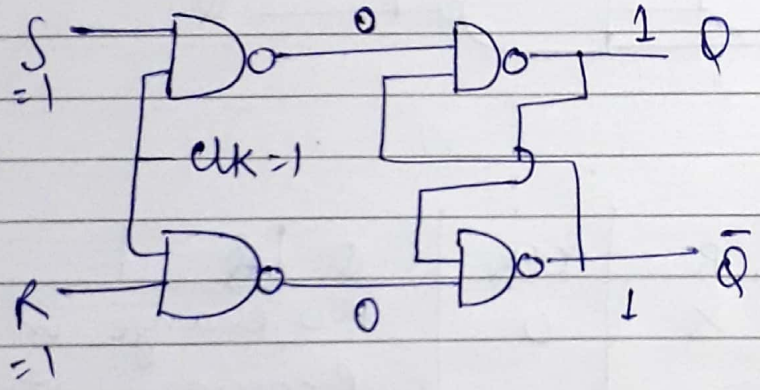


S	R	Clk	Q | $\bar{Q}$
x	x	0	No change in O/P Previous state



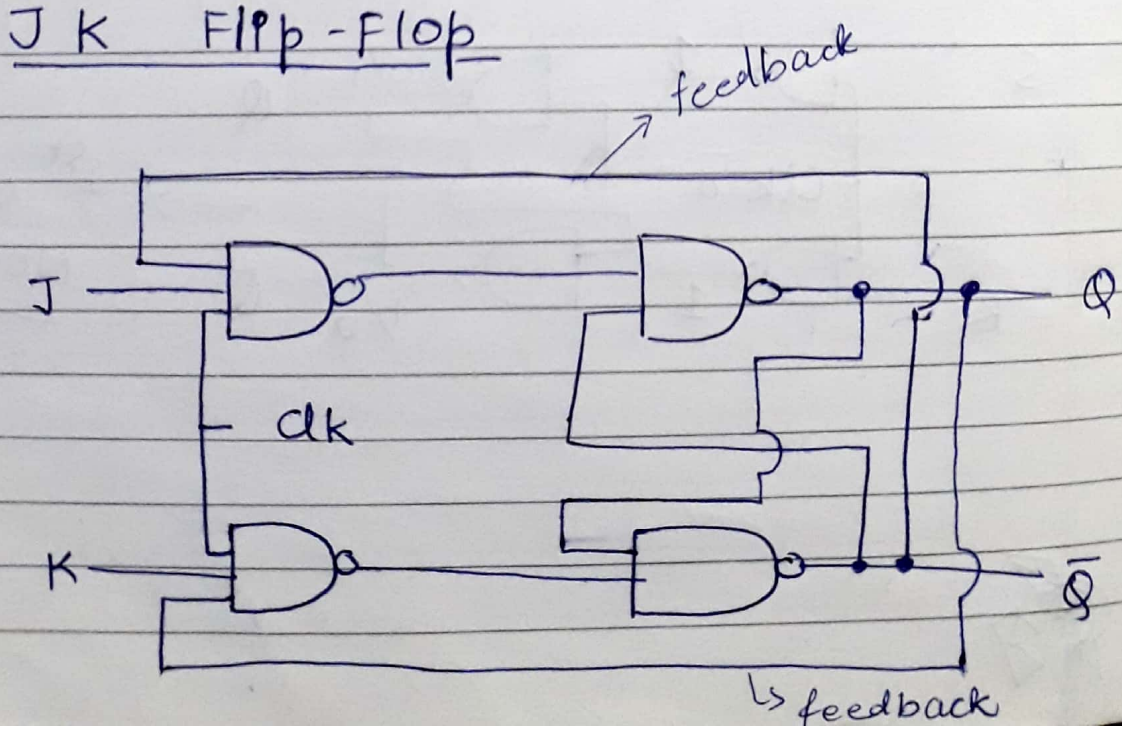
Flip-flop → storage dcts

S	R	clk	Q	$\bar{Q}$
x	x	0	No change in o/p	
0	0	1	No change in o/p	
0	1	1	0	1
1	0	1	1	0
1	1	1	Invalid state/ Forbidden state	



last case

JK Flip-Flop

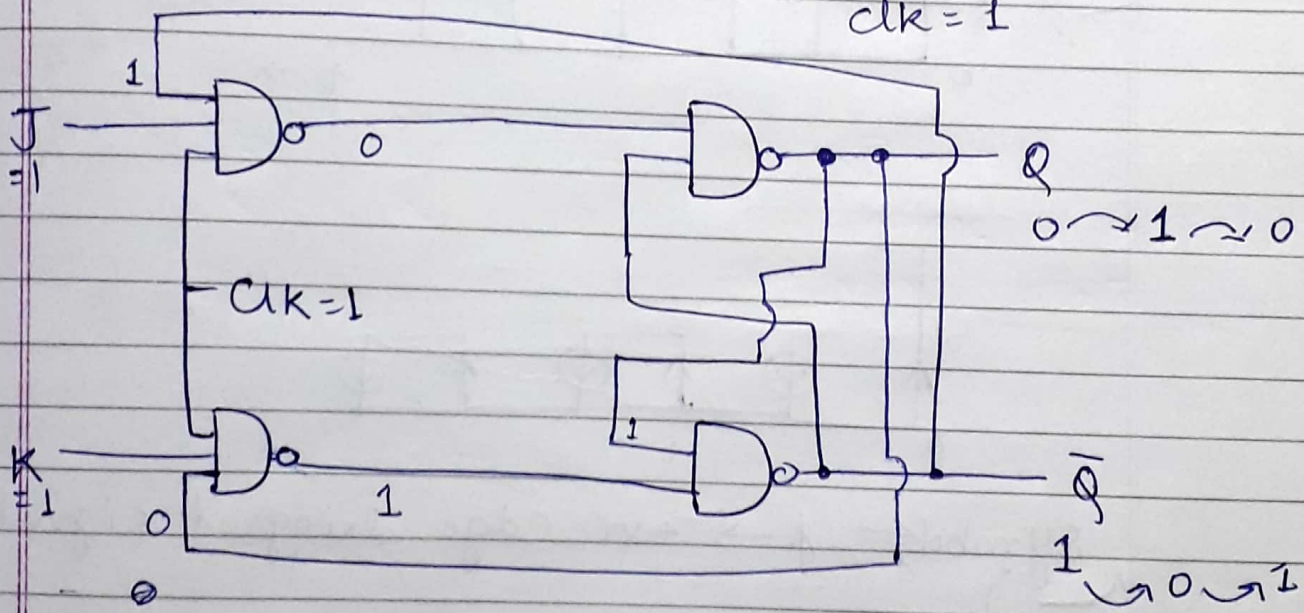


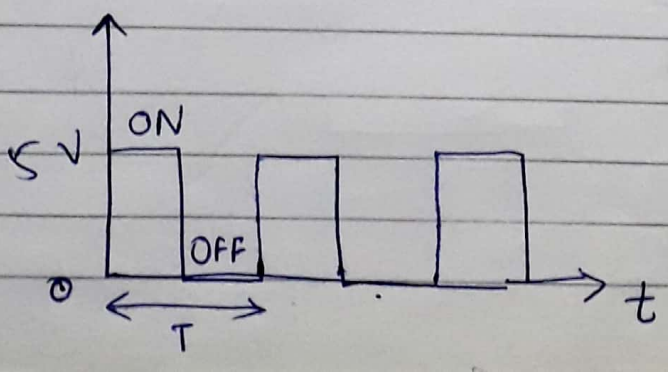
J	K	clk	Q	$\bar{Q}$	
X	X	0	Previous state		
0	0	1	Previous state		
0	1	1	0	1	in these cycles will move till the final o/p
1	0	1	1	0	
1	1	1	Toggle o/p (Race around)		

assume Q = 0 & $\bar{Q}$ = 1 at first.

↙ uncertain cond"

← this will happen till clk = 1





Propogation time

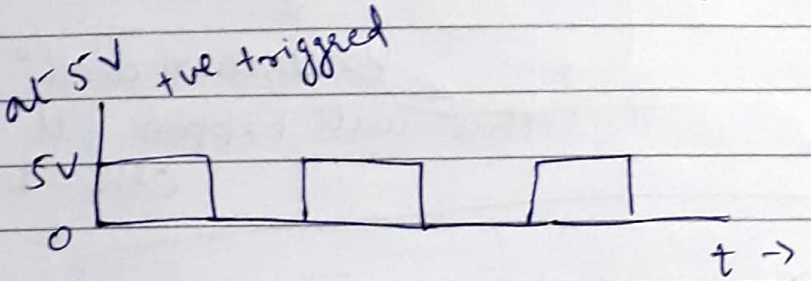
clock

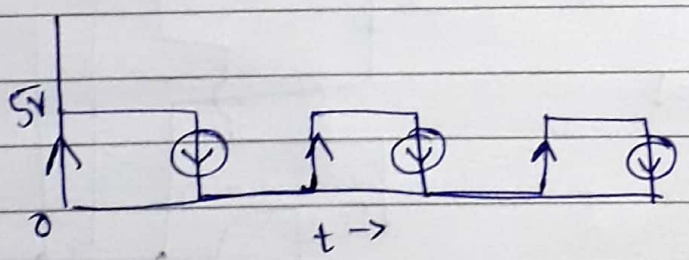
→ giving I/P

level triggering
edge triggering

—— clk Positive level triggred signal
o—— clk negative level triggred signal

>—— clk → edge triggred signal (+ve)
o>—— clk edge triggred (-ve)





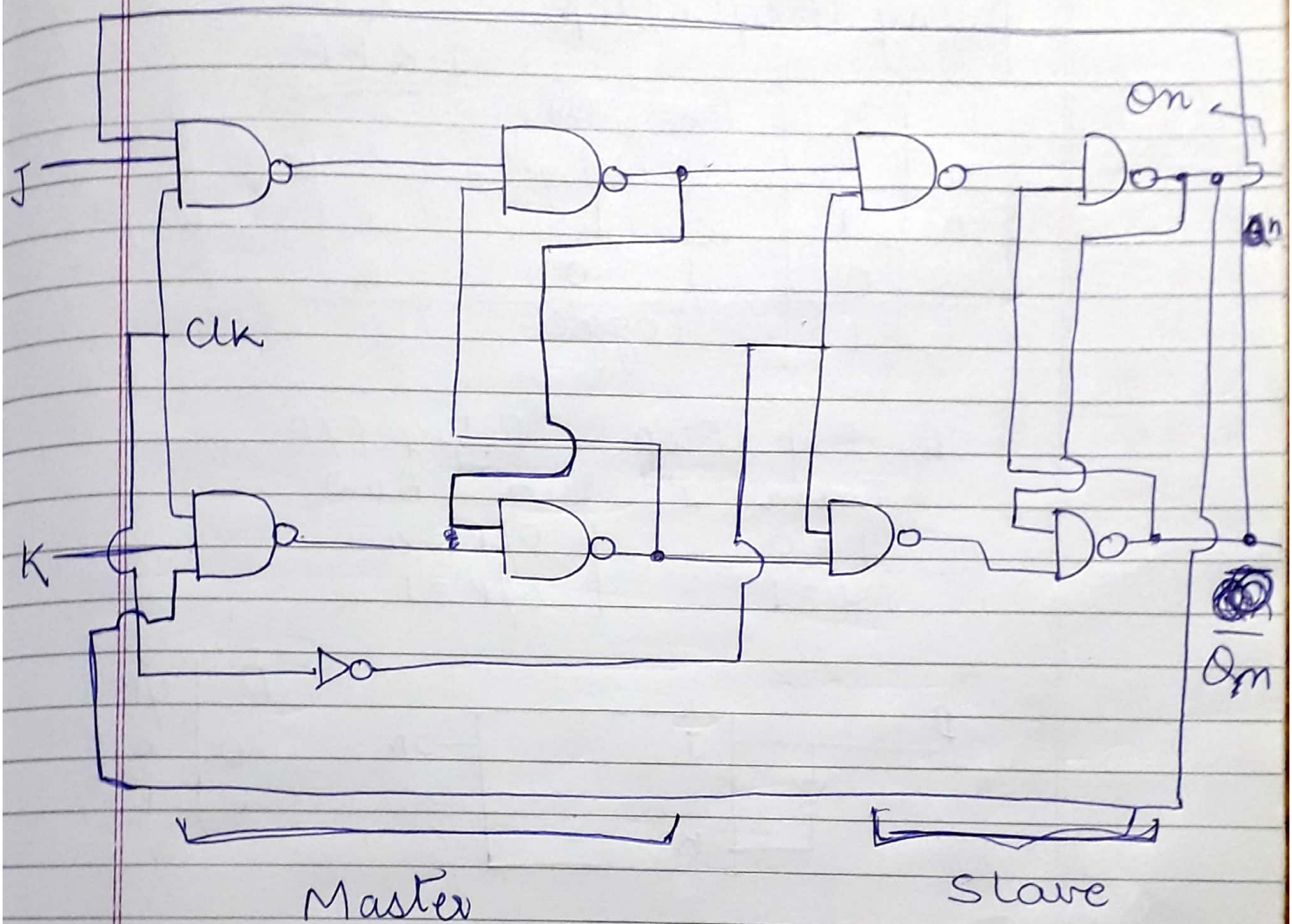
Symbol ← ↑ → +ve edge triggred signal
(>—)

↓ → -ve edge triggred signal

(o—)

Shaili Jain

Masters ~~Slave~~ ~~Safe~~ Slave Mode for JK flip flop



J	K	On
0	0	No change
0	1	0
1	0	1
1	1	$\overline{On}$

Flip-Flop Conversions

Delay Flip-Flop

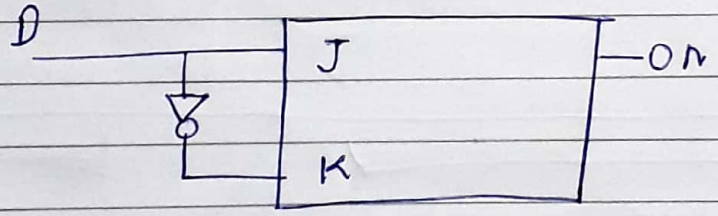
J-K F/F

J	K	Q_n	$\bar{Q}_n$
0	0	No change	
0	1	0	1
1	0	1	0
1	1	Toggle	

D Flip Flop Delay F/F

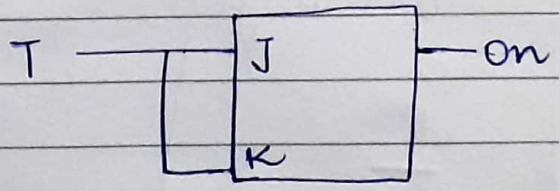
From 2nd & 3rd Row

J = 0	O/P = 0
J = 1	O/P = 1



D	O/P
0	0
1	1

Toggle T-Flip Flop



T	On
0	Previous
1	Toggle

Flip-Flop conversions

SR Flip-Flop to T flip flop

Truth table / Excitation table for T-flip-flop

Modified

T	Present state Q_n	next state Q_{n+1}	S	R	S_m	R_m
0	0	0	0	0	0	x
0	1	1	0	0	x	0
1	0	1	1	0	1	0
1	1	0	0	1	0	1

always see the next state o/p

K-map for S

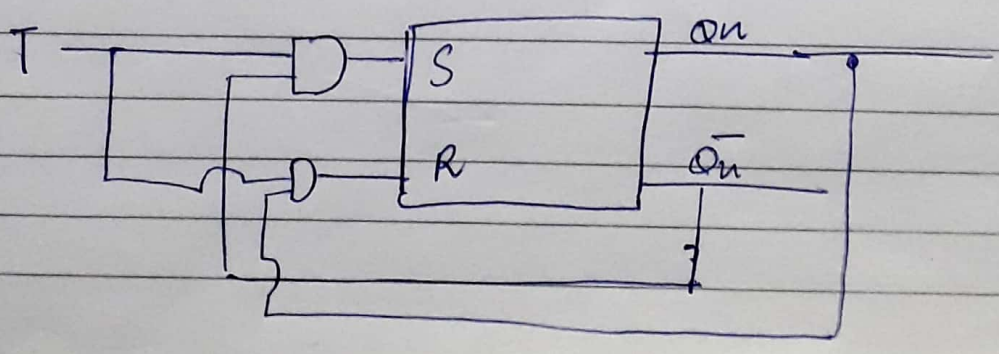
Q_n \ T	0	1
0	0 (0)	1 (2)
1	x (1)	0 (3)

K-map for R

Q_n \ T	0	1
0	x (0)	0 (2)
1	0 (1)	1 (3)

$S = T\bar{Q}_n$

$R = TQ_n$



SR flip-flop to D-flip flop

D	Q_n	$\bar{Q_n}$	S	R	Modified S	Modified R
0	0	0	0	1	0	x
			0	0		
1	1	1	1	0	x	0
			0	0		