Topic: - 8255A - Programmable Peripheral Interface

The 8255A is a general purpose programmable I/O device designed to transfer the data from I/O to interrupt I/O under certain conditions as required. It can be used with almost any microprocessor.

It consists of three 8-bit bidirectional I/O ports (24I/O lines) which can be configured as per the requirement.

Ports of 8255A

8255A has three ports, i.e., PORT A, PORT B, and PORT C.

- **Port A** contains one 8-bit output latch/buffer and one 8-bit input buffer.
- **Port B** is similar to PORT A.
- **Port C** can be split into two parts, i.e. PORT C lower (PC0-PC3) and PORT C upper (PC7-PC4) by the control word.

These three ports are further divided into two groups, i.e. Group A includes PORT A and upper PORT C. Group B includes PORT B and lower PORT C. These two groups can be programmed in three different modes, i.e. the first mode is named as mode 0, the second mode is named as Mode 1 and the third mode is named as Mode 2.

Operating Modes

8255A has three different operating modes −

- **Mode 0** − In this mode, Port A and B is used as two 8-bit ports and Port C as two 4-bit ports. Each port can be programmed in either input mode or output mode where outputs are latched and inputs are not latched. Ports do not have interrupt capability.
- **Mode 1** − In this mode, Port A and B is used as 8-bit I/O ports. They can be configured as either input or output ports. Each port uses three lines from port C as handshake signals. Inputs and outputs are latched.
- **Mode 2** − In this mode, Port A can be configured as the bidirectional port and Port B either in Mode 0 or Mode 1. Port A uses five signals from Port C as handshake signals for data transfer. The remaining three signals from Port C can be used either as simple I/O or as handshake for port B.

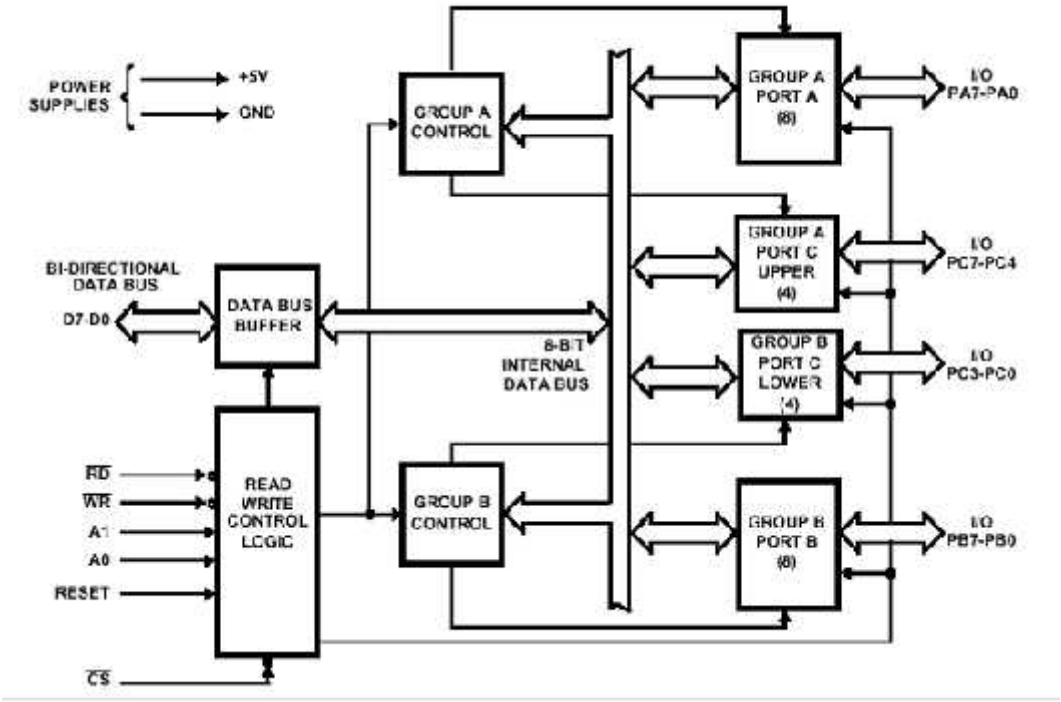
Features of 8255A

The prominent features of 8255A are as follows −

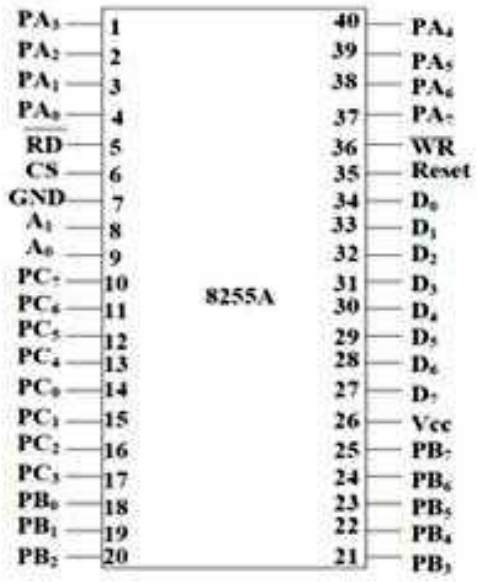
- It consists of 3 8-bit IO ports i.e. PA, PB, and PC.
- Address/data bus must be externally demux'd.
- It is TTL compatible.
- It has improved DC driving capability.

8255 Architecture

The following figure shows the architecture of 8255A –



The functional description of the pins in 8255A.



Data Bus Buffer

It is a tri-state 8-bit buffer, which is used to interface the microprocessor to the system data bus. Data is transmitted or received by the buffer as per the instructions by the CPU. Control words and status information is also transferred using this bus.

Read/Write Control Logic

This block is responsible for controlling the internal/external transfer of data/control/status word. It accepts the input from the CPU address and control buses, and in turn issues command to both the control groups.

CS

It stands for Chip Select. A LOW on this input selects the chip and enables the communication between the 8255A and the CPU. It is connected to the decoded address, and A_0 & A_1 are connected to the microprocessor address lines.

Their result depends on the following conditions –

CS	A_1	A_0	Result
0	0	0	PORT A
0	0	1	PORT B
0	1	0	PORT C
0	1	1	Control Register
1	X	X	No Selection

WR

It stands for write. This control signal enables the write operation. When this signal goes low, the microprocessor writes into a selected I/O port or control register.

RESET

This is an active high signal. It clears the control register and sets all ports in the input mode.

RD

It stands for Read. This control signal enables the Read operation. When the signal is low, the microprocessor reads the data from the selected I/O port of the 8255.

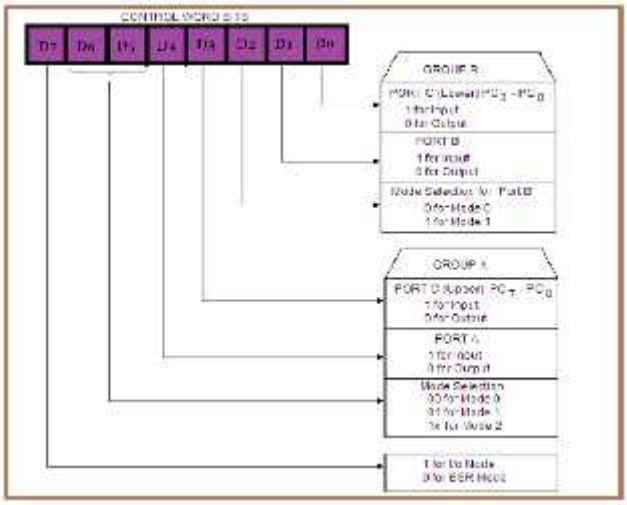
A_0 and A_1

These input signals work with RD, WR, and one of the control signal. Following is the table showing their various signals with their result.

A_1	A_0	RD	WR	CS	Result
0	0	0	1	0	**Input Operation** PORT A → Data Bus
0	1	0	1	0	PORT B → Data Bus
1	0	0	1	0	PORT C → Data Bus
0	0	1	0	0	**Output Operation** Data Bus → PORT A
0	1	1	0	0	Data Bus → PORT A
1	0	1	0	0	Data Bus → PORT B
1	1	1	0	0	Data Bus → PORT D

CONTROL WORD FORMAT FOR 8255A

The format for the control word format for 8255A is shown in figure bellow. As per the requirement of the programmer the control word is written into the control word register of 8255A. No read operation of the control word is allowed.



So from above control word format for 8255A diagram we can see the bit wise function of control word generation. Now we go for further description of the control bits. We know in control word format it has 8 bits. And every bit responsible for respective work. Now see what are the work those bits do?

Bit D0:

Sets Port C Lower as input or output port.
To make Port C Lower as input port this bit is set to 1.
To make Port C Lower as output port this bit is set to 0.

Bit D1:

Sets Port B as input or output port.
To make Port B as input port this bit is set to 1.
To make Port B as output port this bit is set to 0.

Bit D2:

This bit is for mode selection for the port B.
If this bit is set to 0, the port B will operate in mode 0.
If this bit is set to 1, the port B will operate in mode 1.

Bit D3:

Sets Port C Upper as input or output port.
To make Port C Upper as input port this bit is set to 1.
To make Port C Upper as output port this bit is set to 0.

Bit D4:

Sets Port A as input or output port.
To make Port A as input port this bit is set to 1.
To make Port A as output port this bit is set to 0.

Bits D5 and D6:

These two bits are used to determine the I/O mode of port A.

These bits are defined for the various modes of port A as follows:

D6	D5	Mode of port A
0	0	Mode 0
0	1	Mode 1
1	0 or 1	Mode 2

Bit D7:

This bit specifies either I/O function or bit set/reset function (BSR mode). If this bit is set to 1 then the 8255 will work in I/O mode. If this bit is set to 0 then the 8255 will work in BSR mode.