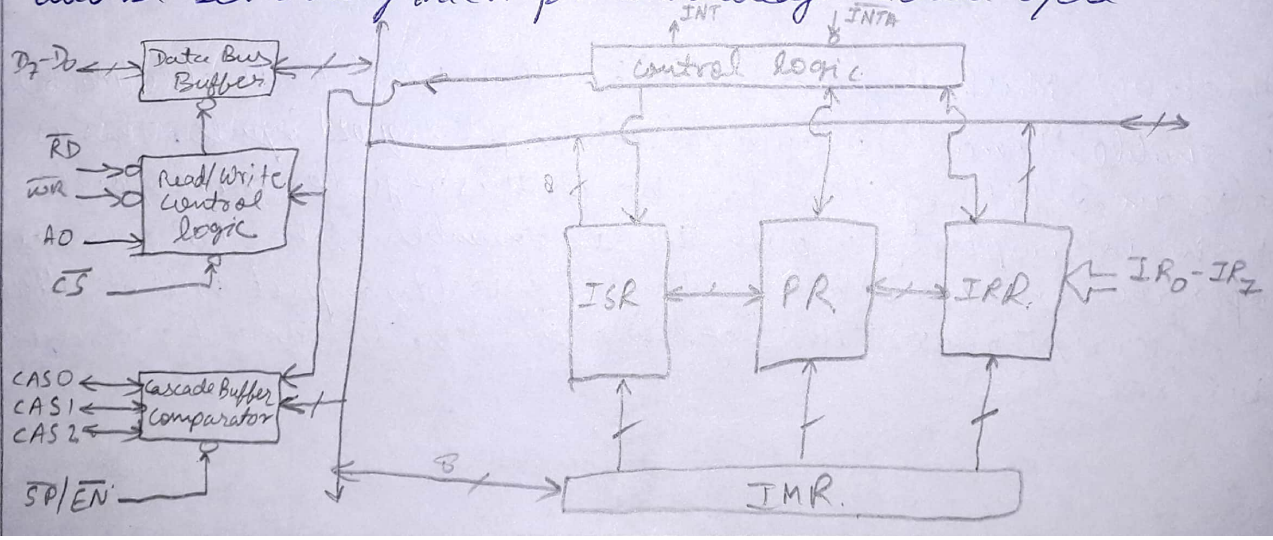
Q1 The 8259 programmable Interrupt Controller is specially designed to work with Intel microprocessor 8080, 8085 etc.

In-Service Register (ISR): The inservice register keeps track of which interrupt inputs are currently being serviced. For each input that is currently bling serviced the corresponding bit of in-service register (ISR) will be set. In 8259, during the service of an interrupt request, if another higher priority interrupt becomes active, it will be acknowledged and the control will be transferred from lower priority interrupt service subroutine (ISS) to higher priority ISS.

Interrupt Mask Register (IMR): IMR is used to disable (Mask) or enable (Unmask) individual interrupt request inputs. This is also an 8-bit register. Each bit in this register corresponds to the interrupt input with the same number. The IMR operates operates on IRR. Masking of higher priority input will not affect the interrupt request lines of lower priority. To unmask; corresponding bit is set to 0.

Interrupt Request Register (IRR): It stores all the interrupt inputs that are requesting service. It is an 8-bit register - 1 bit for each interrupt request. It keeps track of which interrupt input is asking for service. If an interrupt input is unmasked and has an interrupt signal on it, then the corresponding bit in the IRR will be set. Its content can be read to know the status of pending interrupts.

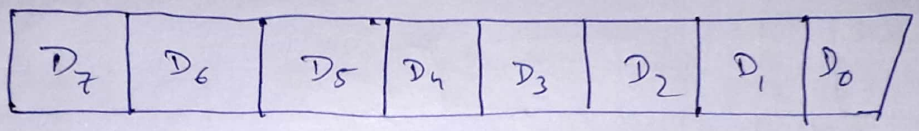
Priority Resolver (PR): This determines the priorities of interrupts set in the IRR. It takes the information from IRR, IMR and ISR to determine whether the new interrupt request is having highest priority or not. If the new interrupt request is having the highest priority, it is selected & processed. The corresponding bit of ISR will be set during interrupt acknowledge machine cycle.



Q2

Given:
Address of CW register = 83 H.
I/O mode, port A → Input, port B → output / port CL → output, port CU → input

Now,



for I/O mode D_7 is set to 1.

for D_6 & D_5 they are set to 0 ~~for port A is input~~ for mode 0 I/O.

D_4 is set to 1 for port A input.

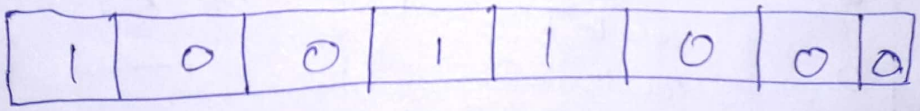
D_3 is set to 1 for port C upper input.

D_2 is set to 0 for mode 0 port B.

D_1 is set to 0 for port B output

D_0 is set to 0 for port C lower output

⇒

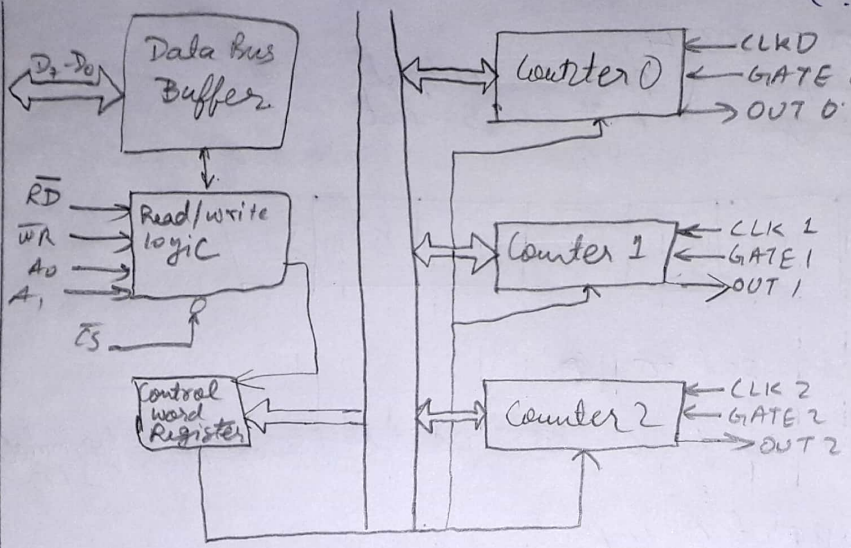


= 98 H.

Commands: MVI A, 98H ; load control word.
OUT 83H ; send control word.

Q3

(a)

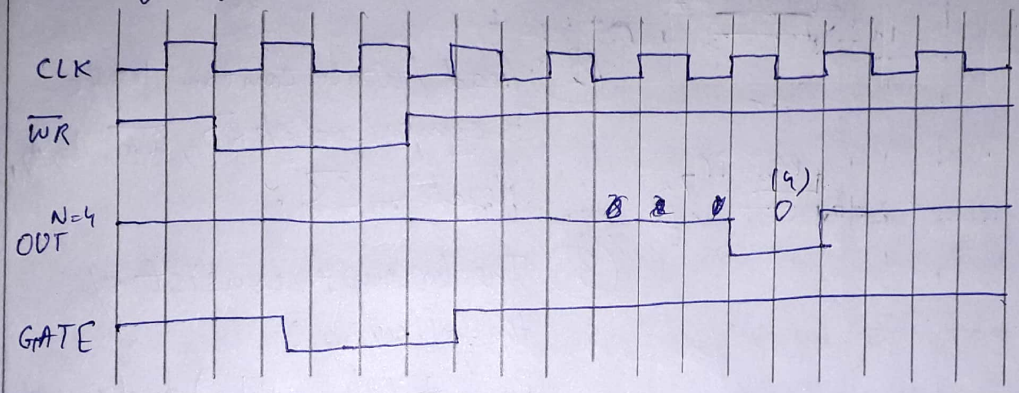


It includes 5 signals, i.e. RD, WR, CS and the address lines A_0 & A_1. In the peripheral I/O mode, the RD & WR signals are connected to IOR and IOW, respectively. In the memory mapped I/O mode, these are connected to MEMR & MEMW. The control word register & counters are selected according to signals on lines A_0 & A_1.

A_1	A_0	Result
0	0	Counter 0
0	1	counter 1
1	0	counter 2
1	1	control word Register
x	x	No Selection.

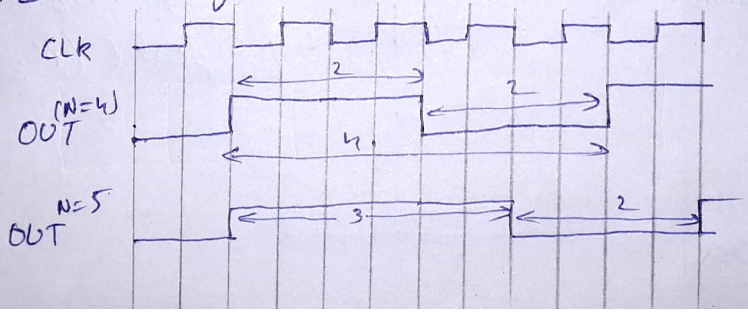
(b) Mode 2 : Rate Generator / Divide by N Counter.

When N is loaded as count, after N pulses, OUT goes low for only 1 clock cycle and then count N is reloaded & result is OUT; as high for N clock pulses.

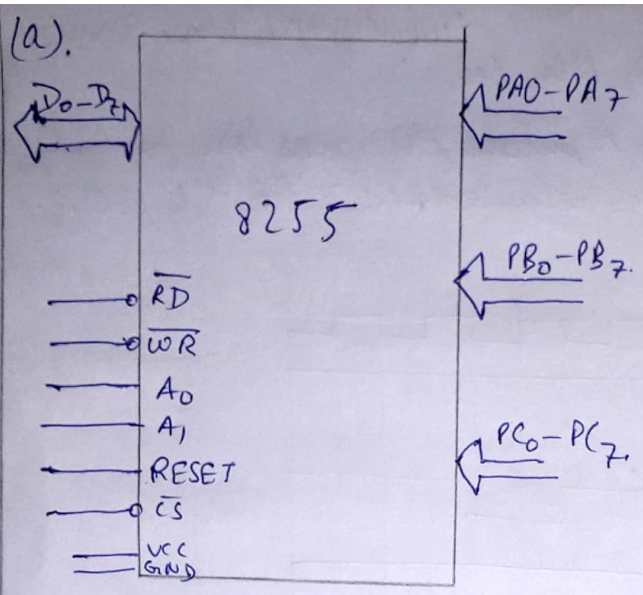


Mode 3 : Square Wave Rate generator.

When count N loaded with even the O/p remains high for half the count & LOW for the rest. If it is odd. the O/p remains high for (N+1)/2 & low for (N-1)/2.



Q4 (a).



I/O port assignment

A_1	A_0.	function
0	0	Port A
0	1	Port B
1	0	Port C
1	1	command Register

(1) D_0-D_7 is a bidirectional data Bus buffer.

(2) Read / Write control logic is comprised of $\overline{RD}$, $\overline{WR}$, A_0, A_1, Reset & $\overline{CS}$.

(3) The Group A consist of the following:
Port A (PA_7-PA_0) and upper half of port C (PC_7-PC_4)

(4) Group B is comprised of port B (PB_7-PB_0) and lower half of port C (PC_3-PC_0).

(b) There are two modes of 8255.
1.) Input/Output mode. 2.) Bit Set Reset (BSR) mode

1.) The I/O mode further comprises of :-

Mode 0 → It is used to provide simple I/P & O/P capabilities using each of the three ports.

Mode 1 → It is strobed I/O where in two groups - group A and B are available for strobed data transfer.

Mode 2 → It is for bi-directional operation in which only single 8 bit port in group A is available.

2.) BSR mode: In this mode any of the 8-bits of port C can be set or reset depending on D_0 of the control word. The bit to be set or reset is selected by bit select flags D_3, D_2 & D_1 of the CWR (Control Word Register).

Q5. The 8251 is a USART (Universal Synchronous Asynchronous Reciever Transmitter) for serial data communication..

↳ The Control words are of two types:

1.) Mode Instruction: It is used for setting the funct" of the 8251. Mode Instruction will be in "wait for write" at either internal reset or external reset. That is, the writing of a control word after resetting will be recognized as a "mode instruction".

2.) Command: It is used for setting the operation of the 8251. It is possible to write a command whenever necessary after writing a mode instruction and sync characters.

↳ Status Word: To see the internal status of 8251, status words are used. by reading a status word it is possible to see internal status. Some of the status words are.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
DSR	SYNDET/BD	FE	OE	PE	TXEMPTY	RXRDY	TXRDY

(bit configuration)

Data buffer Register: It helps in interfacing the internal data bus of 8251 to the system data bus. It is the data buffer register which makes the transmission possible between 8251 and CPU by the data bus buffer block.

Block dig of 8251 USART.