[This question paper contains 8 printed pages.]

Your Roll No.....

Sr. No. of Question Paper : 1039 **D**

Unique Paper Code : 2342011102

Name of the Paper : Computer System Architecture

Name of the Course : **B.Sc. (H) COMPUTER SCIENCE (NEP-UGCF-2022)**

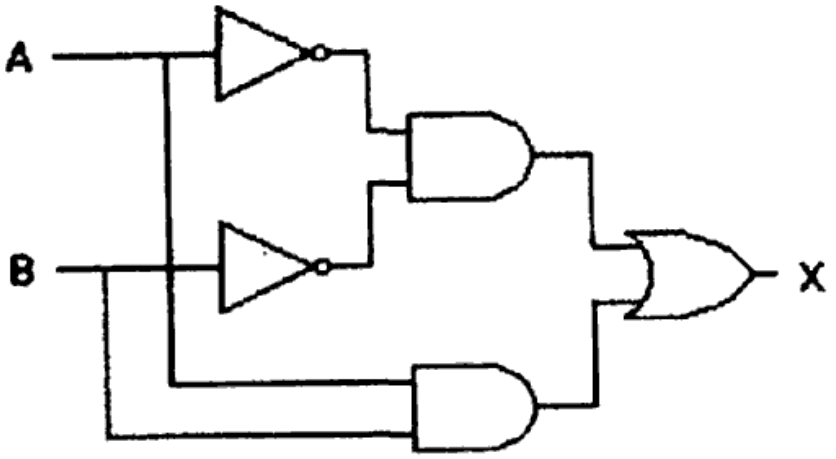
Semester : I

Duration : 3 Hours Maximum Marks : 90

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. Question No. **1** is compulsory.
3. Attempt any **4** questions from Question **2** to Question **7**.
4. Parts of a question must be answered together.

1. (a) Give the Boolean expression for the following logic diagram.



(b) State DeMorgan's law and prove it using truth table. (3)

(c) Name the register:

(i) Instruction from memory will be transferred to this register.

(ii) The address part of the memory-reference instruction is transferred to this register.

(iii) This register contains the address of next instruction that will be executed. (3)

(d) What is a register-reference instruction? Give any two examples. Name the addressing mode used by these instructions? (3)

(e) Perform the arithmetic operation (-5) + (-6) in binary using 2's complement and 4-bit register. Show if there is any overflow. (3)

(f) (i) Find 8's complement of $(542)_8$.

(ii) Subtract $(0100\ 1011)_2$ from $(0110\ 0110)_2$. (3)

(g) Write the microinstructions for fetch and decode phase of the instruction cycle along with control signals. (4)

(h) Briefly explain the working of encoder? How is it different from decoder? (4)

(i) Explain control command, status command, data input command, data output command in relation to I/O communication. (4)

2. (a) Draw the logic diagram of a 8-to-1 line multiplexer. Explain its working with the help of function table. (4)

(b) Simplify the following Boolean function F, together with the don't-care condition d in SOP form and draw the logic diagram for the simplified F.

$F(A, B, C, D) = \Sigma(4, 5, 7, 12, 13, 14)$

$d(A, B, C, D) = \Sigma(1, 9, 11, 15)$ (5)

(c) An instruction at address 021 in the basic computer has I=0, an operation code specifying the AND operation, and an address part equal to 083 (all numbers are in hexadecimal). The memory word at address 083 contains the operand B8F2 and the content of AC is A937. Go over the instruction cycle and determine the contents of the following registers: PC, AR, DR, AC and IR at the end of each timing signal starting from T_0 to the end of execute cycle. (6)

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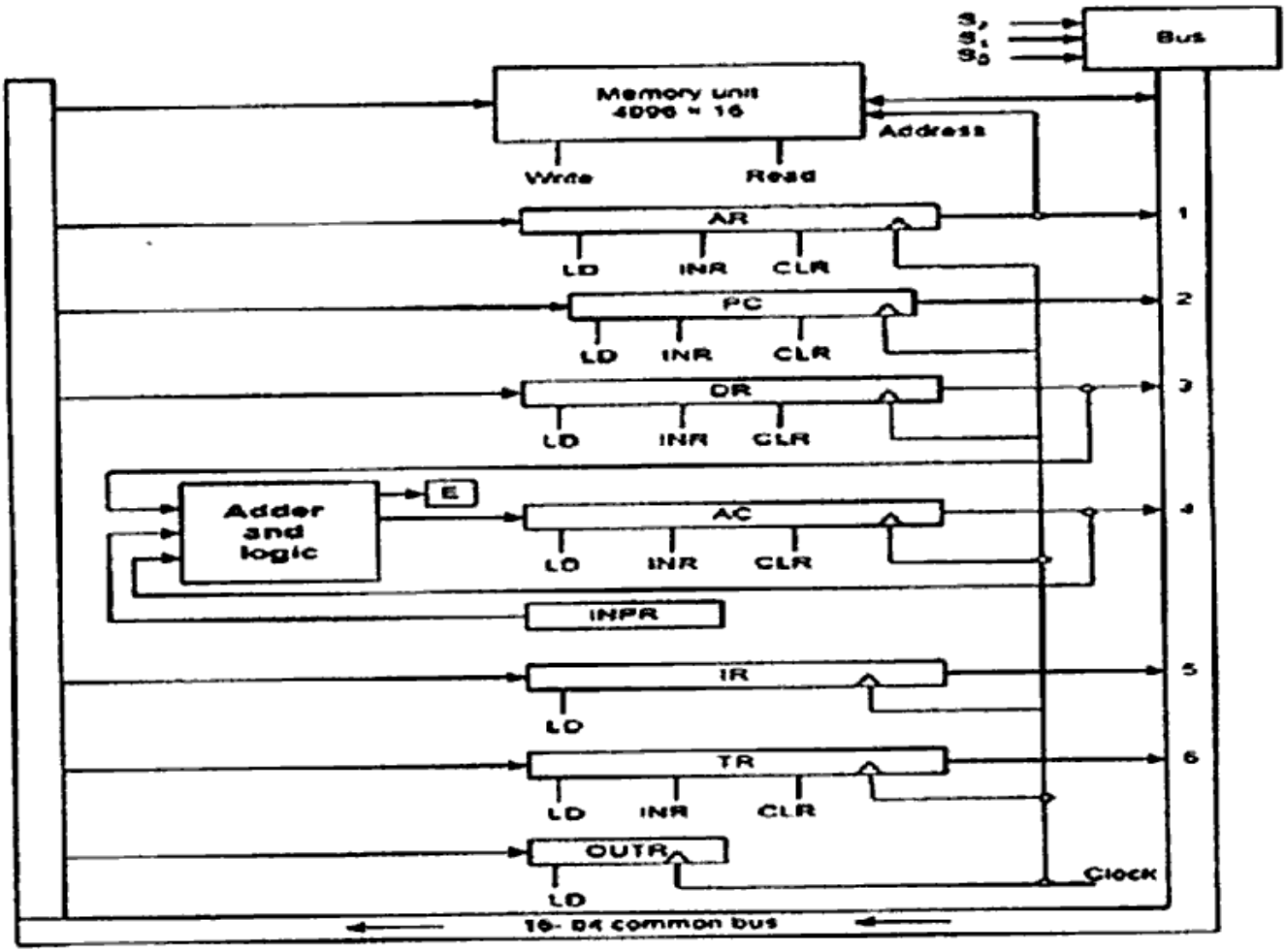
3. (a) Perform the following conversions :

(i) Convert the decimal number 245.25 to hexadecimal.

(ii) Convert $(101101.11)_2$ to decimal. (4)

(b) How many 2-to-4-line decoders will be used to construct a 4-to-16-line decoder? Give the block diagram of the same. (5)

(c) Consider the bus system shown below : (6)



(i) The following control inputs are active in the given bus system

For each case, specify the register transfer that will be executed during the next clock transition.

S.No.	S_2	S_1	S_0	LD of register	Memory	Adder
a.	1	1	1	TR	Read	-
b.	0	1	0	AR	-	-
c.	1	0	0	DR	Write	-
d.	0	0	0	AC	Add	

(ii) Write the microinstruction to set the flip-flop R to 1 including the control conditions.

4. (a) Write the excitation tables for the JK flip flop. How can you derive D flip-flop from a JK flip-flop? Show with the help of a block diagram. (4)

(b) The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of seven addressing modes, a register field to specify one of the 56 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the instruction is in one memory word. (5)

(c) Assuming the time delay of the four segments in a pipeline are as follows :

t_1 = 50 ns, t_2 = 30 ns, t_3 = 95 ns, t_4 = 45 ns. The interface registers delay time t_r = 5 ns. How long

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would it take to execute an instruction over 100 pairs of data in the pipeline? What will be the speedup ratio if the time taken to execute same instruction in a non-pipelined system is 300 ns. (6)

5. (a) List any four characteristics of GPU. (4)

(b) What is DMA? How cycle stealing is different from burst transfer. (5)

(c) Draw the diagram of a 4-bit binary adder-subtractor. Explain its working with the help of an example. (6)

6. (a) Specify the fourteen-bit control word for the basic computer that must be applied to the processor to implement the following micro-operation, given the operation code for the operations are as follows :

(i) $R_6 \leftarrow shr\ R_1$

(ii) $R_3 \leftarrow R_1 - R_3$

Operation	OPCODE
ADD	00010
SHR	10000

(4)

(b) Assume that the following 8-bit registers R_1, R_2, R_3 and R_4, initially have the following unsigned values:

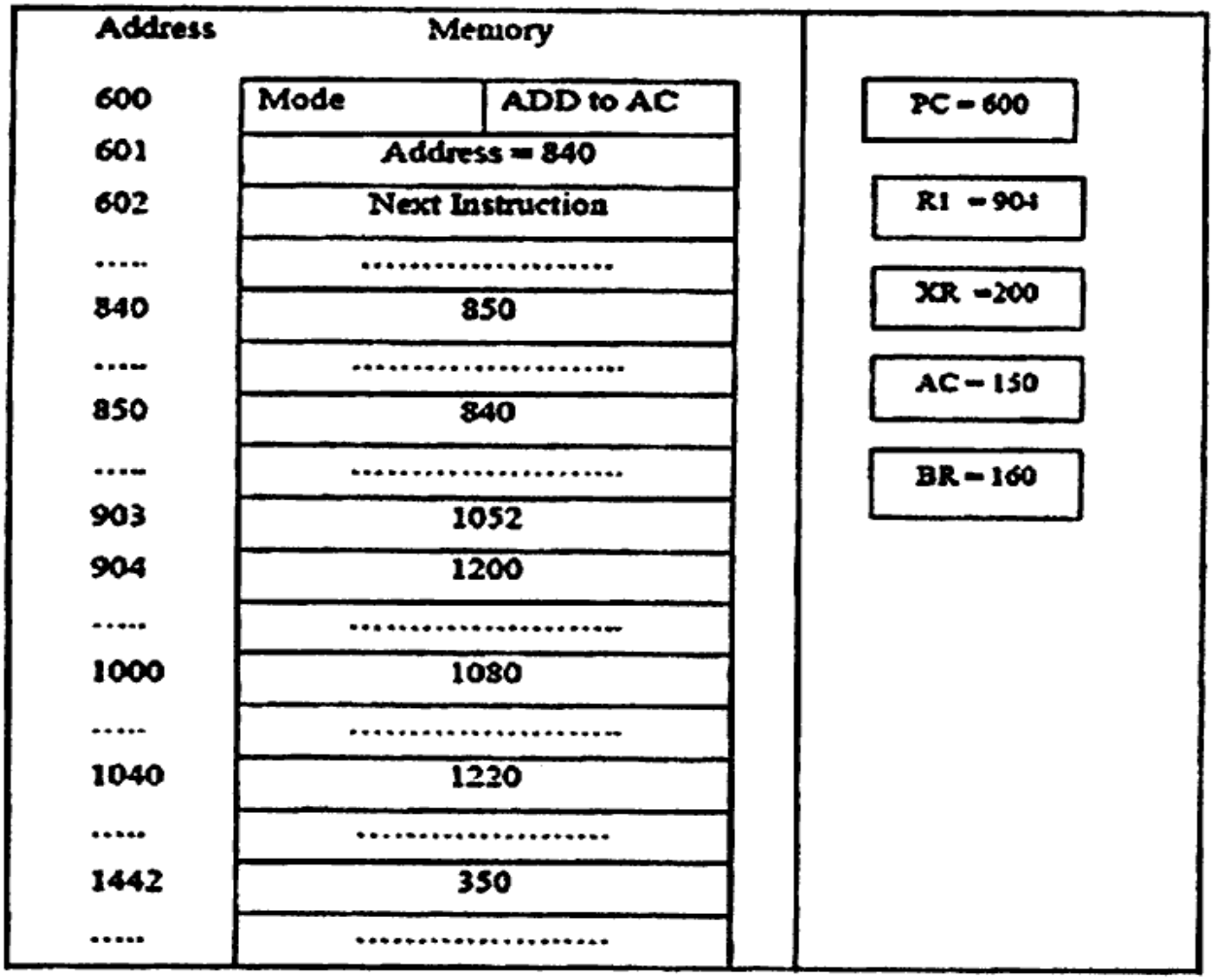
R_1=1111 0011, R_2=1110 0011, R_3=0011 1010, R_4=1010 1010

Determine the 8-bit values in each register after the execution of the following micro-operations in sequential manner:

$T_1 : R_2 \leftarrow R_4 \wedge \overline{R_3}$

$T_2 : R_4 \leftarrow \left(R_3 \vee \overline{R_2}\right) \wedge R_4$ (5)

(c) Consider the fragment of memory as shown below :



Assume that all the addresses and register / memory contents are in decimal. A two-word instruction is stored at an address 600 with address part stored at address 601. The first word consists of a 'mode bit' and the op-code for *ADD to AC* machine instruction, whereas second word of the instruction contains the value 840. Further, the

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content of memory at different addresses is as shown in the figure above. PC is a Program counter register with value 600, R1 is a general-purpose register with value 904, XR is an Index register with value 200. BR is the Base register with content 160. Determine the effective address and the content of AC register after the operation is performed for the following addressing modes:

(i) Direct Addressing

(ii) Indirect Addressing

(iii) Relative

(iv) Indexed

(v) Register Indirect

(vi) Base Register addressing. (6)

7. (a) What is cache memory? How is it different from auxiliary memory? (4)

(b) Given the Boolean function:

$F(A, B, C) = A'B'C + AB'C' + A'BC + ABC'$

(i) List the truth table of the function.

(ii) Simplify the algebraic expression.

(iii) Draw the logic diagram of the simplified expression using NAND gates only. (5)

(c) Explain programmed I/O with the help of a flowchart. How is it different from Interrupt driven I/O? (6)

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