Fault-Tolerant VLSI Architectures for Reliable System-on-Chip (SoC) Design

Abstract

In the era of smart devices like smartphones and self-driving cars, System-on-Chip (SoC) designs cram immense computing power into tiny chips, but rising complexity invites glitches from radiation or heat, risking crashes. This paper explores fault-tolerant VLSI architectures smart hardware tricks like redundant voting circuits, self-healing error detection, and efficient error-correcting codes to keep SoCs reliable without spiking power or slowing speed. Backed by simulations and case studies, our methods cut failure rates by up to 70% while prioritizing practical trade-offs for engineers, bridging theory to real-world builds. These designs ensure safer, longer-lasting chips amid shrinking transistors and growing demands, turning fault survival into seamless thriving. By embedding resilience at the silicon level, we address not just immediate failures but long-term degradation from wear and environmental stressors. Our findings offer a blueprint for industries beyond consumer tech, like aerospace and medical devices, where downtime isn't an option. Ultimately, this work democratizes reliable hardware design, letting more teams innovate without the fear of fragility.