

ANALOG AND DIGITAL ELECTRONICS
(Common to CSE & ISE)

Subject Code: 18CS33
Hours/Week : 03
Total Hours : 40

I.A. Marks : 40
Exam Marks : 60
Exam Hours : 3

MODULE – 1	10 Hours
Photodiodes, Light Emitting Diodes and Optocouplers ,BJT Biasing :Fixed bias ,Collector to base Bias , voltage divider bias, Operational Amplifier Application Circuits: Multivibrators using IC-555, Peak Detector, Schmitt trigger, Active Filters, Non-Linear Amplifier, Relaxation Oscillator, Current-to-Voltage and Voltage-to-Current Converter , Regulated Power Supply Parameters, adjustable voltage regulator , D to A and A to D converter.	
MODULE – 2	10 Hours
Karnaugh maps: minimum forms of switching functions, two and three variable Karnaugh maps, four variable karnaugh maps, determination of minimum expressions using essential prime implicants, Quine-McClusky Method: determination of prime implicants, The prime implicant chart, petricks method, simplification of incompletely specified functions,simplification using map-entered variables.	
MODULE – 3	10 Hours
Combinational circuit design and simulation using gates: Review of Combinational circuit design, design of circuits with limited Gate Fan-in , Gate delays and Timing diagrams,Hazards in combinational Logic, simulation and testing of logic circuits Multiplexers, Decoders and Programmable Logic Devices: Multiplexers, three state buffers,decoders and encoders, Programmable Logic devices, Programmable Logic Arrays, Programmable Array Logic.	
MODULE – 4	10 Hours
Introduction to VHDL: VHDL description of combinational circuits, VHDL Models for multiplexers, VHDL Modules. Latches and Flip-Flops: Set Reset Latch, Gated Latches, Edge-Triggered D Flip Flop 3,SR Flip Flop, J K Flip Flop, T Flip Flop, FlipFlop with additional inputs, Asynchronous Sequential Circuits	
MODULE – 5	10 Hours
Registers and Counters: Registers and Register Transfers, Parallel Adder with accumulator, shift registers, design of Binary counters, counters for other sequences, counter design using SR and J K Flip Flops, sequential parity checker, state tables and graphs.	

Textbooks:

1. Charles H Roth and Larry L Kinney, Analog and Digital Electronics, Cengage Learning,2019

Reference Books:

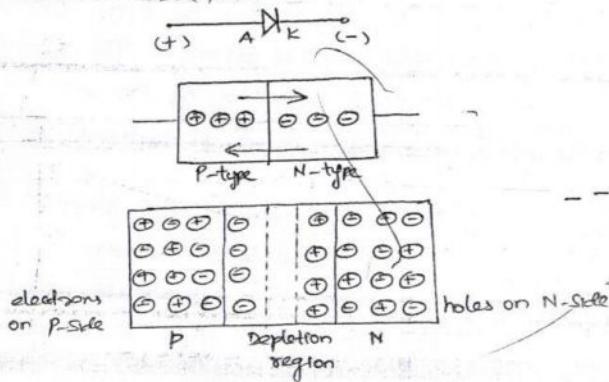
1. Anil K Maini, Varsha Agarwal, Electronic Devices and Circuits, Wiley, 2012.
2. Donald P Leach, Albert Paul Malvino & Goutam Saha, Digital Principles and Applications, 8th Edition, Tata McGraw Hill, 2015.
3. M. Morris Mani, Digital Design, 4th Edition, Pearson Prentice Hall, 2008.
4. David A. Bell, Electronic Devices and Circuits, 5th Edition, Oxford University Press, 2

ANALOG AND DIGITAL ELECTRONICS
MODULE 1: DIODE, BJT & OP-AMP

INTRODUCTION 8PH

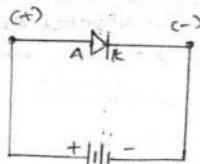
Diode:

Diode is a two-terminal semiconductor device with P-N junction. The terminals are Anode and cathode. This device is also called as Rectifier.

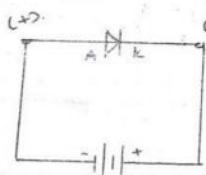


Biasing of a diode:

i) Forward Biasing



ii) Reverse Biasing



Purpose of a diode:

A diode can allow the flow of current in one direction while blocking the flow of current in the other direction. This principle of diode makes it work as a rectifier, to convert alternate current (ac) to direct current (dc) in a circuit.

This device can also work as a switch, and its useful for limiting signal levels, frequency multiplication, tuning and protecting circuitry from the flow of current in a given direction.

Types:

Backward diode, Gunn diode, Step recovery diode, Zener, Light Emitting diode, Photodiode, PIN diode, Laser diode, Schottky, Tunnel, Varactor diode.



2

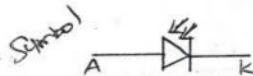
PHOTODIODES:

photodiodes are light sensitive junction semiconductor devices, that converts light energy into electric current or voltage.

When the PN Junction is illuminated by light radiation, then current or voltage is generated by the device. The Bandgap energy E_g decides the spectral response of the device.

The upper cutoff wavelength of a photodiode is given by -

$$-\lambda_c = \frac{1240}{E_g}$$



A normal p-n junction diode allows a small amount of electric current. To increase the electric current

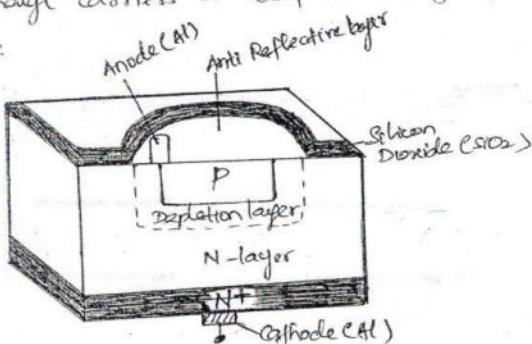
under reverse bias condition, we need to generate more minority carriers. The external reverse voltage applied to the p-n junction diode will supply energy to the minority carriers but it will not increase the population of minority charge carriers.

The minority carriers generated at outside or inside will recombine in the same material before they cross the junction. As a result, no electric current flows due to these charge carriers.

To overcome this problem, we need to apply external energy directly to the depletion region to generate more charge carriers.

A special type of diode called photodiode is designed to generate more no. of charge carriers in depletion region. In photodiodes we use light or photons as the external energy to generate charge carriers in depletion region.

⇒ Construction:



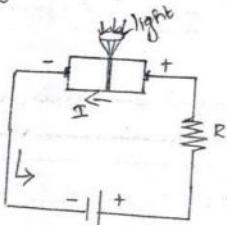


The (light facing) top of the diode is protected by a layer of Silicon Dioxide (SiO_2) in which there is a window for light to shine on the semiconductor. This window is coated with a thin anti-reflected layer of Silicon Nitride (Si_3N_4) to allow maximum absorption of light and an anode connection of Aluminium (Al) is provided to the P-type layer. More heavily doped N+ layer provides low resistance connection to the cathode.

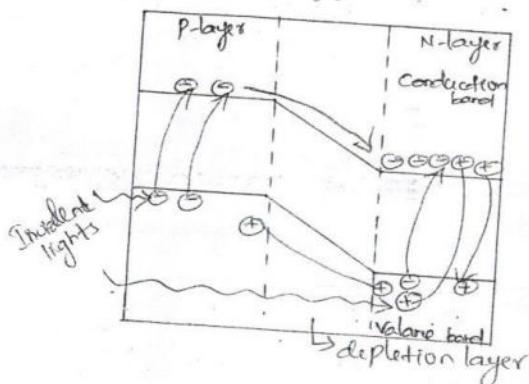
In this construction, the surface of a N+ layer is bombarded with P-type silicon ions to produce a P-type layer about 1 nm thick. During the formation of diode, excess electrons move from n-type towards p-type and excess holes move from p-type towards n-type, thus process is called diffusion, resulting in the removal of the charge carriers close to the P-N junction, and creating a depletion layer.

This construction technique is cold ion implantation.

⇒ Working Principle:



The junction of photodiode is illuminated by the light source, the photons strike the junction surface. The photons impart their energy in the form of light to the junction

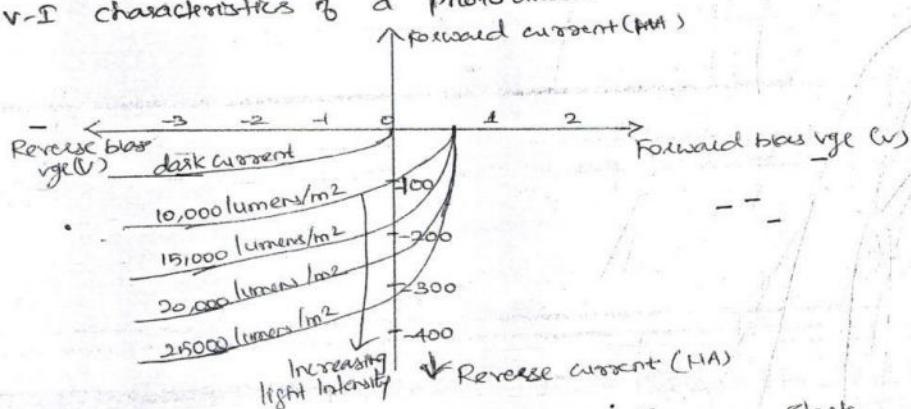


When the light is incident on the photodiode, photo induced current are generated which includes electrons in the conduction band of P-type material and holes in the valence band of N-type material.



When the photo diode is reverse biased, the photo induced electrons will move from P-side to N-side and holes will move from N-side to P-side. It causes a current flow.

⇒ V-I characteristics of a photo diode:



When the light intensity increases, the curve starts shifting downwards.

The current under large reverse bias

$$I = I_{SC} + I_0 (1 - e^{-V/V_{AT}})$$

$I_0 \Rightarrow$ The reverse saturation current in the photodiode is denoted by I_0 . It varies with light intensity

$I_{SC} \Rightarrow$ when the light is falling on photodiode and terminals are shorted, a current flows from anode to cathode is called short circuit current I_{SC} .

- $V \Rightarrow$ V is positive for forward voltage & negative for reverse bias voltage

$V_T \Rightarrow$ Volt equivalent for temperature

$\Delta \Rightarrow$ Unity(1) for germanium
2 for silicon.

⇒ Applications:

⇒ Diodes are used in smoke detector, compact disc players

& TV remote controls.

⇒ Used in clock radios, camera light meters, street lights

⇒ Used to measure exact intensity of light in science &

industry.

LIGHT EMITTING DIODE (LED):-

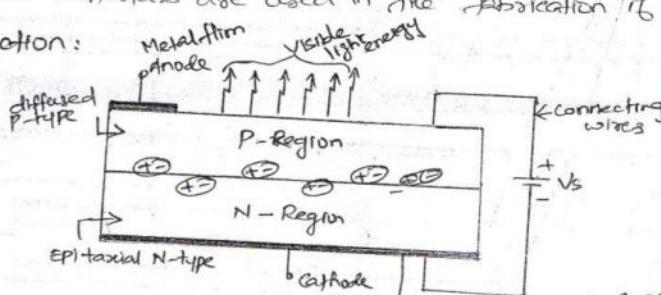
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LED is a Semiconductor PN Junction diode, designed to emit light when they are forward biased. When the ordinary Si or Ge semiconductor diodes are forward biased the electrons in N-type & holes in P-type move towards the junction and recombine and releasing the energy. This energy in Si & Ge diode is mostly converted into heat energy and very little is converted into light.

But in some compound semiconductors such as Gallium Arsenide (GaAs) & Gallium phosphide (GAP) large amount of light energy is released in the form of photons.

Hence these materials are used in the fabrication of LEDs.

⇒ Construction:



The P-type layer is formed from diffusion of semiconductor material, and the N-type layer is formed from epitaxial layer.

The metal film is used on the P-type layer to provide anode connection to the diode & gold film layer is coated on N-type to provide cathode connection.

PN Junction is formed between the P & n region. The metal contact to P-type material is much smaller than N-type, it is to allow the maximum no. of photons of light energy.

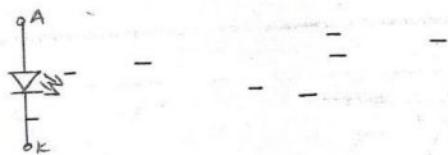
When the diode is forward biased, the recombination process starts at the PN junction. It emits light. There will be some absorption of energy inside the structure but major amount of photon will leave the material. It results visible light.



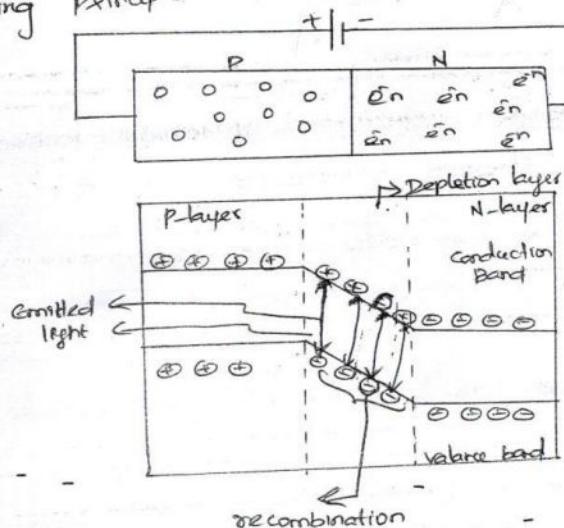
6

Gold film layer on N-type also provides reflection from the bottom surface of the diode. If the radiated light tends to hit bottom surface then that will be reflected from the bottom surface to the top. This increases LED's efficiency.

⇒ Symbol:



⇒ Working Principle:



Conduction band of P-layer contains holes and valence band of N-layer contains electrons. When the diode is forward biased, concentration of number of electrons and holes in the depletion layer will be increased.

These electron-hole pairs are recombining and emitting light.

The wavelength λ of the emitted light is proportional to the band gap energy ΔE .

$$\lambda = \frac{1240}{\Delta E} \text{ nm}$$



⇒ Applications :

Used in remote control systems such as TV or LCD remote.

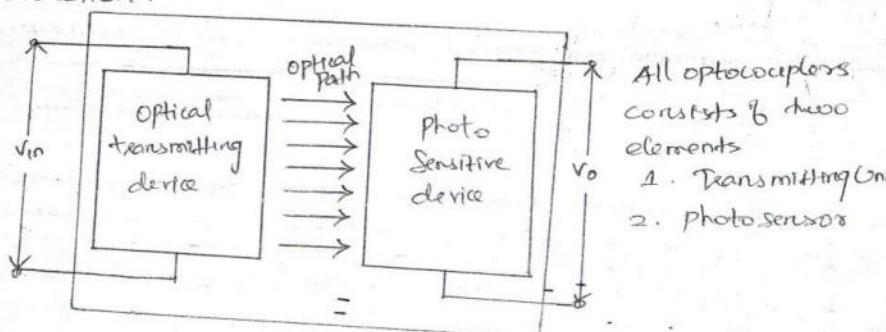
Used in electronic calculators, traffic signals, digital computers for displaying computer data, digital watches and automotive head lamps

Photocoupler (or) Optocouplers :-

It's also called as optoisolator. It is a device that uses a short optical transmission path to transfer signals between two isolated circuits

Optocouplers are sealed units that house an optical transmitting device and a photo sensitive device that are coupled together optically. The optical path may be air or a dielectric waveguide.

⇒ Construction :



Transmitting unit contains either a lamp, an LED or laser diode. Receiver unit may be a photodiode, photo transistor, photo FET, a photo SCR, photo DIAC, a photo TRIAC, a photo conductor etc.

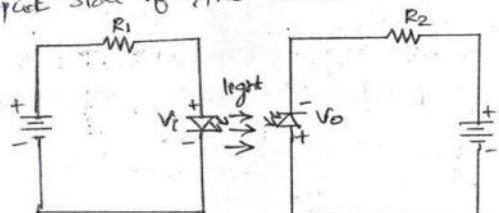
Both the elements are separated by a dielectric (nonconducting) barrier.

⇒ Working principle :

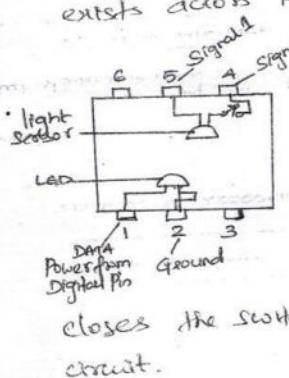
When the input current is applied to the LED, it switches ON and emits infrared light, the photo sensor then



detects this light and allows current to flow through the output side of the circuit. ⁸



When the LED is off, no current will flow through through the photodiode. By this method, the two flowing currents are electrically isolated. Here the LED and photodiode circuits are isolated electrically. LED is forward biased, photo diode is reverse biased and o/p exists across R2.



When the current is not being applied via pin 1, the LED is off, and the ckt connected to pin 1 + 5 is experiencing no current flow.

When power is applied to the 1st pin, the LED switches on, the sensor detects the light closes the switch and initiates current flow in the output circuit.

» Applications:

- Used in input, and output switching
- Switch-mode power supplies
- Signal isolation
- Power control
- PC/modem communications
- Controlling transistors and triacs



TRANSISTORS:

9

Transfer Resistor \Rightarrow Signals are transferred from low resistance circuit (input) into high resistance (output) circuit.

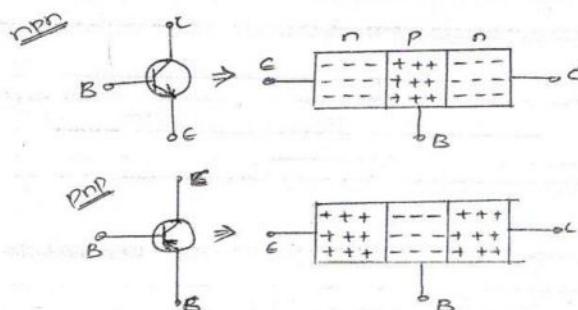
Transistor is a current driven, 3-terminal semiconductor device, which can be used to control the flow of electric current. The 3 terminals are Base, Emitter & Collector.

- A small amount of current in the Base, controls a larger current b/w collector and emitter. It can produce a stronger output signal; a voltage or current which is proportional to a weaker input signal. Thus a transistor can act as an amplifier.

3 terminals \Rightarrow Base, Emitter & Collector

2 junctions \Rightarrow Emitter-Base junction & Collector-Base junction

2 Basic types \Rightarrow n-p-n & p-n-p



Transistors are used to amplify and switch electronic signals and electric power.

Types of Transistors:

Bipolar Junction Transistor (BJT)

Unipolar Junction Transistor (UJT)

Field effect Transistor (FET)

Insulated Gate Bipolar Transistor (IGBT)

Avalanche

Thin-film

Darlington

Photo Transistor

$$\text{from } ① \Rightarrow I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$\text{Sub } I_B \text{ on } ② \Rightarrow I_C = \beta \left(\frac{V_{CC} - V_{BE}}{R_B} \right) \approx \frac{\beta V_{CC}}{R_B}$$

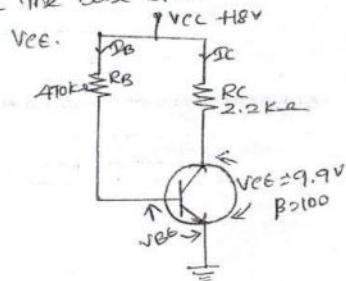
β = Transistor current gain

The values of collector current (I_{CQ}) & collector-emitter voltage (V_{CEQ}) represent operating point or Q-point. It's denoted by I_{CQ} & V_{CEQ} .

$$I_{CQ} = \beta \left(\frac{V_{CC} - V_{BG}}{R_B} \right)$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C$$

Prob 1 The base bias ckt is shown in the figure. Calculate I_B , I_C &



Given:

$$R_B = 470\text{k}\Omega, R_C = 2.2\text{k}\Omega, V_{CC} = 18\text{V}, \beta = 100$$

Solution

$$I_B = \frac{V_{CC} - V_{BG}}{R_B} = \frac{18 - 0.7}{470\text{k}\Omega} = 36.8\mu\text{A}$$

$$I_C = \beta I_B$$

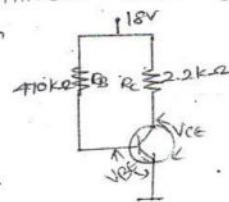
$$= 100 \times 36.8\mu\text{A}$$

$$= 3.68\text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C \\ = 18 - 3.68 \times 10^{-3} \times 2.2 \times 10^3 \\ = 9.9\text{V}$$

$I_B = 36.8\mu\text{A}$
$I_C = 3.68\text{mA}$
$V_{CE} = 9.9\text{V}$

Prob 2 calculate the maximum and minimum levels of I_C & V_{CE} for the base bias circuit in fig, when $h_{FE(\min)} = 50$ and $h_{FE(\max)} = 200$.



Given :

13

$$h_{FE(\min)} = 50, h_{FE(\max)} = 200$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18 - 0.7}{470 \times 10^3} = 36.8 \mu A$$

case (i) : $h_{FE(\max)} = 200$

$$I_C = h_{FE} I_B \text{ or } \beta I_B$$

$$= 200 \times 36.8 \mu A$$

$$= 7.36 mA$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 18 - 7.36 \times 10^{-3} \times 2.2 \times 10^3$$

$$= 1.8 V$$

case (ii) : $h_{FE(\min)} = 50$

$$I_C = h_{FE} I_B$$

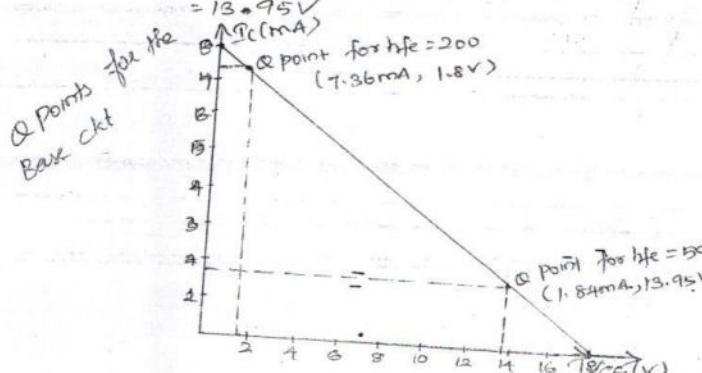
$$= 50 \times 36.8 \mu A$$

$$= 1.84 mA$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 18 - 1.84 \times 10^{-3} \times 2.2 \times 10^3$$

$$= 13.95 V$$



Advantages:

→ Simple circuit which uses very few components.

→ The operating point can be fixed anywhere in the active region.

Disadvantages:

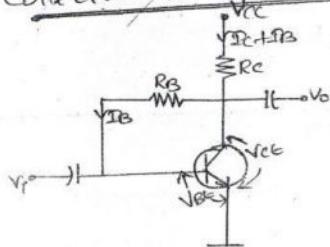
→ Collector current increases with increase in temperature. (i.e.)

Thermal stability is not provided by the circuit. So operating point is not maintained.

→ Stabilization of operating point is very poor.



2) Collector to base bias circuit:



14

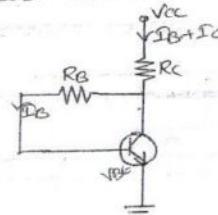
In collector to base configuration the base bias voltage is obtained from the collector of the transistor instead of the collector supply voltage.

This configuration is also called as feedback-bias configuration.

This ckt offers better stability of the operating point against variations in temp and transistor gain (B) due to negative feedback. In this ckt biasing resistor is connected between the collector and base of the transistor to provide a feedback path. Thus I_B flows through R_B & $(I_C + I_B)$ flows through R_C .

DC Analysis:

⇒ Base Circuit:



Apply KVL to base circuit

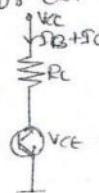
$$\begin{aligned} V_{BC} - R_C(I_B + I_C) - I_B R_B - V_{BE} &= 0 \\ V_{BC} - V_{BE} &= R_C(I_B + I_C) + I_B R_B \\ &= I_B R_C + I_C R_C + I_B R_B \\ &= I_B R_C + I_B R_B + B I_B R_C \\ &= I_B R_C (1 + B) + I_B R_B \end{aligned}$$

$$V_{BC} - V_{BE} = I_B [R_C + R_C (1 + B)]$$

$$I_B = \frac{V_{BC} - V_{BE}}{R_B + R_C (1 + B)}$$

$$I_C = B \left[\frac{V_{BC} - V_{BE}}{R_B + R_C (1 + B)} \right]$$

⇒ Collector's Ckt:



Apply KVL

$$V_{BC} - (I_C + I_B) R_C - V_{CE} = 0$$

$$V_{CE} = V_{BC} - (I_C + I_B) R_C$$

$$I_B \ll I_C$$

$$V_{CEQ} = V_{BC} - I_C R_C$$

The Q points

$$I_{CO} = B \left[\frac{V_{BC} - V_{BE}}{R_B + R_C (1 + B)} \right]$$

$$V_{CEQ} = V_{BC} - I_{CO} R_C$$



⇒ Advantages :

15

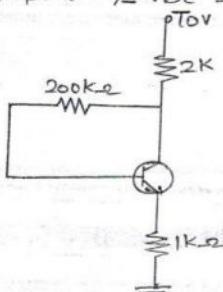
It provides stability to the operating point against variations in temperature and transistor gain B .

Disadvantage :

Due to negative feedback, the AC voltage gain of the amplifier is reduced.

Prob3 For the given ckt, determine the quiescent levels of I_B &

$$V_{CE} = 10V, B = 100, V_{BE} = 0.7V$$



Soln

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + B)(R_C + R_E)}$$

$$= \frac{10 - 0.7}{200 \times 10^3 + (1 + 100)(2 \times 10^3 + 1 \times 10^3)}$$

=

$$I_{CO} = B I_B$$

$$= 100 \times$$

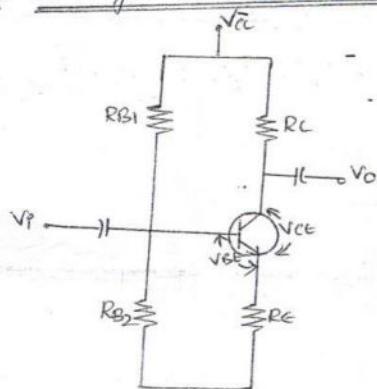
$$= 1.8mA$$

$$V_{CE} = V_{CC} - I_C R_C$$

=

$$= 4.675V$$

3) Voltage Divider Bias circuit :



The stability of the emitter.

In this circuit, biasing is provided by 3 resistors R_{B1} , R_{B2} & R_E .

R_{B1} & R_{B2} are acting as a potential divider giving a fixed voltage to Point B which is base.

This ckt offers improved stability against variation in the temperature & transistor gain.

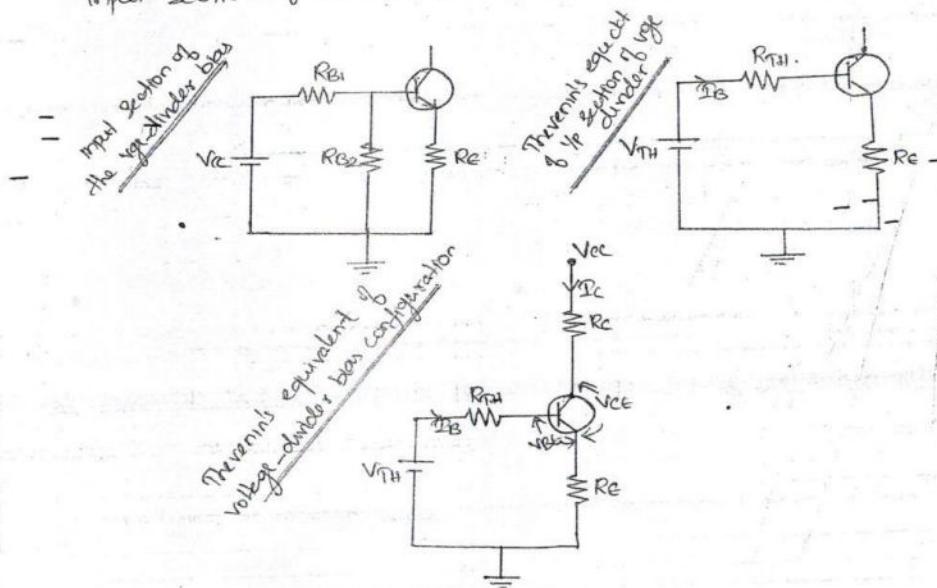


16

DC Analysis:

(i) Accurate method:

This method uses Thevenin's equivalent theorem. The input section of the circuit can be reduced.



$$R_{TH} = R_{B1} \parallel R_{B2} = \frac{R_{B1} R_{B2}}{R_{B1} + R_{B2}}$$

V_{TH} is the open ckt Thevenin's voltage and is equal to the voltage drop across the resistor R_{B2} .

$$V_{TH} = \frac{R_{B2} V_{cc}}{R_{B1} + R_{B2}}$$

Applying KVL to base-emitter loop of the circuit

$$V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0$$

$$\text{Sub } I_E = (1+B) I_B$$

$$V_{TH} - I_B R_{TH} - V_{BE} - (1+B) I_B R_E = 0$$

$$V_{TH} - V_{BE} = I_B [R_{TH}(1+B) R_E]$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH}(1+B) R_E}$$

If $V_{BE} \ll V_{TH}$

$$I_B = \frac{V_{TH}}{R_{TH}(1+B) R_E}$$



17

$$I_C = \beta \left[\frac{V_{TH} - V_{BE}}{R_{TH} + (1/\beta) R_E} \right]$$

Applying KVL to collector-emitter loop

$$V_{CE} - I_C R_C - V_E - I_E R_E = 0$$

$$I_C \approx I_E$$

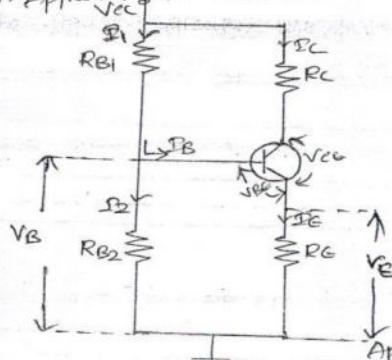
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

The Q points are given by

$$I_{CQ} = \beta \left[\frac{V_{TH} - V_{BE}}{R_{TH} + (1/\beta) R_E} \right]$$

$$V_{CEQ} = V_{CC} - I_{CQ} (R_C + R_E)$$

(ii) Approximate method:



If we assume $\beta_B \gg \beta_E$, we can neglect I_B & $I_E = I_C$

$$\therefore V_B = \frac{V_{CC} R_B 2}{R_B 1 + R_B 2}$$

$$V_{BE} = V_B - V_E$$

$$\therefore V_E = V_B - V_{BE}$$

$$I_E = I_C = V_E / R_E = \frac{V_B - V_{BE}}{R_E} = \beta_C$$

Apply KVL to collector-emitter loop

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$\boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)} \quad [\because I_C \approx I_E]$$

We can use approximate method when $(1/\beta_E) R_E \geq 10 R_2$

→ Advantages:

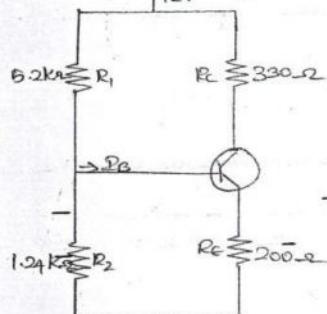
It provides excellent stabilization

→ Disadvantages:

The negative feedback introduced by existence of reverse biased diode reduces AC gain.



Prob 9 Draw the DC loadline & mark Q points for the following transistor configuration, obtain the Q points. Assume $\beta = 100$ 18



Solution:

Since $(\beta R_E) / R_E = 200$ which is greater than $10R_2$ we can use approximate method

$$\Rightarrow V_B = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{12 \times 1.24 \times 10^3}{(5.2 + 1.24) \times 10^3} = 2.31V.$$

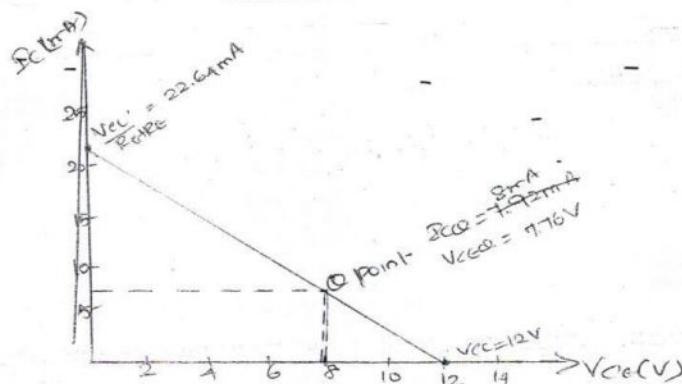
$$\Rightarrow V_E = V_B - V_{BE} = 2.31 - 0.7 = 1.61V$$

$$\Rightarrow I_E = V_E / R_E = \frac{1.61V}{200\Omega} = 8mA$$

$$I_E \approx I_C = 8mA$$

$$\Rightarrow V_{CE} = V_{CC} - I_C (R_E + R_C) \\ = 12 - 8 \times 10^{-3} (200 + 330) \\ = 12 - 8 \times 10^{-3} (530)$$

$$V_{CE} = 7.76V$$





Comparison of Various Biasing Techniques

19

Parameter	Base Bias	Collector to Base Bias	Voltage Divider Bias
Circuit			
Stability Required	Less stability	Medium stability	Highest stability
Feedback	Feedback is not used	voltage shunt negative feedback	current series negative feedback
Applications	Used in circuit where stability is not the important criterion	It is used in switching circuits	It is most preferred biasing circuit to prevent the transistor from going into saturation. It is used in circuit where stability requirements are moderate

OPERATIONAL AMPLIFIER APPLICATION CIRCUITS:

MULTIVIBRATORS USING IC-555 :

⇒ Operating modes of 555 Timer:

It has 3 modes

(i) ⇒ One Shot or Monostable mode: In this mode, output remains in a stable state until the arrival of a trigger input on which the output goes to a quasi-stable state.

(ii) ⇒ Astable Mode: This mode generates a continuous train of pulses of desired frequency and duty cycle. The circuit has 2 quasi stable states and output oscillates b/w these 2 states.

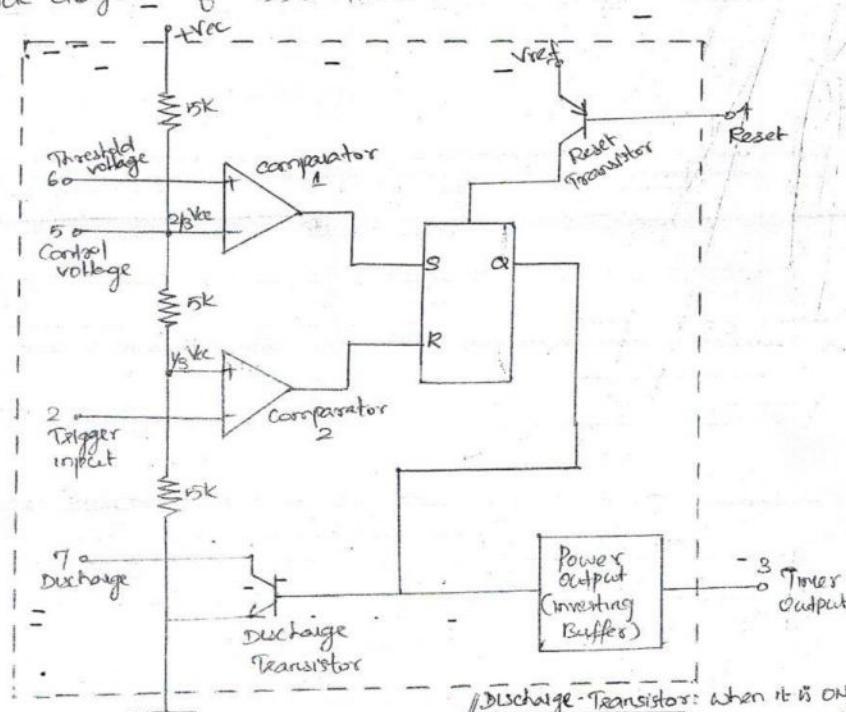
2 states

20

↳ Stable state: The output of the circuit is either high or low. It remains in its state until the trigger signal is applied.

↳ Quasi stable state: The output of the circuit is automatically changing after time period T .

⇒ Block diagram of 555 Timer:



Discharge Transistor: When it is ON, the capacitor connected across it will be discharged, when it is off capacitor will charge.

555 Timer consists of a pair of Analog comparators

3 equal values resistors (15k)

One SR flip-flop

2 transistors (1 is discharge 2nd is reset)

An output stage which is an inverting buffer.

3 resistors are connected between Vcc & ground.

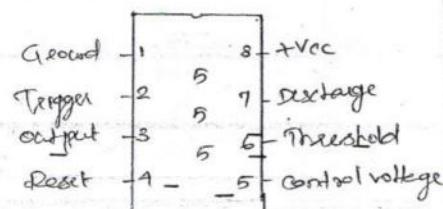
It is acting as a potential divider, establishing a voltage of $V_{TH} = \frac{2}{3}V_{CC}$ at the inverting input of comparator 1 and



$V_{LT} = \frac{1}{3} V_{CC}$ to the non inverting input of comparator 2.

$V_{FH}, V_{LT} \rightarrow$ Higher and lower threshold voltage.

→ Pin diagram:



Operation:

→ When the non-inverting input of comparator 1 rises above $\frac{1}{3} V_{CC}$, the output of this comparator is 1.

→ When the inverting input of comparator 2 drops below $\frac{1}{3} V_{CC}$, the o/p of this comparator is 1.

→ The outputs of the 2 comparators are connected to the input of SR flipflop, whose output drives the Power o/p stages; the discharge & reset transistors.

→ If the comparator 1 o/p is high, the FF o/p is also high. If the comparator 2 o/p is high, the FF o/p is low.

→ Since the o/p stage is an inverting buffer, the timer output is complement of the FF o/p.

→ The discharge transistor will be off when the FF output is low. It turns ON when the FF o/p is high.

→ When the reset pin is not used, it should be connected to V_{CC} .

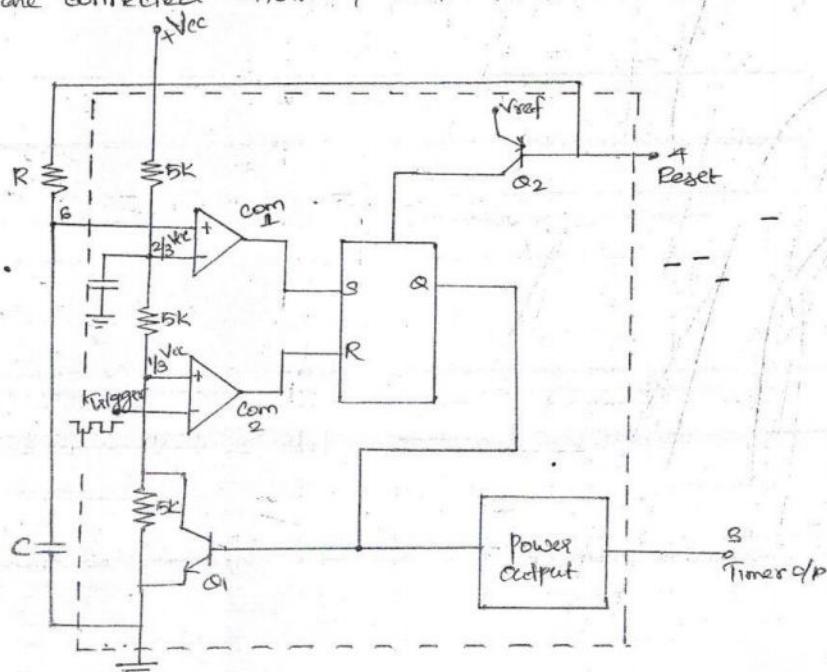
Types:

(i) Monostable Multivibrator Using 555 Timer:-

Monostable multivibrator has one stable state and one quasi stable state. The state is changed on the application of negative trigger pulse.

22

Timer will remain in quasi stable state for a predetermined duration. It is determined by a resistor R and capacitor C which are connected externally to the timer.



⇒ Operation:

	Stable State	Quasi Stable	Stable State	Quasi Stable
Timer Output	0	1	0	1

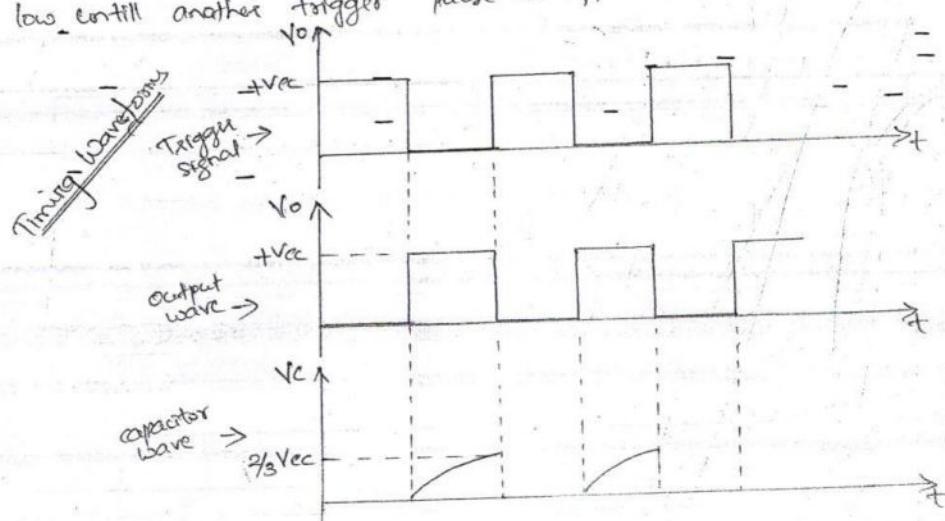
- i) Assume that the output of the 555 Timer is initially low. It implies that output of the flipflop is high and the discharge transistor Q1 is ON, and the capacitor Q is grounded.
- ii) When the negative trigger pulse is applied to pin 2, the inverting input goes below $\frac{1}{3} V_{cc}$ so that the comparator 2 goes high, forcing the o/p of flipflop to low.
- iii) It causes the timer output to go high.
- iv) Since flipflop output is low; Q turns off and the capacitor C begins to charge towards V_{cc} through Resistor R.



23

- v) when the capacitor voltage rises above $2/3 V_{CC}$, the output of comparator 1 becomes high & flipflop output high. It forces the timer output to go low.

- vi) It turns on the discharge transistor Q₁. Capacitor C discharges and the output of the monostable circuit remains low until another trigger pulse is applied to Pin2.



⇒ Expression for pulse width:

The equation for charging or discharging of capacitor is given by

$$V_C = V_f + (V_i - V_f) e^{-t/RC}$$

[V_f = final vge
 V_i = initial vge]

In this case $V_i = 0V$, $V_f = V_{CC}$, $t = RC$

$$\therefore V_C = V_{CC} + (0 - V_{CC}) e^{-t/RC}$$

$$= V_{CC} - V_{CC} e^{-t/RC}$$

$$V_C = V_{CC} [1 - e^{-t/RC}] \quad \text{①}$$

The output pulse width T_P of the monostable multivibrator is the time interval during which the external capacitor changes from 0 - $2/3 V_{CC}$. Hence sub $V_C = 2/3 V_{CC}$ at $t = T_P$

$$\text{①} \Rightarrow 2/3 V_{CC} = V_{CC} [1 - e^{-T_P/RC}]$$

$$e^{-T_P/RC} = 1 - 2/3$$

$$= 1/3$$



24

$$-TP/RC = \ln(1/3)$$

$$-TP/RC = \ln 1 - \ln 3$$

$$TP/RC = \ln 3$$

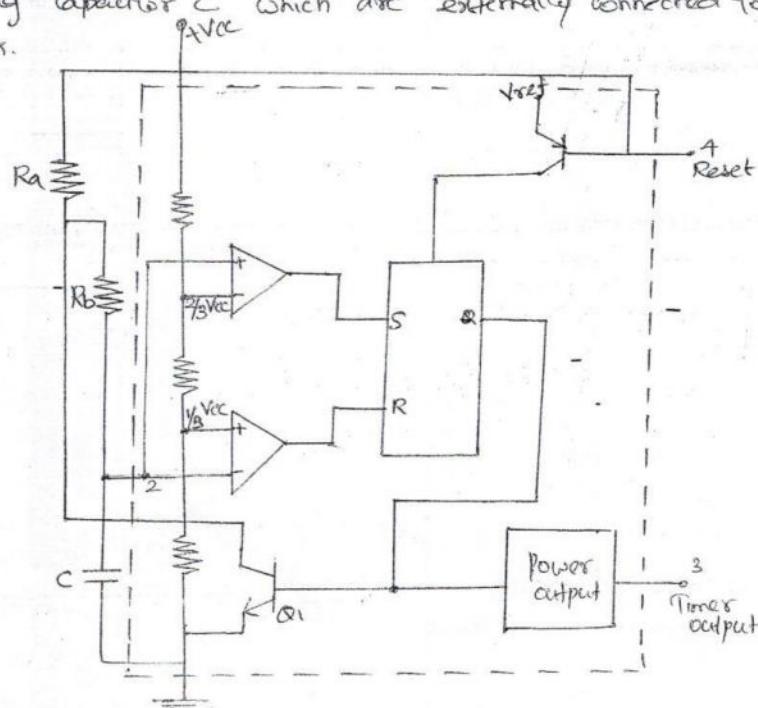
$$TP = RC \ln 3$$

$$\boxed{TP = 1.1RC}$$

(ii) Astable Multivibrator - Using 555 Timer:

- It is also called free-running multivibrator. Because it does not require an external trigger pulse to change its output. The output continuously changes between high and low states.

The time for which the output remains at high and low is determined by 2 timing resistors R_a & R_b and a timing capacitor C which are externally connected to 555 Timer.



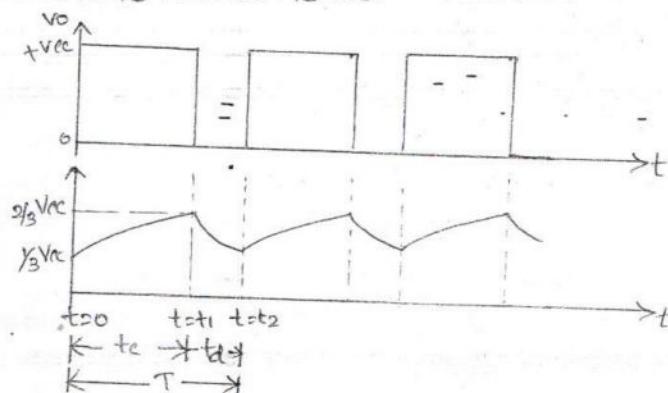
⇒ Operation :

	Quasi State 1	Quasi State 2	Quasi State 1	Quasi State 2
Timer output	1	0	1	0



25

- i) Assume that initially the 555 timer output is in high state and capacitor C is uncharged. When timer output is 1, flip-flop output is 0, discharge transistor is OFF and the capacitor starts charging towards Vcc through Ra & Rb.
- ii) When the capacitor voltage rises above $2/3 V_{cc}$, it causes the comparator 1 output to go high. Hence the flip-flop output is high and the timer o/p is low. This is quasi stable state 2.
- iii) Since the flip-flop output is high, discharge transistor switches ON, and the capacitor C discharges through Rb towards 0V.
- iv) When the capacitor voltage drops below $1/3 V_{cc}$, the o/p of comparator 2 goes high and comparator 1 to low. As a result, the output of FF goes low and timer output is high.
- v) The discharge transistor Q1 turned off and the capacitor C charges again towards $2/3 V_{cc}$.
- vi) Here the capacitor charges from $1/3 V_{cc}$ to $2/3 V_{cc}$ & discharges from $2/3 V_{cc}$ to $1/3 V_{cc}$.





⇒ Expression for the frequency of the output v_o:

⇒ Capacitor charging time (t_c):

During this time, the time interval between time t=0 & t=t₁.

Here the capacitor charges from $\frac{1}{3}V_{cc}$ to $\frac{2}{3}V_{cc}$ through R_a & R_b.

Here V_i = $\frac{1}{3}V_{cc}$, V_f = V_{cc}, C = (R_a+R_b)C, t = t₁-0 = t_c

$$V_c = V_f + (V_i - V_f) e^{-t/c}$$

$$V_c = V_{cc} + (\frac{1}{3}V_{cc} - V_{cc}) e^{-t_1/(R_a+R_b)C}$$

$$= V_{cc} + \left[\frac{V_{cc} - \frac{1}{3}V_{cc}}{3} \right] e^{-t_1/(R_a+R_b)C}$$

$$= V_{cc} + [-\frac{2}{3}V_{cc}] e^{-t_1/(R_a+R_b)C}$$

$$V_c = V_{cc} [1 - \frac{2}{3} e^{-t_1/(R_a+R_b)C}] \quad \text{--- (1)}$$

at the end of the charging time t = t₁ = t_c & V_c = $\frac{2}{3}V_{cc}$

$$\therefore (1) \Rightarrow \frac{2}{3}V_{cc} = V_{cc} [1 - \frac{2}{3} e^{-t_c/(R_a+R_b)C}]$$

$$\frac{2}{3} e^{-t_c/(R_a+R_b)C} = 1 - \frac{2}{3} = \frac{1}{3}$$

$$e^{-t_c/(R_a+R_b)C} = \frac{1}{3} \times \frac{3}{2} = \frac{1}{2}$$

$$\frac{-t_c}{(R_a+R_b)C} = \ln 1 - \ln 2$$

$$\frac{-t_c}{(R_a+R_b)C} = -0.693$$

$$t_c = C(R_a+R_b) 0.693$$

$$\boxed{t_c = t_{on} = 0.693(R_a+R_b)C}$$

⇒ Capacitor discharging time (t_d):

During this time, the time interval is between t=t₁ & t=t₂. The capacitor discharges from $\frac{2}{3}V_{cc}$ to $\frac{1}{3}V_{cc}$ through Resistor R_b.

So V_i = $\frac{2}{3}V_{cc}$, V_f = 0V, C = R_bC, t = t₂-t₁ = t_d

$$\text{Now } V_c = 0 + (\frac{2}{3}V_{cc} - 0) e^{-\frac{(t_2-t_c)}{R_bC}}$$

27

$$V_C = \frac{1}{3} V_{CC} e^{-\frac{(t_2-t_1)}{RBC}} \quad \text{--- (2)}$$

at the end of the discharging time $t = t_2 = T$

$$V_C = \frac{1}{3} V_{CC}$$

$$\therefore \text{--- (2)} \Rightarrow \frac{1}{3} V_{CC} = \frac{1}{3} V_{CC} e^{-\frac{(T-t_1)}{RBC}}$$

$$t_1 + t_d = T, T - t_1 = t_d$$

$$e^{-t_d/RBC} = \frac{1}{3} \times \frac{2}{3} = \frac{1}{3}$$

$$-\frac{t_d}{RBC} = \ln 1 - \ln 2$$

$$\frac{t_d}{RBC} = \ln 2$$

$$\boxed{t_d = 0.693 RBC}$$

$$\begin{aligned} T &= t_1 + t_d = 0.693 (R_a + R_b) C + 0.693 RBC \\ &= 0.693 R_a C + 0.693 R_b C + 0.693 RBC \\ &= 0.693 R_a C + 2 \times 0.693 RBC \end{aligned}$$

$$\boxed{T = 0.693 [R_a + 2R_b] C}$$

$$\text{freq } f = \frac{1}{T} = \frac{1.44}{(R_a + 2R_b)C}$$

\Rightarrow Duty cycle:

The ratio of the time duration for which the output is high (t_{on}) to the total time period T is called duty cycle of the astable multivibrator.

$$\text{Duty cycle } D = \frac{t_{on}}{T} \text{ or } \frac{t_{on}}{T}$$

$$D = \frac{0.693 (R_a + R_b) C}{0.693 (R_a + 2R_b) C}$$

$$\% D = \frac{R_a + R_b}{R_a + 2R_b} \times 100$$

To obtain a 50% duty cycle, we need to set $R_a = 0$, then $\% D = \frac{0 + R_b}{0 + 2R_b} \times 100 = \frac{R_b}{2R_b} \times 100 = 50\%$

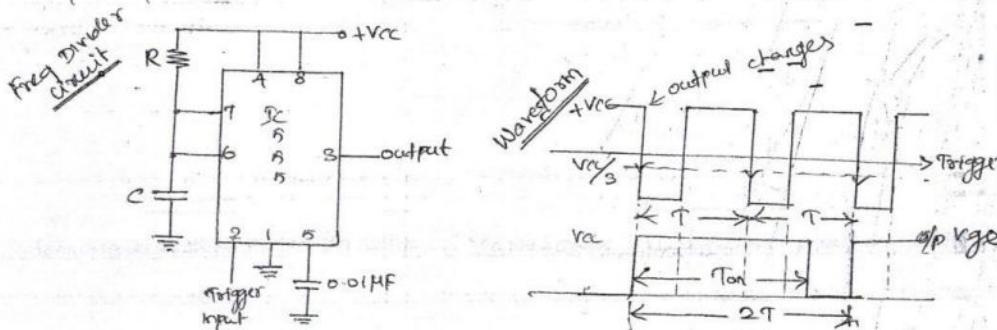
28

→ Applications of a Monostable Multivibrator:

Few important applications of Monostable M.V are

- Frequency divider
- Missing pulse detector
- Pulse width modulator
- Pulse position modulator

i) Frequency divider:



In the waveform, the o/p goes high corresponding to the first negative going trigger pulse. The on time of o/p wave is given as $T_{on} = 1.1 RC$.

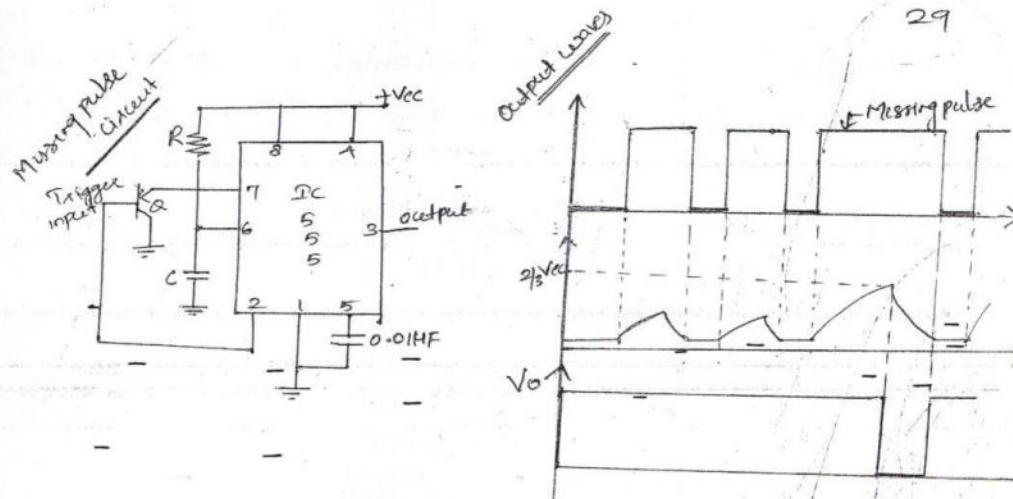
From the waveforms it is noticed that T_{on} is kept slightly longer than the time period T of trigger input signal.

This operation of frequency division is possible because - multivibrator cannot be triggered during the on time T_{on} . Therefore the 2nd negative going trigger pulse is neglected by monostable.

The frequency of trigger input waveform is $(1/T)$ and frequency of output voltage is $1/2T$. Thus frequency division by 2 has taken place.

2 Missing pulse detector:

When trigger input is low, due to the comparator and flip-flop action, the transistor Q is forward biased (ON). The capacitor connected across it is discharged and the final output goes high.



29

As long the trigger pulse keeps coming at pin 2, the output remains high.

However if pulse misses, the trigger input is high and transistor ~~K2~~ is in cut off. The output goes low after time T of the monostable.

Applications:

This type of circuit can be used to detect missing heartbeat.

It can also be used for speed control and measurement. If input trigger pulses are generated from a rotating wheel, the circuit tells when the wheel speed drops below a predetermined value.

Prob. For a monostable multivibrator time delay $T = 100ms$ and resistance $R = 105k\Omega$, calculate the capacitor value.

Given: $T = 100ms$, $R = 105k\Omega$

Solution: W.K.T pulse width $T = 1.1RC$

$$C = \frac{T}{1.1R} = \frac{100 \times 10^{-3}}{1.1 \times 105 \times 10^3}$$

$$C = 0.865 \mu F$$



Prob. Design a monostable multivibrator circuit using 555 Timer to produce an output pulse of 20sec width.

Solution:

The output pulse $T_{on} = 20 \text{ sec}$

$$\text{WKT } T = 1.1RC$$

$$\text{Assume } C = 150\text{ nF}$$

$$20 = 1.1R \times 150 \times 10^{-9}$$

$$R = \frac{20}{1.1 \times 150 \times 10^{-9}}$$

$$R = 121.21 \text{ k}\Omega$$

Prob. 3. Find the resistive element value to generate T_0 time delay, using 555 Timer as a monostable multivibrator

Assume $C = 0.47\text{ nF}$.

Solution:

$$T = 1.1RC$$

$$10 \times 10^{-3} = 1.1 \times R \times 0.47 \times 10^{-9}$$

$$R = \frac{10 \times 10^{-3}}{1.1 \times 0.47 \times 10^{-9}}$$

$$R = 19.34 \text{ k}\Omega \quad \text{We can choose standard value as}$$

$$R = 18 \text{ k}\Omega$$

Prob. 4. Design a timer that can turn on a heater immediately after pressing the button, and it should hold the heater in on-state for 10 seconds.

Solution:

The relay coil should be energized for 10 seconds to hold heater on. So T_{on} is 10 seconds and choosing $C = 47\text{ nF}$

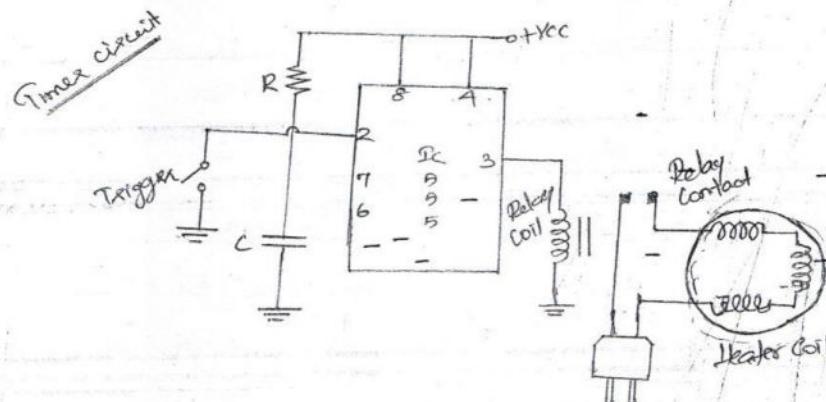
$$\text{WKT } T_{on} = 1.1RC$$

$$10 = 1.1RC$$

31

$$R = \frac{60}{1.1 \times 10^{-6}} = 54.54 \text{ k}\Omega$$

$$R = 193.42 \text{ k}\Omega$$

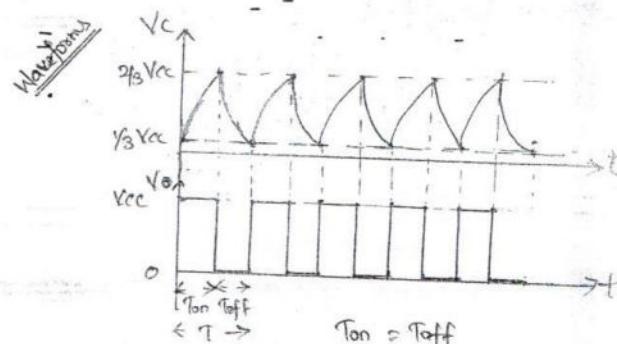
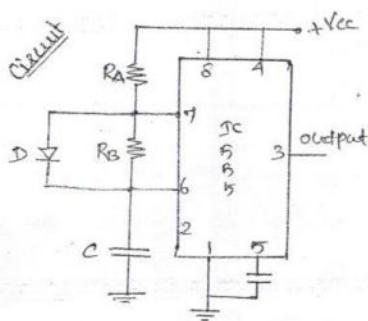


Applications of Astable Multivibrator:

555 timer in astable mode can be used for many applications. Such as

- square wave oscillator
- free running ramp generator
- voltage controlled oscillator (vco)
- FSK Generator etc

(i) Square wave oscillator (generator):-



With the astable circuit, diode D is connected across RB. During ON time, the diode is forward biased and passes the resistor RB, thus charging of capacitor takes place through RA & D.

82

Expression for on time, assuming ideal diode is given by

$$T_{on} = T_C = 0.693 R_A C$$

During discharging time T_D , the diode is reverse biased and discharging through R_B

$$T_{off} = T_D = 0.693 R_B C$$

For a wave to be perfect square wave

$$T_C = T_D$$

$$\therefore 0.693 R_A C = 0.693 R_B C$$

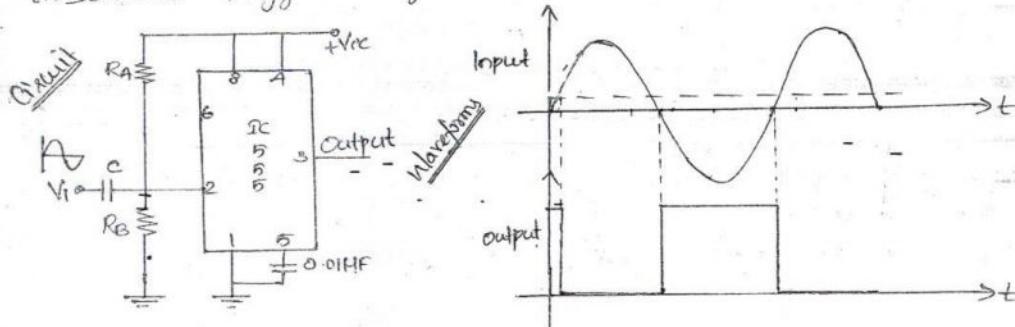
$\therefore R_A = R_B$. Hence R_A & R_B should be equal.

$$\text{Frequency of oscillator } f_0 = \frac{1}{T} = \frac{1}{T_C + T_D}$$

$$= \frac{1}{0.693(R_A + R_B)C}$$

$$f_0 = \frac{1.41}{(R_A + R_B)C}$$

(ii) Schmitt Trigger using IC-555:



In Schmitt trigger using IC-555, Pin 2 & 6 are connected together and the dc voltage is adjusted to $\frac{V_{cc}}{2}$ by means of equal resistor R_A & R_B .

The input is applied to the pin 2 through coupling capacitor C. This voltage will be $\frac{1}{2} V_{cc}$ of input voltage.

As soon as v_{ge} at pin 6 exceeds $\frac{2}{3} V_{cc}$, the upper comparator output goes high setting the SR FF bit.

33

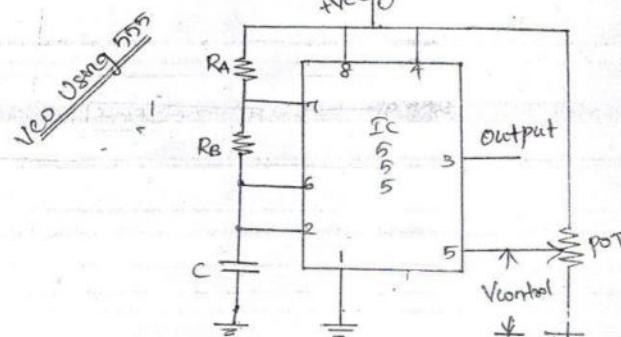
$S=1$ and $\phi=1$. Thus upper trigger point (UTP) is at $2/3 V_{cc}$.

- The output will remain low as long as the voltage at pin 2 & 6 is higher than $1/3 V_{cc}$, the lower comparator op-amp goes high and reset the flip-flop and $\phi=0$.

When voltage at pin 2 & 6 goes below $1/3 V_{cc}$ then the lower trigger point (LTP) is at $1/3 V_{cc}$.

- Thus for a sine wave input, we get a perfect square output.

(iii) 555-Timer as a voltage controlled oscillator (VCO):-



This circuit is also called as voltage to frequency converter. Because the output frequency can be changed by changing the input voltage.

Operation:

- Pin 5 is connected to a potentiometer.
- Initially the control voltage is not at $2/3 V_{cc}$, but when increases and exceeds $2/3 V_{cc}$, the capacitor C charges and changes the output state.
- As charging time constant $(R_A + R_B)C$ is constant, capacitor will take longer time to charge to the required voltage.
- Similarly it will take longer time to discharge to $1/3 V_{cc}$. Thus the total time $T = T_C + T_D$ will increase and output frequency will decrease.



→ When V_c reduces below $2/3 V_{cc}$ the output frequency will increase.

→ The frequency f_o is a function of V_c applied at pin 5 and circuit works as VCO.

Prob1. For an astable circuit $R_1 = 22\text{ k}\Omega$, $R_2 = 30\text{ k}\Omega$ and $C = 0.5\text{ nF}$.

- Find on & off period of the output waveform shown in figure.



Solution:

→ The on period corresponds to charging period of a capacitor and charging takes place through resistors R_1 & R_2 .

$$\therefore T_C = T_{on} = 0.693(R_a + R_b)C$$

$$= 0.693(22+30) \times 10^3 \times 0.5 \times 10^{-9}$$

$$\boxed{T_{on} = 18\text{ ms}}$$

→ The off period corresponds to discharging time (T_D) of the capacitor and discharging taken place through R_2 only.

$$\therefore T_D = T_{off} = 0.693 R_b C$$

$$= 0.693 \times 30 \times 10^3 \times 0.5 \times 10^{-9}$$

$$\boxed{T_{off} = 10.395\text{ ms}}$$

Prob2. A 555 Timer is configured to operate in astable mode with $R_A = 5\text{ k}\Omega$, $R_B = 5\text{ k}\Omega$ and $C = 0.01\text{ nF}$, Determine the frequency of the output and duty cycle.

Solution:

$$R_A = 5\text{ k}\Omega, R_B = 5\text{ k}\Omega, C = 0.01\text{ nF}$$

$$\Rightarrow \text{freq } f = 1/T = \frac{1.44}{(R_A + 2R_B)C}$$

$$= \frac{1.44}{5 \times 10^3 + 2 \times 5 \times 10^3 \times 0.01 \times 10^{-9}}$$



$$\boxed{f = \frac{1}{(R_A + 2R_B)C}} \quad 9600 \text{ Hz} \rightarrow 9.6 \text{ kHz}$$

$$\begin{aligned} \Rightarrow \text{Duty cycle } D &= \frac{R_A + R_B}{R_A + 2R_B} \\ &= \frac{15 \times 10^3 + 5 \times 10^3}{15 \times 10^3 + 2(5 \times 10^3)} \\ &\boxed{D = 66.66\%} \end{aligned}$$

Prob3. Design an astable multivibrator using 555 timer for a frequency of 2 kHz and a duty cycle of 75%.
Assume $C = 0.1 \mu F$.

Given : $f = 2 \text{ kHz}$, duty cycle = 75%, $C = 0.1 \mu F$

Solution : $T_{on} = 0.693(R_A + R_B)C$

$$T_{off} = 0.693 R_B C$$

$$T = T_{on} + T_{off} = 0.693(R_A + 2R_B)C$$

$$D = \frac{T_{on}}{T} = \frac{0.693(R_A + R_B)C}{0.693(R_A + 2R_B)C}$$

$$D = \frac{R_A + R_B}{R_A + 2R_B} = \frac{3}{4} = 0.75$$

$$\therefore 3(R_A + 2R_B) = 4(R_A + R_B)$$

$$3R_A + 6R_B = 4R_A + 4R_B$$

$$2R_B = R_A$$

$$R_B = \frac{R_A}{2}$$

Substituting R_B in expression of T

$$T = 0.693 \left(R_A + 2 \times \frac{R_A}{2} \right) C$$

$$T = 0.693 (2R_A)C$$

$$f = \frac{1}{T}$$

$$2 \times 10^3 = \frac{1}{2 \times 0.693 \times R_A \times 0.1 \times 10^{-6}}$$

$$R_A = \frac{1}{2 \times 0.693 \times 2 \times 10^3 \times 0.1 \times 10^{-6}}$$

=

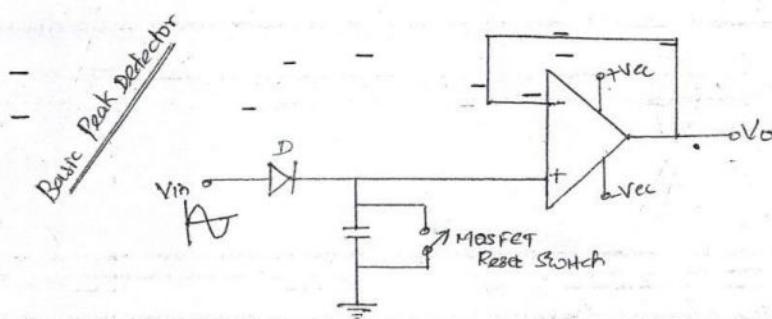
$$\therefore R_B = \frac{R_A}{2} = \frac{1}{2}$$

=

PEAK DETECTOR CIRCUIT:

36

The peak value of non-sinusoidal waveforms such as square, triangular, sawtooth pulse etc, can not be measured using conventional voltmeters. Hence to measure the peak of non-sinusoidal waveforms a peak-detector ckt is used.



Peak detector ckt produces a voltage at the output side equal to peak value of the input signal.

This circuit follows the peak of an input signal and stores the highest peak value in terms of voltage on a capacitor.

If more peak occurs in an input signal, the new peak value gets stored until the capacitor gets discharged.

Operation:

→ When the positive of input signal V_{in} is given, the diode gets forward biased and the capacitor C charges to the peak value of input signal through the diode D.

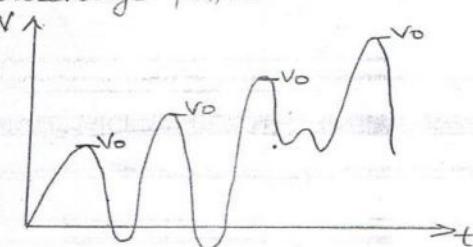
→ The capacitor remains charged to the peak value of input unless and until discharged with the help of MOSFET switch.

→ Opamp is connected as voltage follower and its output will be equal to the drop across capacitor which is positive peak of applied voltage. For negative cycle of input, the diode is reverse biased and the capacitor discharges.

→ During the positive half cycle of the signal, the diode D is forward biased. The capacitor C charges to the positive peak from the output of the op-amp through the ON resistance of the forward biased diode.

→ During the negative half cycle, the diode gets reverse biased and the capacitor discharges through the load resistance R_L .

→ The value of resistance R_L is much greater than forward biased diode's ON-resistance. This is to allow a discharge path.



→ The charging time constant

$$CR_f \leq T/10$$

→ The discharging time constant

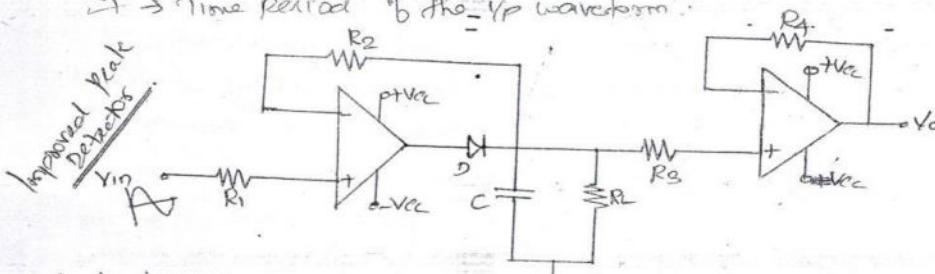
$$CR_L \geq 10T$$

The RL Time constant controls the response time. The RT is nothing but the time needed to respond to a decreasing peak amplitude of the input signal.

R_f → feedback resistor

R_L → load resistor

T → Time Period of the input waveform



Applications:

Used in amplitude modulation in communication and in test and measurement instrumentation applications.



SCHMITT TRIGGER: (Regenerative Comparator) :-

38

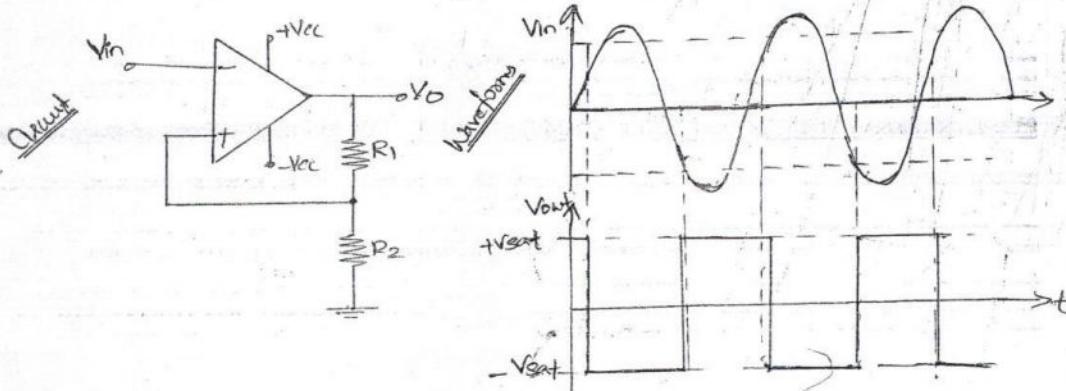
Basic comparators can be converted into a schmitt trigger very easily by adding some positive feedback to the operational amplifiers or comparator circuit. Schmitt trigger ckt is a fast-operating voltage level detector.

2 types :

Inverting schmitt trigger

Non inverting schmitt trigger

(i)-Inverting schmitt trigger:-



The input voltage V_{in} is applied to the inverting input terminal and the feedback voltage goes to the non-inverting terminal.

Let us assume that the input voltage at inverting is slightly positive than feedback voltage at the non-inverting. Since the inverting is positive than non-inverting, this produces a negative output voltage.

Now due to negative output, the feedback voltage from voltage divider circuit is also negative and available at the non-inverting input.

If the input voltage becomes more negative than reference feedback, the output is driven into the positive saturation at $+V_{sat}$.

39

The upper and lower trigger points can be written as

$$UTP = \frac{R_2}{R_1+R_2} V_{sat}$$

$$LTP = \frac{R_2}{R_1+R_2} (-V_{sat})$$

$$V_{HYS} = UTP - LTP$$

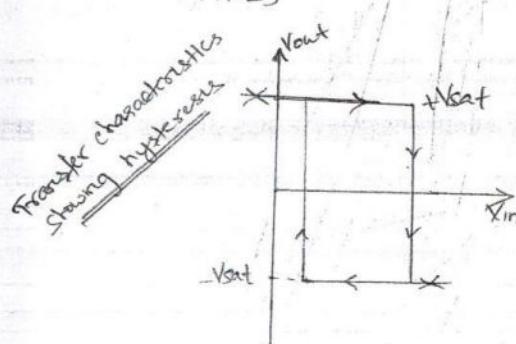
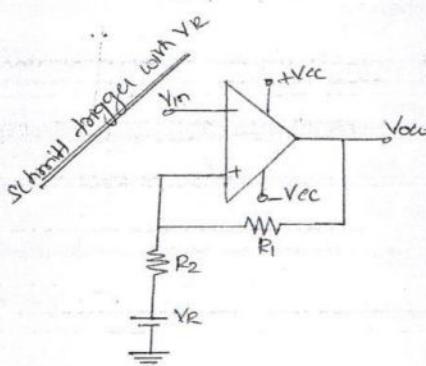
$$= \frac{R_2}{R_1+R_2} V_{sat} - \frac{R_2 (-V_{sat})}{R_1+R_2}$$

$$= 2 \left(\frac{R_2}{R_1+R_2} \right) V_{sat}$$

$$= 2 \beta V_{sat}$$

The voltage at which the output switches from $+V_{sat}$ to $-V_{sat}$ & $-V_{sat}$ to $+V_{sat}$ are called Upper & Lower trip points. And the difference between the 2 trigger points is called hysteresis.

$$\therefore \beta = \frac{R_2}{R_1+R_2}$$



When $V_o = +V_{sat}$ & the reference

UTP is given by

$$UTP = \frac{(V_{sat} - VR) R_2}{R_1 + R_2} + VR$$

$$= \frac{V_{sat} R_2}{R_1 + R_2} - \frac{VR R_2}{R_1 + R_2} + \frac{VR (R_1 + R_2)}{R_1 + R_2}$$

$$= \frac{V_{sat} R_2}{R_1 + R_2} - \frac{VR R_2}{R_1 + R_2} + \frac{VR R_1}{R_1 + R_2} + \frac{VR R_2}{R_1 + R_2}$$

$$= \beta V_{sat} + \frac{R_1 VR}{R_1 + R_2}$$

When $V_o = -V_{sat}$ & the reference voltage, LTP is given by

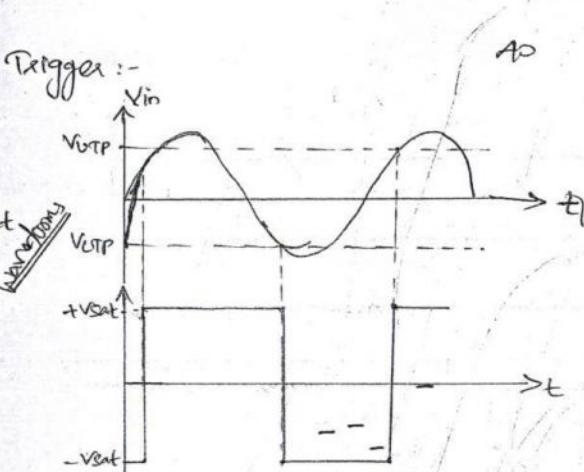
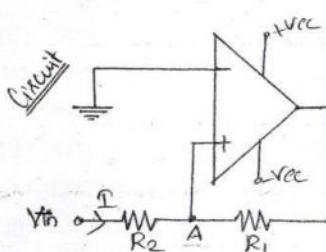
$$LTP = \frac{(-V_{sat} - VR) R_2}{R_1 + R_2} + VR$$

$$= -\beta V_{sat} + \frac{R_1 VR}{R_1 + R_2}$$

If VR is positive the loop is shifted to right side,
if VR is negative, the loop is shifted to left side.



ii) Non-inverting Schmitt Trigger :-



The feedback is given at non-inverting terminal. The inverting terminal is grounded and the input voltage is applied to non-inverting terminal of op-amp.

Let us assume that the output is negatively saturated. Then the feedback voltage is also negative ($-V_{sat}$). This feedback voltage will hold the output in negative saturation, until the input voltage becomes positive enough to make voltage positive.

V_A is the V_{ge} at Point A.

$$\therefore V_A = I R_2$$

- Since no current passes through op-amp entire current

- flows through R_2 .

$$\therefore I = \frac{V_0}{R_1} = \frac{+V_{sat}}{R_1}$$

When V_{in} becomes positive and its magnitude is greater than $(R_2/R_1)V_{sat}$, then the output switches to $+V_{sat}$.

$$\therefore V_{OTP} = \frac{R_2 V_{sat}}{R_1}$$

When the output is in positive saturation, feedback voltage is positive. To switch the output state, the input voltage has to become more negative, then the output changes from positive saturation to negative saturation voltage.

41

When V_{in} becomes negative and its magnitude is greater than $\frac{R_2}{R_1} V_{sat}$, then the output switches to $-V_{sat}$.

$$\therefore UTP = \left(-\frac{R_2 V_{sat}}{R_1} \right)$$

The difference

$$V_{TH} = UTP - LTP = \frac{R_2 V_{sat}}{R_1} + \frac{R_2 V_{sat}}{R_1} \\ = 2 \left(\frac{R_2}{R_1} \right) V_{sat}$$

$$V_{TH} = 2B V_{sat}$$

Applications:

- Used in Digital to analog conversion
- Level detection
- Line reception

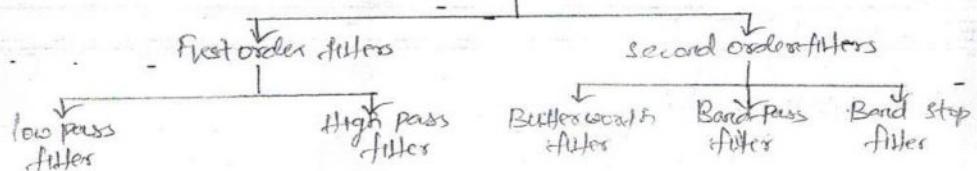
ACTIVE FILTERS:

Filters are circuit that passes only a specified range of signal frequencies and cutoff frequencies outside of this range.

Active filters \rightarrow Used for active devices such as transistor, opamps

Passive filters \rightarrow Used for passive devices

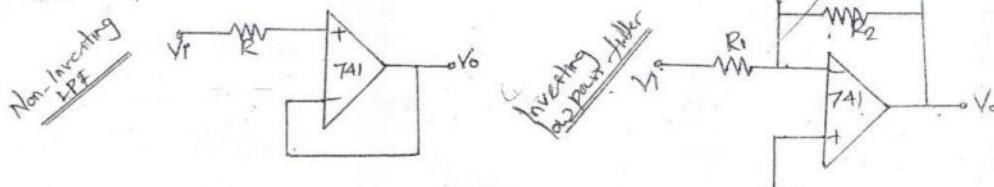
Active filters

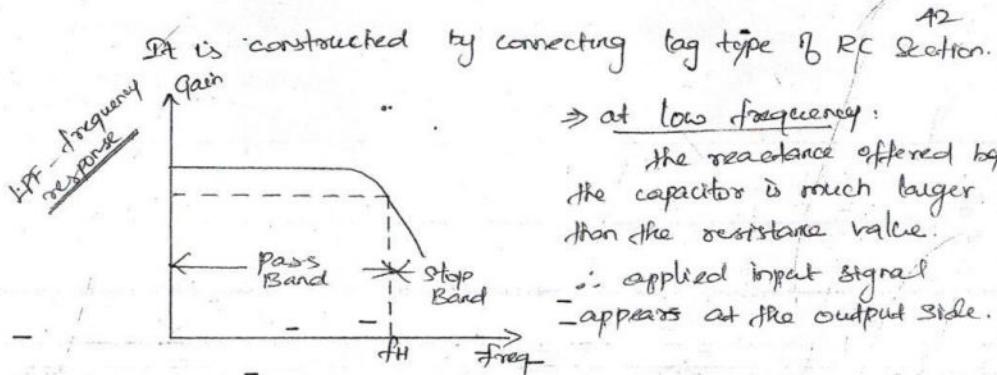


Order of an active filter is determined by no. of RC sections used in the filter.

(in first order filter):

a) Low pass filter (LPF):-





→ at high frequency:

The capacitive reactance becomes much smaller than the resistance, thus the output will be nearly zero.

To make the capacitive reactance equal to the resistance value, the output is 0.907 times the input.

Here a low pass filter, passes signals with a frequency lower than a certain cutoff frequency and attenuates signals with frequencies higher than the cutoff frequency.

Cut off freq $f_c \Rightarrow$ It is a boundary in a system's frequency response at which signal flowing through the system begins to be attenuated.

Reactance \Rightarrow Measure the opposition of the circuit element to a change of electric current or voltage due to inductance or capacitance.

Cut off freq of LPF

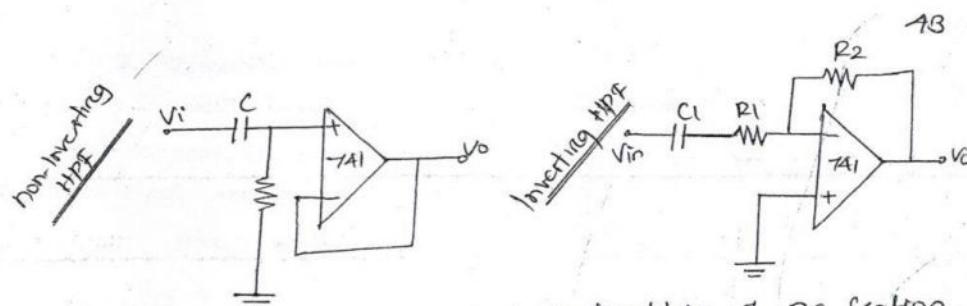
$$\text{Non inverting} \Rightarrow f_c = \frac{1}{2\pi R C}$$

$$\text{Inverting} \Rightarrow f_c = \frac{1}{2\pi R_2 C}$$

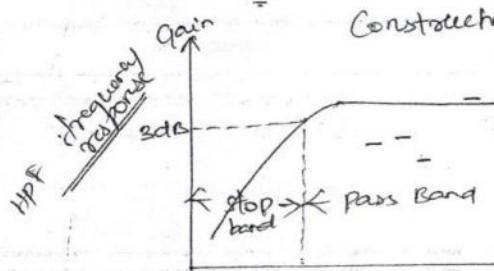
$$\text{Bandgain of LPF} \Rightarrow A_v = -R_2/R_1$$

b) High Pass filter (+HPF):-

A HPF, passes signals with a frequency higher than a certain cutoff frequency and attenuates signals with frequencies lower than the cutoff frequency.



Constructed by lead type of RC section



\Rightarrow Cut off frequency f_c

$$\text{non inverting HPF, } f_c = \frac{1}{2\pi RC}$$

$$\text{inverting HPF, } f_c = \frac{1}{2\pi R_1 C_1}$$

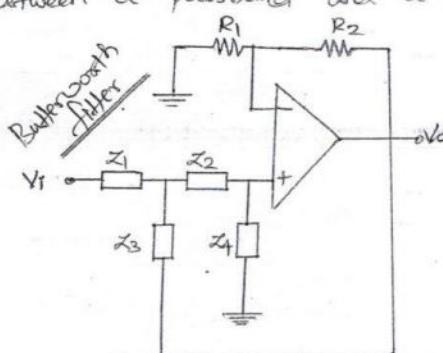
$$\Rightarrow \text{Band gain } Av = -R_2/R_1$$

(ii) Second Order filter:

a) Butterworth filter:

It is also called as maximally flat filter. It offers flat pass and stop band response but it has relatively sluggish roll-off. Thus it requires a higher order to implement.

Roll off \Rightarrow is the steepness of a transmission function with frequency particularly in filter circuits in transmission between a passband and a stopband.



\Rightarrow If $Z_1 = Z_2 = R$

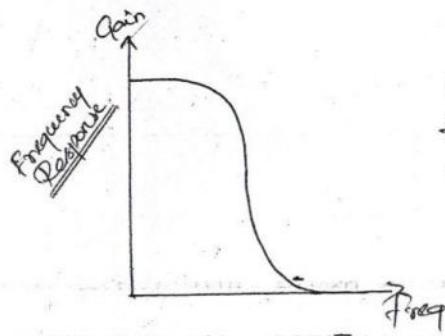
$$Z_3 = Z_4 = C$$

We get a 2nd order LPF

\Rightarrow If $Z_1 = Z_2 = C$

$$Z_3 = Z_4 = R$$

We get a 2nd order HPF



44

The Butterworth filter is a type of signal processing filter designed to have as flat a frequency response as possible in the passband.

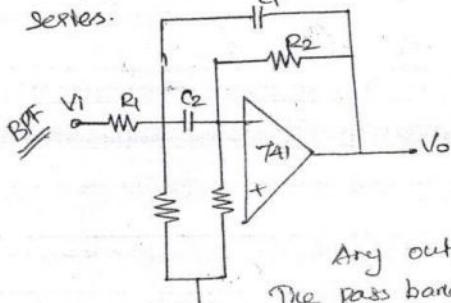
The cutoff frequency is given by

$$f_c = \frac{1}{2\pi R C}$$

$$\text{Gain } Av = 1 + R_2/R_1$$

b) Band Pass filter:

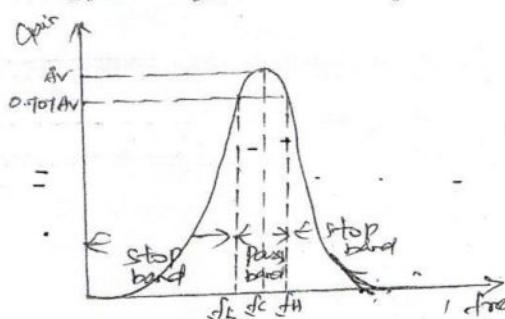
- It is obtained by cascading the HPF & LPF section in series.



A BPF is a frequency selector. It allows one particular band of frequencies to pass. Thus the pass band is between the 2 cutoff frequencies f_{H} & f_{L} .

Any outside frequencies gets attenuated.

The pass band which is between f_{H} & f_{L} is called Bandwidth of the filter.



Operation:

→ at low freq: C_1 & C_2 offers very high reactance, hence the $1/f$ signal is prevented. So no output.

→ at high freq: The output is shorted to the inverting input which converts the circuit to an inverting amplifier with zero gain. ∴ no output

→ at both high & low: output is zero

→ at some intermediate band frequencies, the gain is provided by the circuit.

The resonant freq $f_r = \frac{2\pi}{2\pi R_2 C}$, Q = Quality factor

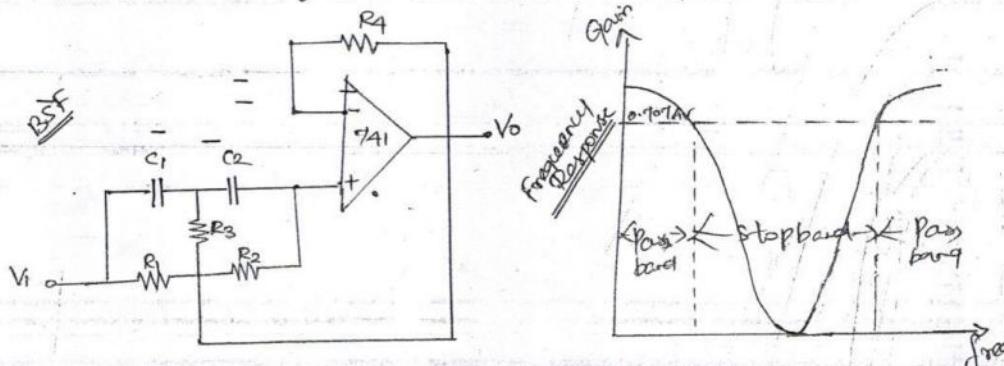
$$Q = \left[\frac{R_1 R_2}{2 R_3} \right]^{1/2}$$

$$\text{Voltage gain } Av = \frac{Q}{2\pi R_1 f_r C}$$

45

(c) Band Rejection filter (or) Band elimination filter (or) Band Stop Filter:

" Function of BSF is opposite to BPF. It blocks or stops a certain band of signal frequencies, and allows the frequency outside of this band without any attenuation.



This filter is implemented by summing together the o/p's of the LPF & HPF.

In this ckt, a Twin-T network is connected series with the non-inverting input of the op-amp. This Twin-T offers very low frequency signals going out through the LPF constituted by $R_1 - R_2 - C_3$.

Very High frequency signals reaching the output through the HPF formed by $C_1 - C_2 - R_3$.

But the intermediate band frequencies are stopped by both filters.

Component values of Twin-T-network are chosen according to the following equations.

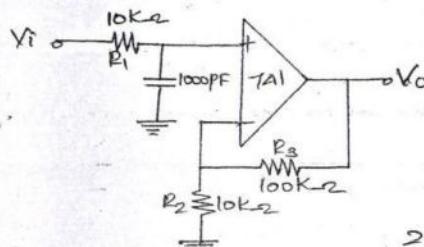
$$R_1 = R_2 = R, \quad R_3 = R/2$$

$$C_1 = C_2 = C, \quad C_3 = 2C$$

$$0 \leq R_4 \leq (R_1 + R_2)$$

$$f_R = \frac{1}{2\pi RC}$$

Prob1. Refer to the first order low pass filter. Determine the cutoff frequency and the gain value at 4 times the cutoff frequency.



Solution -

$$1. \text{ Cutoff freq } f_c = \frac{1}{2\pi R_2 C} \\ = \frac{1}{2\pi \times 10 \times 10^3 \times 1000 \times 10^{-12}} \\ = 15.915 \text{ kHz}$$

$$2. \text{ Gain } Av = 1 + R_3 / R_2 \\ = 1 + \frac{100 \times 10^3}{10 \times 10^3} = 11$$

$$Av \text{ in dB} = 20 \log_{10} 11 = 20.82 \text{ dB}$$

$$3. \text{ Gain at cutoff Point} = 20.82 - 3 \\ = 17.82 \text{ dB}$$

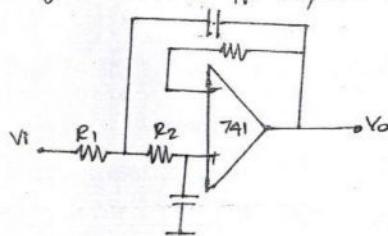
4. Gain at frequency 4 times the cutoff frequency will be 12dB below the value of mid-band gain

$$\therefore \text{Gain at 4 times the cutoff freq} = 20.82 - 12 \\ = 8.82 \text{ dB}$$

Prob2 Diagram shows a 2nd order LPF built around a single op-amp. calculate the values of R₁, R₂, C₁ & C₂ and R₃.

If the filter had a cutoff freq of 10kHz, Q-factor

b 0.707 & input impedance not less than 10kΩ.



Solution:

$$\rightarrow \text{For } R_1 = R_2 = R$$

$$\text{Cut-off freq } f_c = \frac{1}{2\pi R \sqrt{C_1 C_2}}$$

$$\rightarrow Q = \frac{1}{2} \sqrt{\frac{C_1}{C_2}}$$

$$\text{For } Q = 0.707, C_1 = 2C_2$$

\rightarrow for input impedance of 10kΩ, R₁ = 10kΩ = R₂

$$\rightarrow f_c = \frac{1}{2\pi \times 10 \times 10^3 \times C_2} = \sqrt{2}$$

$$= 10 \times 10^3$$



47

This gives $C_2 = 0.001\text{uF}$

$$\rightarrow C_1 = 2C_2 = 0.0022\text{uF}$$

$\rightarrow R_3$ is equal to R_1+R_2 in order to have "dc resistance between each op-amp input and ground.

$$\therefore R_3 = 20\text{k}\Omega$$

Prob Design an opamp based Twin T band reject filter having a notch frequency of 100kHz . Specify the small signal bandwidth of the chosen op-amp if the highest expected freq were 1MHz .

Soln: -

$$\rightarrow \text{The notch frequency } f_N = \frac{1}{2\pi R C} = 100\text{kHz}$$

$$\text{Where } R_1 = R_2 = R, \quad C_1 = C_2 = C, \quad R_3 = R/2, \quad C_3 = 2C$$

$$\rightarrow \text{Let } C = 0.0001\text{uF}$$

$$\text{This gives } R = \frac{1}{2\pi \times 100 \times 10^3 \times 0.0001 \times 10^{-6}} = 15.92\text{k}\Omega$$

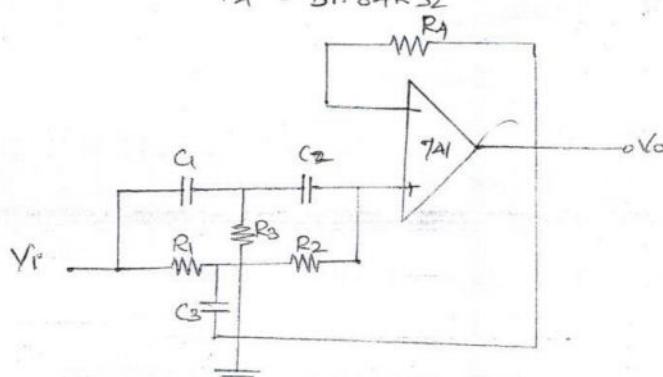
$$= 15.92\text{k}\Omega$$

$$\rightarrow \text{This gives } C_1 = C_2 = 0.0001\text{uF} \quad \& \quad C_3 = 0.0002\text{uF}$$

$$\rightarrow R_1 = R_2 = 15.92\text{k}\Omega \quad \& \quad R_3 = \frac{15.92 \times 10^3}{2} = 7.96\text{k}\Omega$$

$$\rightarrow R_A = R_1 + R_2 = 15.92 \times 10^3 + 15.92 \times 10^3$$

$$R_A = 31.84\text{k}\Omega$$



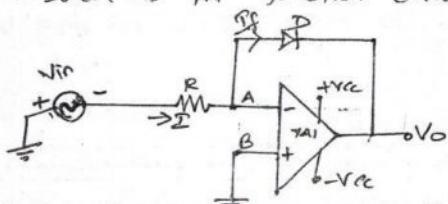


NON LINEAR AMPLIFIER:

AS

A non-linear amplifier is a circuit which gives non linear relationship between its input and output signals. The output signal strength do not vary in direct proportion to the input signal strength.

The Non-linear amplification can be achieved in a simple way by connecting a non-linear device such as PNP Junction diode in the feedback path.



Operation:

→ When the input voltage V_i is small than the cut-off voltage V_0 of diode, the diode behaves as open circuit. Resulting in large gain due to open loop operation of op-amp.

⇒ When the input voltage is large, the diode offers very small resistance & thus gain is low. Such a circuit cause output voltage to change in the ratio of 2:1 for an input change of 1000:1

By virtual ground concept as node B is grounded, node A will be virtually grounded.

$$\therefore V_A = 0$$

$$\text{we have } I = \frac{V_i - V_A}{R}$$

$$\text{Since } V_A = 0$$

$$I = \frac{V_i}{R}$$

Let I_f be the diode current, & voltage across diode is $V_A - V_o$. Since $V_A = 0$ then voltage across diode is $-V_o$.

Considering diode equation, we get

$$-V_o = V_T \ln \left(\frac{I_f}{I_s} \right)$$

Where V_T = voltage equivalent of temperature

I_f = Diode forward current

I_s = Diode reverse saturation current



49

Since current through opamp is negligible, we get

$$I = I_f$$

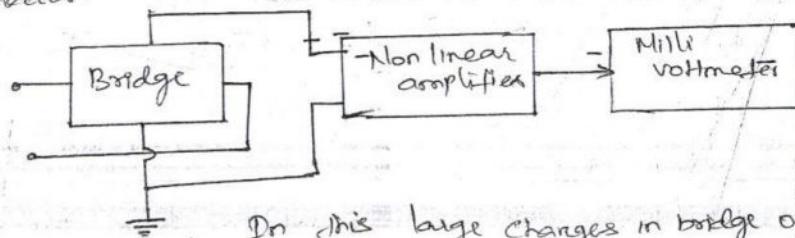
$$\therefore I_f = I = V_{in}/R$$

$$V_o = \eta V_T \ln \left[\frac{V_{in}}{V_{ref}} \right]$$

Since $\eta V_T R$ is constant, it can be denoted as V_{ref}

$$V_o = \eta V_T \ln \left[\frac{V_{in}}{V_{ref}} \right]$$

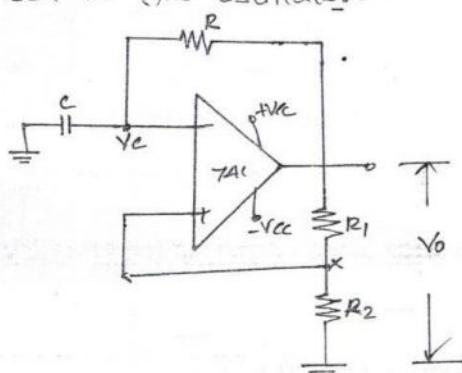
Application of non-linear amplifier is AC Bridge balance detector.



In this large changes in bridge output voltage get converted to small changes and millivoltmeter can show the variation in the voltage at the input.

RELAXATION OSCILLATOR :

Relaxation oscillator using op-amp is a free-running oscillator producing a square wave whose period depends on the charging & discharging time of the capacitor used in the oscillator.



Assume that the output

$$V_0 = +V_{sat}$$

Due to the positive feedback the voltage at point X is given by

$$V_x = \frac{R_2}{R_1+R_2} V_0$$

$$= \frac{R_2}{R_1+R_2} V_{sat}$$

$$\text{Let } \frac{R_2}{R_1+R_2} = \beta$$

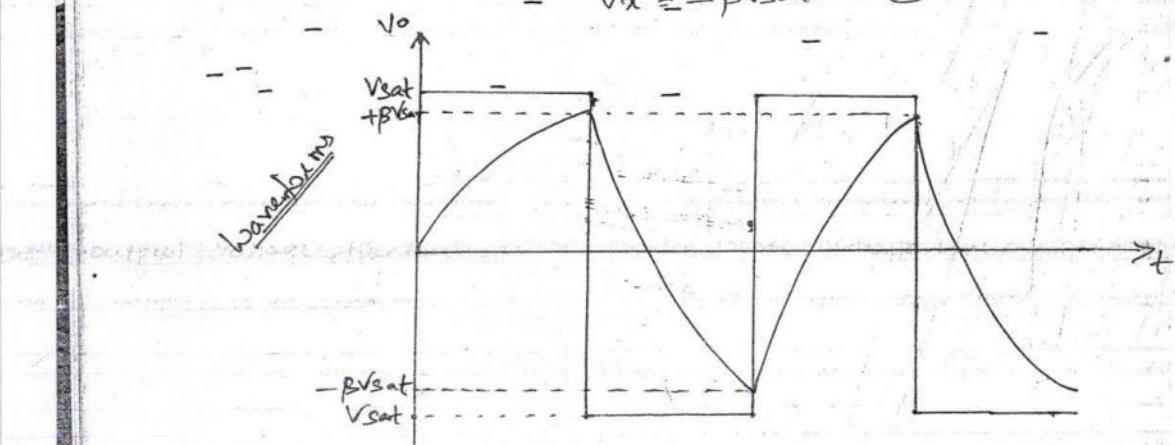
$$\therefore V_x = \beta V_{sat} \quad \text{--- (1)}$$

50

Let us assume the capacitor C is initially uncharged. Then the capacitor C starts charging through R with time constant RC . When the magnitude of the voltage V_C across the valve BV_{sat} due to comparator action, the output V_O immediately changes from $+V_{sat}$ to $-V_{sat}$.

- Note $V_O = -V_{sat}$

$$- V_x = -BV_{sat} \quad \text{--- (2)}$$



The capacitor has a positive value of V_C now discharges to zero and starts charging in the reverse direction towards ground, so that V_C becomes $-V_C$. The charging time constant is RC .

When the capacitor voltage V_C goes below $-BV_{sat}$, the output voltage V_O changes back to $+V_{sat}$ due to opamp comparator action. It produces a square wave between $+V_{sat}$ and $-V_{sat}$.

⇒ Expression for time period T :

The voltage across the capacitor at any instant of time is given by

$$V_C = V_f + (V_i - V_f) e^{-t/RC}$$

where V_i initial = Initial value of capacitor voltage = BV_{sat} at $t=0$

V_f final = final value of capacitor voltage = V_{sat} at $t=\infty$



51

$\tau = \text{time constant } RC$

$$\text{Now } V_C = V_{sat} + (-\beta V_{sat} - V_{sat}) e^{-t/\tau}$$

$$= V_{sat} - V_{sat} (1+\beta) e^{-t/\tau}$$

at $t = T/2$, the capacitor voltage $V_C = \beta V_{sat}$

now V_C becomes

$$\beta V_{sat} = V_{sat} - V_{sat} (1+\beta) e^{-T/2\tau}$$

$$-V_{sat} (1+\beta) e^{-T/2\tau} = \beta V_{sat} - V_{sat}$$

$$= -V_{sat} (1-\beta)$$

$$(1+\beta) e^{-T/2\tau} = -\frac{V_{sat} (1-\beta)}{-V_{sat}}$$

$$e^{-T/2\tau} = \frac{1-\beta}{1+\beta}$$

$$-T/2\tau = \ln \left(\frac{1-\beta}{1+\beta} \right)$$

$$T/2\tau = -\ln \left(\frac{1+\beta}{1-\beta} \right)$$

$$\text{where } \beta = \frac{R_2}{R_1+R_2}$$

$$\frac{1+\beta}{1-\beta} = \frac{1 + \frac{R_2}{R_1+R_2}}{1 - \frac{R_2}{R_1+R_2}} = \frac{\frac{R_1+R_2+R_2}{R_1+R_2}}{\frac{R_1+R_2-R_2}{R_1+R_2}}$$

$$= \frac{R_1+R_2+R_2}{R_1+R_2-R_2} = \frac{R_1+2R_2}{R_1}$$

$$= \frac{R_1}{R_1} + \frac{2R_2}{R_1}$$

$$\frac{1+\beta}{1-\beta} = 1 + \frac{2R_2}{R_1}$$

$$\therefore T = 2\tau \ln \left(1 + \frac{2R_2}{R_1} \right)$$



54

The filter circuit is used after the rectifier to reduce the ripple content in the pulsating dc and makes it smoother. Still the filter output contains some ripples. This voltage is called unregulated dc voltage.

- After the filter, a regulator block is used to remove all the ripples - ~~so that~~ makes output voltage smooth.
- It keeps the output voltage constant irrespective of changes in input dc voltage also keeps the output voltage constant under variable load conditions.

PARAMETERS OF REGULATED POWER SUPPLY:

1) Load Regulation:

Load regulation is defined as change in regulated output voltage of the power supply as the load current varies from 0 (no load condition) to maximum rated value (full load condition).

$$\text{Percentage load regulation} = \left(\frac{V_{NL} - V_{FL}}{V_{FL}} \right) \times 100$$

2) Line regulation: (source regulation)

Line regulation is defined as variation of regulated output voltage for a specified change in line voltage. Ideally the source regulation should be zero and practically it should be as low as possible.

If the output voltage of 10v varies by $\pm 1\%$ for a specified variation in line voltage, then the line regulation

$$\text{is } \frac{0.2}{10} \times 100 = 2\%$$

3) Voltage Stability factor (SV):

It shows the dependency of output voltage on the input line voltage.

It is defined as the percentage change in the output voltage which occurs per volt change in input voltage, where load current and temperature are assumed to be constant.

4) Temperature Stability factor (ST):

Temperature stability of the power supply will be determined by temperature coefficients of various temperature sensitive semiconductor devices.

So it's better to choose the low temperature coefficient devices to keep output voltage constant and independent of temperature.

Zener diodes are having breakdown voltages between 5V to 8V having very low temperature coefficients and hence these are preferred in the power supply circuit.

5) Ripple Rejection (RR):

Ripple Rejection Ratio is defined as the ratio of ripple in the regulated output voltage to the ripple present in unregulated input voltage.

$$\text{Ripple Rejection Factor} = \frac{V_{\text{Ripple}}(\text{Output})}{V_{\text{Ripple}}(\text{Input})}$$

When expressed in decibels

$$\text{RRF in dB} = 20 \log \left[\frac{V_{\text{Ripple}}(\text{Output})}{V_{\text{Ripple}}(\text{Input})} \right] \text{dB}$$

ADJUSTABLE VOLTAGE REGULATED:

An adjustable voltage regulator is a kind of regulator, whose regulated output voltage can be varied over a range. There are 2 types.



58

- The discrete signal from sample and hold circuit is fed to analog to digital (ADC) converter.

The ADC gives digital output signal that can be easily processed, stored and transmitted by digital systems or computer system.

- The digital signal is converted back to analog by digital to analog converter (DAC).

- The output of the DAC is usually a staircase wave form which is passed through smoothing filter to reduce the quantization noise.

Applications :

Digital signal processing

Digital Audio mixing

Music and video synthesis

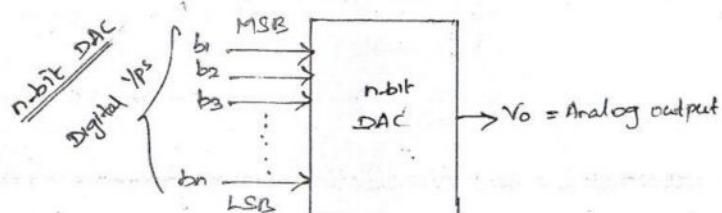
Data acquisition

pulse code modulation

Microprocessor based instrumentation

DIGITAL TO ANALOG CONVERTERS :

The DAC converts digital or binary data into its equivalent analog value. The DAC accepts 'n' bit input words $b_1, b_2, b_3 \dots b_n$ in binary and produces equivalent analog signal proportional to it.



The bit b_1 is called most significant bit (MSB) and b_n is called as least significant bit (LSB).

If $n=1$, indicates it is 1 bit DAC. Each digital input requires an electrical signal representing either a logic 1 or a logic 0.

59.

The DAC output can either be a voltage or current signal.
For a voltage output DAC, the conversion characteristics
can be expressed by

$$V_o = kV_{FS} (b_1 \cdot 2^1 + b_2 \cdot 2^2 + b_3 \cdot 2^3 + \dots + b_n \cdot 2^n)$$

Where V_o = Output voltage

V_{FS} = full scale output voltage

k = scaling factor usually adjusted to unity.

$b_1 \dots b_n$ = n-bit binary - fractional word with
decimal point located at the left.

b_1 = MSB with a weight = $\frac{V_{FS}}{2^1}$

b_n = LSB with weight = $\frac{V_{FS}}{2^n}$

⇒ Performance Parameters of DAC:

1. Resolution:

Resolution is the number of various analog output values
that is provided by a DAC.

∴ for n-bit DAC Resolution = 2^n

Resolution can also be defined as the ratio of change in
output voltage resulting from a change of LSB at the
digital inputs.

$$\text{For n-bit DAC, resolution is } = \frac{V_{OFS}}{2^{n-1}}$$

where V_{OFS} = full scale output voltage if $n=8$, and
 $V_{OFS} = 10\text{mV}$

$$\begin{aligned} \text{Resolution} &= \frac{V_{OFS}}{2^{n-1}} = \frac{10.1}{2^8-1} \\ &= \frac{10.1}{255} = 10.18\text{mV/LSB} \end{aligned}$$

An input of 1 LSB cause the output to change by 10.18mV.
We can obtain input-output relation for DAC is

$$\boxed{V_o = \text{Resolution} \times b}$$

↳ decimal values of digital input

2. Accuracy :

Comparison of actual output with expected is called as accuracy.

If $V_{FS} = 10.0$ for 8-bit DAC

$$\text{Accuracy} = \frac{V_{FS}}{(2^n-1) \cdot 2} = \frac{10}{256 \times 2} = 19.5 \text{ mV}$$

3 Setting time :

It is time required for a DAC output to settle within $\pm 1/2 \text{ LSB}$ of final value for a given digital input.

4 Stability :

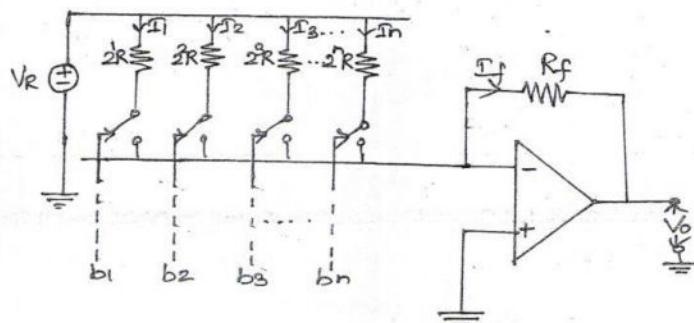
Stability \rightarrow performance of converter

Stability changes with parameters such as temperature, power-supply variations and also due to ageing of the components. Also some relevant parameters such as offset, gain, linearity error variation.

DAC TECHNIQUES :

- 1. Binary weighted resistor DAC
- 2. R-2R ladder DAC

1. Binary weighted Resistor DAC :



Here op-amp is used to sum n-binary weighted currents derived from a reference voltage VR via current scaling resistors.



61

This DAC circuit uses n-electronic switches controlled by the binary inputs $b_1, b_2 \dots b_n$.

If the binary input is high (logic 1), then switch connects the resistance to reference voltage V_R .

When digital input bit is low, it disconnects the resistor from V_R and no current flows through corresponding circuit.

$$\text{for ON Switch current } I = \frac{V_R}{R} \quad - \quad - \quad -$$

$$\text{for OFF Switch current } I = 0 \quad - \quad - \quad -$$

Due to high input impedance of opamp, flowing current will flow through R_f .

∴ The total current through R_f is written as

$$I_f = I_1 + I_2 + I_3 + \dots + I_n$$

$$= \frac{V_R}{2^1 R} b_1 + \frac{V_R}{2^2 R} b_2 + \frac{V_R}{2^3 R} b_3 + \dots + \frac{V_R}{2^n R} b_n$$

$$= \frac{V_R}{R} [b_1 2^1 + b_2 2^2 + b_3 2^3 + \dots + b_n 2^n]$$

The output voltage across R_f is

$$V_o = -I_f R_f \quad \text{---} \quad \textcircled{1}$$

Sub. If in \textcircled{1}

$$V_o = -\frac{V_R}{R} R_f [b_1 2^1 + b_2 2^2 + b_3 2^3 + \dots + b_n 2^n]$$

$$I_f R_f = R$$

$$V_o = -V_R [b_1 2^1 + b_2 2^2 + b_3 2^3 + \dots + b_n 2^n] \quad \boxed{\text{---}}$$

Drawbacks :

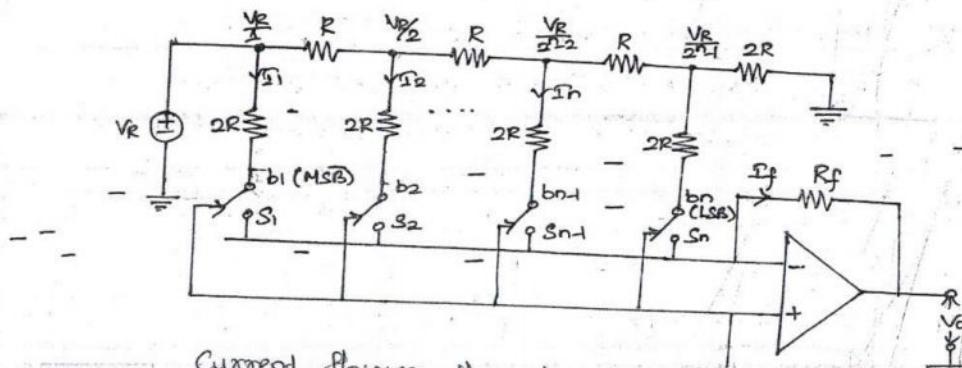
→ Large range of resistor values are required. Example for 8 bit DAC, we require $2^1 R, 2^2 R \dots 2^8 R$. ∴ the largest resistor is 256 times the smallest one.

→ It is impractical to fabricate large values of resistor on integrated circuit (IC).

2) R-2R ladder type DAC:

62

In R-2R ladder network DAC, only two values R & $2R$ are used. Hence can be used in IC-based applications.



Current flowing through each of these $2R$ resistances

$$I_1 = \frac{VR}{2R}$$

$$I_2 = \frac{VR/2}{2R} = \frac{VR}{4R}$$

$$I_3 = \frac{VR/4}{2R} = \frac{VR}{8R}$$

$$\vdots I_n = \frac{VR/2^{n-1}}{2R}$$

But we know that

$$V_o = -I_f R_f$$

$$= -R_f (I_1 + I_2 + \dots + I_n)$$

$$= -R_f \left[\frac{VR}{2R} b_1 + \frac{VR}{4R} b_2 + \dots + \frac{VR}{2^n R} b_n \right]$$

$$= -\frac{VR}{R} R_f (b_1 2^1 + b_2 2^2 + \dots + b_n 2^n)$$

When $R_f = R$

$$V_o = -VR (b_1 2^1 + b_2 2^2 + \dots + b_n 2^n)$$

Advantages:

As it uses only 2 types of resistors, it's easy to fabricate.

Binary input length can be increased by adding more R-2R sections.

Node voltages remains constant with changing binary input in inverted R-2R DAC. This helps in avoiding slowdown effect by stray capacitance.



63

Prob1. The digital input for a 4-bit DAC is $D = 0111$. calculate its output voltage take $V_{OFS} = 15V$.

Solution:

$$\text{Resolution} = \frac{V_{OFS}}{2^n-1} = \frac{15}{2^4-1} = 1V/\text{LSB}$$

$$\therefore V_O = \text{Resolution} \times D$$

$$D = \text{Decimal values}(0111) = 7$$

$$V_O = \frac{1V}{\text{LSB}} \times 7$$

$$\boxed{V_O = 7V}$$

Prob2. A 8bit DAC having resolution of $22mV/\text{LSB}$. Calculate V_{OFS} and output if the input is $(00000000)_2$.

Solution:

$$\text{Resolution} = 22mV, \text{input} = (00000000)_2$$

$$\text{Resolution} = \frac{V_{OFS}}{2^n-1}$$

$$22mV = \frac{V_{OFS}}{2^8-1}$$

$$V_{OFS} = 15.6V$$

$$D = \text{equivalent of } (00000000)_2 = 128$$

$$V_O = 22 \times 10^{-3} \times 128$$

$$\boxed{V_O = 2.8V}$$

Prob3. Calculate output voltage produced by DAC, when output range is between 0 and 10V for input binary number.

- a) 10 (2 bit DAC) b) 0011

Solution:

a) Bits $\Rightarrow 10$

$$\therefore V_O = 10V (1 \times \frac{1}{2} + 0 \times \frac{1}{4}) = 5V$$

b) Bits $\Rightarrow 0011$

$$\therefore V_O = 10V (0 \times \frac{1}{2} + 0 \times \frac{1}{4} + 1 \times \frac{1}{8} + 1 \times \frac{1}{16}) = 1.875V$$



- Reobta calculate the values of the LSB and full scale output for a bit DAC for 0 to 10V range.

Solution :

$$\text{As done, } \text{LSB} = \frac{1}{2^4} = \frac{1}{16}$$

For 10V range

$$\text{LSB} = \frac{10\text{V}}{16} = 625\text{mV}$$

$$\text{and } \text{NSB} = (\frac{1}{2}) \text{ full scale}$$

$$= \frac{1}{2} \times 10$$

$$= 5\text{V}$$

$$\text{Full scale output} = \text{full scale voltage} - 1 \text{ LSB}$$

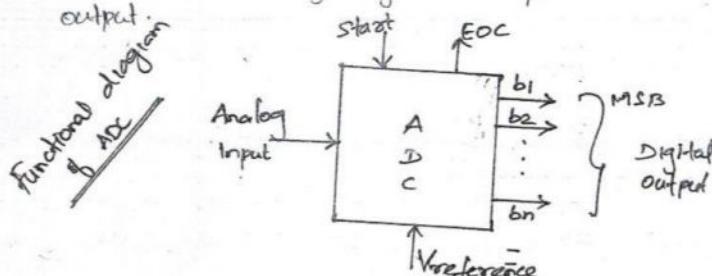
$$= 10 - 625\text{mV}$$

$$= 9.375\text{V}$$

A-D CONVERTERS :

Analog to digital converter is exactly opposite to DAC.

It takes an analog signal as input and converts into digital output.



ADC is provided with 2 control pins start and end of conversion. Here start input initiates the conversion and end of conversion (EOC) output indicates end of conversion.

Classification of ADCs :

These ADCs are classified into 2 groups based on conversion technique. They are

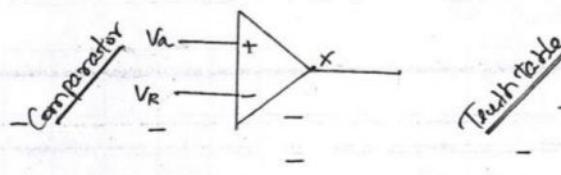
- 1) Direct type ADCs
- 2) Integrated type ADCs

⇒ ADC TECHNIQUES :

▷ Flash (comparators) type ADC:

This is also called parallel comparators A-D converter.

It is simple, fastest and most expensive conversion technique.

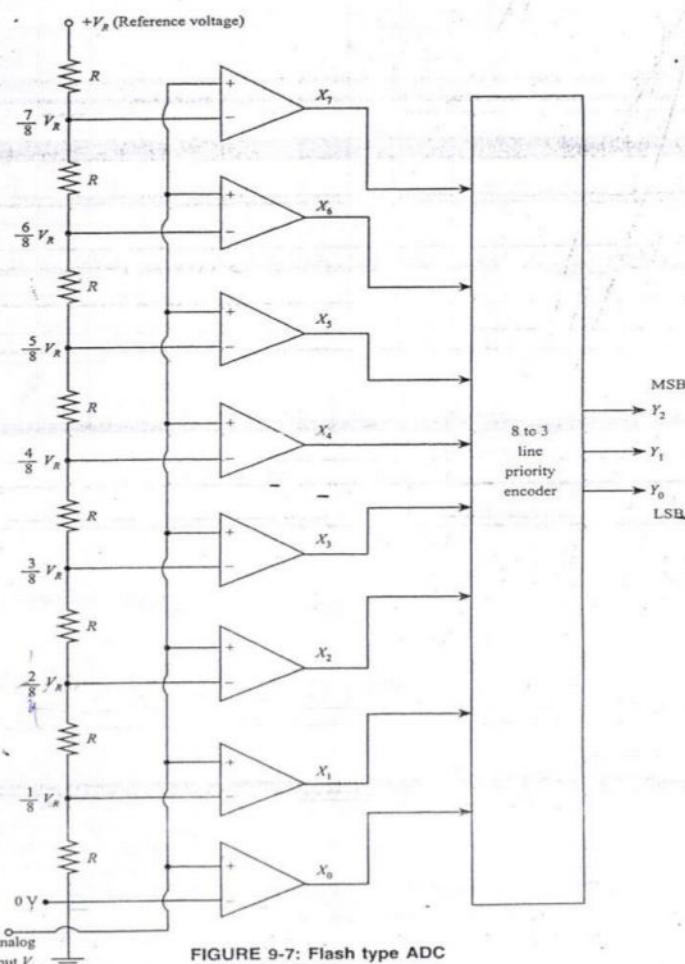


Input voltage Logic output

$V_a > V_R$ $X = 1$

$V_a < V_R$ $X = 0$

$V_a = V_R$ Previous value



66

The resistive network is set to equal reference voltages at each node. The comparator compares set reference value at inverting terminal of op-amp with analog output at non-inverting terminal.

Truth Table for flash ADC.

Input Voltage (V_a)	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
$0 \text{ to } \frac{V_R}{8}$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V_R}{8} \text{ to } \frac{V_R}{4}$	0	0	0	0	0	0	1	1	0	0	1
$\frac{V_R}{4} \text{ to } \frac{3V_R}{8}$	0	0	0	0	0	1	1	1	0	1	0
$\frac{3V_R}{8} \text{ to } \frac{5V_R}{8}$	0	0	0	0	1	1	1	1	0	1	1
$\frac{5V_R}{8} \text{ to } \frac{15V_R}{8}$	0	0	0	1	1	1	1	1	1	0	0
$\frac{15V_R}{8} \text{ to } \frac{3V_R}{4}$	0	0	1	1	1	1	1	1	1	0	1
$\frac{3V_R}{4} \text{ to } \frac{7V_R}{8}$	0	1	1	1	1	1	1	1	1	1	0
$\frac{7V_R}{8} \text{ to } V_R$	1	1	1	1	1	1	1	1	1	1	1

Advantages:

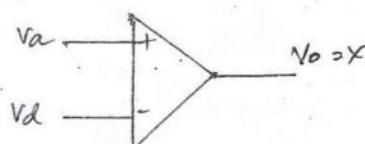
High speed

Disadvantages:

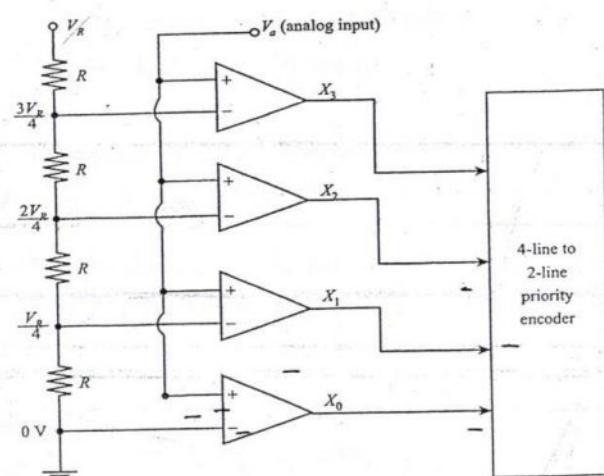
No. of comparators required almost doubles for each added bit

For ex: for 2-bit ADC, No. of comparator $2^n = 2^2 = 4$
3-bit " " " " " $2^3 = 8$

⇒ Design of a 2-bit flash ADC :



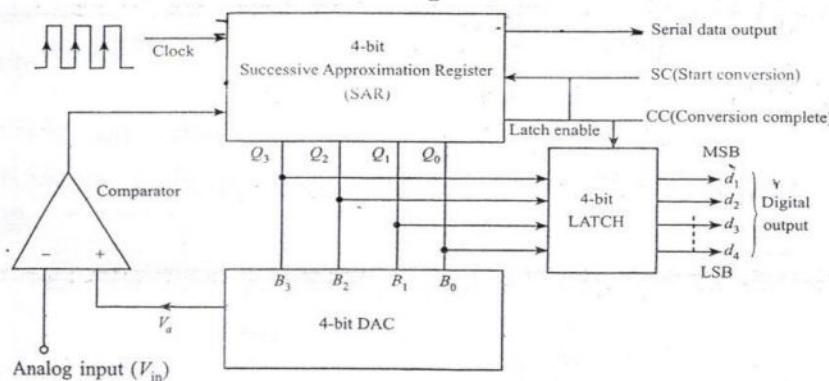
Input voltage	Logic output
$V_a > V_d$	1
$V_a < V_d$	0
$V_a = V_d$	Previous value



Truth Table

Analog input voltage (V_a)	X_3	X_2	X_1	X_0	Y_1	Y_0
0 to $V_a/4$	0	0	0	1	0	0
$V_a/4$ to $2V_a/4$	0	0	1	1	0	1
$2V_a/4$ to $3V_a/4$	0	1	1	1	1	0
$3V_a/4$ to V_a	1	1	1	1	1	1

2) Successive Approximation type ADC :



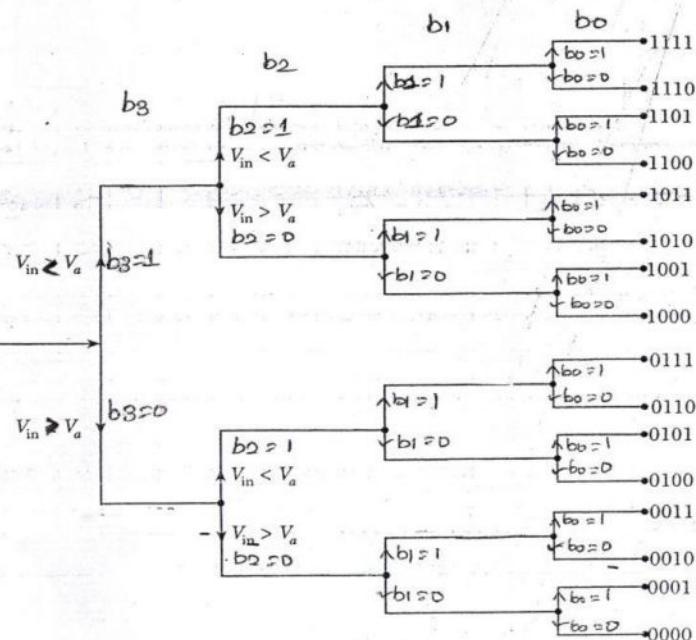
68

It consists of a successive approximation register (SAR), the output of which is connected to DAC as well as output latch circuit.

The input analog signal (V_{in}) is compared with the analog output signal (V_a) of the DAC. The output of comparator is feedback into SAR.

The control logic inside SAR adjusts its digital output until it is equal to the analog input signal V_a .

Operation:



At the start of conversion cycle, the start conversion terminals is made high. On the first clock pulse, the output of SAR is made 1000.

The DAC produces an analog signal V_a proportional to the digital input
 \rightarrow If $V_{in} > V_a$,

69

MODULE - 2
KARNAUGH MAPS

KARNAUGH MAP:

The Karnaugh map (K.M or K-map) is a pictorial method of simplifying Boolean algebra expressions, without using Boolean algebra theorems and equation manipulation.

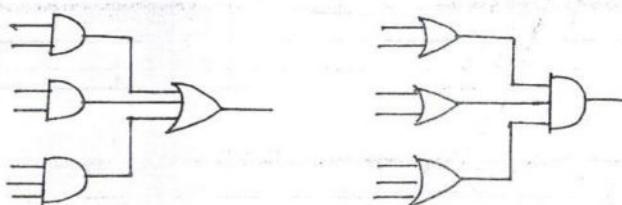
- Maurice Karnaugh introduced it in 1953.

MINIMUM FORMS OF SWITCHING FUNCTIONS:

When a function is realized using AND and OR gates, the cost of realizing the function is directly related to the number of gates and gate inputs used. The K-map techniques lead directly to minimum cost 2-level circuits composed of AND and OR gates.

There are 2 methods to minimize the expression.

1. Sum of Products
2. Product of Sums



Q1: Find a minimum SOP expression for

$$F(a, b, c) = \Sigma m(0, 1, 2, 5, 6, 7) =$$

Solution :

$$\begin{aligned} F &= \bar{a}\bar{b}\bar{c} + \bar{a}\bar{b}c + \bar{a}b\bar{c} + ab\bar{c} + a\bar{b}c + abc \\ &= \bar{a}B(\bar{c}+c) + b\bar{c}(\bar{a}+a) + ac(\bar{b}+b) \\ &= \bar{a}B + b\bar{c} + ac \end{aligned} \quad [\bar{a}+\bar{a}=1]$$

Q2: Find a minimum POS expression for

$$(A+\bar{B}+C+\bar{D})(A+\bar{B}+\bar{C}+\bar{D})(A+\bar{B}+\bar{C}+D)(\bar{A}+\bar{B}+\bar{C}+D)$$

Solution

$$\begin{aligned} &(A+\bar{B}+\bar{C}+D)(\bar{A}+\bar{B}+\bar{C}+D) \\ Y &= (A+\bar{B}+\bar{D})(\bar{B}+\bar{C}+D)(A+\bar{A}) = (B+\bar{C}+D)(A+\bar{A}) \\ &= (A+\bar{B}+\bar{D})(\bar{B}+\bar{C}+D) \\ &= (A+\bar{B}+\bar{D})(\bar{C}+D)(\bar{B}+\bar{B}) \\ &= (A+\bar{B}+\bar{D})(\bar{C}+D) \end{aligned}$$



K-maps:

1) One variable map

\bar{A}	0
A	1

2) Two variable map

\bar{A}	B	B
\bar{A}	$\bar{A}\bar{B}$	$\bar{A}B$
A	$A\bar{B}$	AB
A	$A\bar{B}$	AB

3) Three variable map

\bar{A}	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	ABC	$A\bar{B}C$	$A\bar{B}\bar{C}$	$A\bar{B}C$
A	$\bar{A}BC$	$\bar{A}\bar{B}C$	$\bar{A}\bar{B}\bar{C}$	$\bar{A}B\bar{C}$
A	$\bar{A}BC$	$\bar{A}\bar{B}C$	$\bar{A}\bar{B}\bar{C}$	$\bar{A}B\bar{C}$

4) Four variable map

$\bar{A}\bar{B}\bar{C}\bar{D}$	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
$\bar{A}\bar{B}$	ABCD	$A\bar{B}CD$	$\bar{A}\bar{B}CD$	$\bar{A}\bar{B}C\bar{D}$
$\bar{A}B$	$\bar{A}BCD$	$A\bar{B}CD$	$A\bar{B}C\bar{D}$	$\bar{A}B\bar{C}D$
AB	$\bar{A}BCD$	$A\bar{B}CD$	$A\bar{B}C\bar{D}$	$ABC\bar{D}$
$A\bar{B}$	$\bar{A}BCD$	$A\bar{B}CD$	$A\bar{B}C\bar{D}$	$A\bar{B}CD$

⇒ Convert Truth Table to Karnaugh map

A B C	Y
0 0 0	0
0 0 1	0
0 1 0	1
0 1 1	0
1 0 0	0
1 0 1	0
1 1 0	1
1 1 1	1



K-map

0	0	0	1
0	0	1	1

A B C D	Y
0 0 0 0	0
0 0 0 1	1
0 0 1 0	0
0 0 1 1	0
0 1 0 0	0
0 1 0 1	0
0 1 1 0	1
0 1 1 1	1
1 0 0 0	0
1 0 0 1	0
1 0 1 0	0
1 0 1 1	0
1 1 0 0	0
1 1 0 1	0
1 1 1 0	1
1 1 1 1	0



K-map

0	1	0	0
0	0	1	1
0	0	0	1
0	0	0	0



→ Convert Boolean expression to K-map

71

$$i) Y = ABC + ABC + A\bar{B}C$$

$$ii) Y = \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} +$$

↓

K-map

	$\bar{B}\bar{C}$	$\bar{B}C$	$B\bar{C}$	BC
\bar{A}	0 1	0 0	0 0	0 0
A	0 0	1 0	1 1	1 1

	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
$\bar{A}\bar{B}$	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
$\bar{A}B$	1 0 0 1	0 1 0 0	0 0 1 0	0 0 1 1
$A\bar{B}$	0 1 0 0	0 0 1 0	0 0 1 1	0 0 1 1
AB	0 0 1 1	0 0 1 1	0 0 1 1	0 0 1 1

Pairs, quads and octets:

⇒ Pair:

Pair is a group of two 1's that are horizontally or vertically adjacent.

	$\bar{B}\bar{C}$	$\bar{B}C$	$B\bar{C}$	BC
$\bar{A}\bar{B}$	0 0	0 1	1 0	1 1
$\bar{A}B$	0 0	0 0	0 0	0 0
$A\bar{B}$	0 0	0 0	0 0	0 0
AB	0 0	0 0	0 0	0 0

$$Y = \bar{A}\bar{B}C + \bar{A}B\bar{C}$$

$$= \bar{A}C(\bar{B}+\bar{B})$$

$$\boxed{Y = \bar{A}C}$$

	$\bar{B}\bar{C}$	$\bar{B}C$	$B\bar{C}$	BC
\bar{A}	0 0 1 0	0 1 0 0	1 0 0 0	1 0 0 0
A	0 0 0 0	0 0 1 0	0 0 1 0	0 0 1 0

$$Y = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}B\bar{C} + \bar{A}B\bar{C}$$

$$= \bar{A}C(\bar{B}+\bar{B}) + BC(\bar{A}+\bar{A})$$

$$\boxed{Y = AC + BC}$$

	$\bar{B}\bar{C}$	$\bar{B}C$	$B\bar{C}$	BC
\bar{A}	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
A	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

$$Y = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$$

$$= BC(\bar{A}+\bar{A})$$

$$\boxed{Y = BC}$$

	$\bar{B}\bar{C}$	$\bar{B}C$	$B\bar{C}$	BC
\bar{A}	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
A	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

$$Y = A\bar{B}\bar{C} + A\bar{B}C$$

$$= AC(\bar{B}+\bar{B})$$

$$\boxed{Y = AC}$$

	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
$\bar{A}\bar{B}$	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
$\bar{A}B$	0 1 0 0	0 0 1 0	0 0 0 0	0 0 0 0
$A\bar{B}$	0 0 1 0	0 0 0 0	0 0 0 0	0 0 0 0
AB	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} +$$

$$AB\bar{C}\bar{D} + A\bar{B}CD$$

$$= \bar{A}BD(C+\bar{C}) + A\bar{C}D(B+\bar{B})$$

$$\boxed{Y = ABD + A\bar{C}D}$$

⇒ Quad:

Quad is a group of four 1's that are horizontally or vertically adjacent.

	$\bar{B}\bar{C}$	$\bar{B}C$	$B\bar{C}$	BC
\bar{A}	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
A	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} +$$

$$= \bar{A}B(C+\bar{C}) + A\bar{B}(C+\bar{C})$$

$$= A\bar{B} + AB$$

$$= A(\bar{B}+B)$$

$$\boxed{Y = A}$$

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} +$$

$$= \bar{A}B(C+\bar{C}) + A\bar{B}(C+\bar{C})$$

$$= A\bar{B} + AB$$

$$= A(\bar{B}+B)$$

$$\boxed{Y = A}$$



	$\bar{C}D$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	0	1	0
$\bar{A}B$	0	0	1	0
$A\bar{B}$	0	0	1	0
AB	0	0	1	0

$$\begin{aligned}
 Y &= \bar{A}\bar{B}CD + \bar{A}B\bar{C}D + AB\bar{C}D + A\bar{B}CD \\
 &= \bar{A}CD + ACD \\
 \boxed{Y = CD}
 \end{aligned}$$

	$\bar{C}D$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	0	0	0
$\bar{A}B$	0	1	1	0
$A\bar{B}$	0	1	1	0
AB	0	0	0	0

$$\begin{aligned}
 Y &= A\bar{B}CD + \bar{A}B\bar{C}D + AB\bar{C}D + A\bar{B}CD \\
 &= ABD + A\bar{B}D \\
 \boxed{Y = BD}
 \end{aligned}$$

	$\bar{C}D$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	0	0	0
$\bar{A}B$	0	0	0	0
$A\bar{B}$	1	0	0	1
AB	1	0	0	1

$$\begin{aligned}
 Y &= A\bar{B}CD + \bar{A}B\bar{C}D + AB\bar{C}D + A\bar{B}CD \\
 &= AC\bar{D} + A\bar{C}\bar{D} \\
 \boxed{Y = AD}
 \end{aligned}$$

	$\bar{C}D$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	0	1
$\bar{A}B$	0	0	0	0
$A\bar{B}$	0	0	0	0
AB	1	0	0	1

$$\begin{aligned}
 Y &= A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + A\bar{B}\bar{C}D + A\bar{B}CD \\
 &= \bar{A}\bar{B}\bar{D} + A\bar{B}\bar{D} \\
 &= \bar{B}\bar{D}
 \end{aligned}$$

→ Octet:

i) Octet is a group of eight 1's.

	$\bar{B}L$	$\bar{B}L$	$B\bar{L}$	$B\bar{L}$
\bar{A}	1	1	1	1
A	1	1	1	1

$$\boxed{Y = 1}$$

	$\bar{C}D$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	1	1	1
$\bar{A}B$	0	0	0	0
$A\bar{B}$	0	0	0	0
AB	1	1	1	1

$$\begin{aligned}
 Y &= A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + A\bar{B}CD + \\
 &\quad \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD + A\bar{B}\bar{C}D
 \end{aligned}$$

$$\boxed{Y = \bar{B}}$$



ii)

1	0	0	1
1	0	0	1
1	0	0	1
1	0	0	1

$$Y = \overline{D}$$

iv)

0	0	0	0
1	1	1	1
1	1	1	1
0	0	0	0

$$Y = B$$

73

⇒ Simplify the following k-maps:

	$\bar{C}D$	$\bar{C}D$	CD	CD
$\bar{A}\bar{B}$	0	1	1	1
$\bar{A}B$	0	0	0	1
$A\bar{B}$	1	1	0	1
AB	1	1	0	1

$$Y = Y_1 + Y_2 + Y_3$$

$$\begin{aligned} &= \bar{A}\bar{B}2D + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + AB\bar{C}D + \\ &\quad A\bar{B}CD + AB\bar{C}\bar{D} + AB\bar{C}D + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D \end{aligned}$$

$$Y = \bar{A}\bar{B}D + \bar{A}CB + AC\bar{D} + ABC + A\bar{B}\bar{C}$$

$$\boxed{Y = \bar{A}\bar{B}D + CB + AC}$$

	$\bar{C}D$	$\bar{C}D$	CD	CD
$\bar{A}\bar{B}$	0	0	0	0
$\bar{A}B$	0	1	0	0
$A\bar{B}$	1	1	1	1
AB	1	1	1	1

$$Y = \bar{A}\bar{B}CD + A\bar{B}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D + A\bar{B}CD + A\bar{B}C\bar{D} +$$

$$A\bar{B}C\bar{D} + A\bar{B}CD + A\bar{B}C\bar{D} + A\bar{B}C\bar{D}$$

$$= B\bar{C}D + A\bar{B}C + ABC + A\bar{B}\bar{C} + A\bar{B}C$$

$$= B\bar{C}D + AB + A\bar{B}$$

$$\boxed{Y = B\bar{C}D + A}$$

	$\bar{C}D$	$\bar{C}D$	CD	CD
$\bar{A}\bar{B}$	1	1	0	0
$\bar{A}B$	1	1	0	1
$A\bar{B}$	1	1	0	1
AB	1	1	0	1

$$Y = \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D}$$

$$\boxed{Y = \bar{C} + B\bar{D}}$$

	$\bar{C}D$	$\bar{C}D$	CD	CD
$\bar{A}\bar{B}$	1	1	0	1
$\bar{A}B$	1	1	0	1
$A\bar{B}$	1	1	0	1
AB	1	1	0	1

$$Y = Y_1 + Y_2 + Y_3$$

$$\begin{aligned} &= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} \end{aligned}$$

$$\begin{aligned} &= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + ABC + A\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}\bar{C} \\ &\quad + A\bar{B}\bar{C} + A\bar{B}\bar{C} \end{aligned}$$

$$+ A\bar{B}\bar{C} + A\bar{B}\bar{C}$$

$$+ A\bar{B}\bar{C} + A\bar{B}\bar{C}$$

$$\boxed{Y = \bar{C} + B\bar{D} + A\bar{D}}$$

	$\bar{C}D$	$\bar{C}D$	CD	CD
$\bar{A}\bar{B}$	1	1	1	1
$\bar{A}B$	0	1	0	0
$A\bar{B}$	0	1	1	1
AB	1	1	1	1

$$\Rightarrow \boxed{Y = \bar{D} + \bar{A}B + ACD}$$

Eliminating Redundant groups:-

74

After the finishing of encircling groups, eliminate any redundant group. It is nothing but whose 1's are already used by other groups.

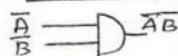
Example

0	0	(1)	0
1	1	0	0
0	1	0	1
0	1	0	0

All the ones of the quad are used by the planes. Because of this the quad is redundant.

0	0	(1)	0
1	1	0	0
0	1	1	1
0	1	0	0

Sum-of-Products method (SOP):



A	B	Fundamental Product
0	0	$\bar{A}\bar{B}$
0	1	$\bar{A}B$
1	0	$A\bar{B}$
1	1	AB

The outputs are called fundamental products. Fundamental products are also called minterms. Sum of Product is a group of product terms ORed together.

* Sum of Product equation

A	B	C	Y	minterm
0	0	0	0	m_0
0	0	1	0	m_1
0	1	0	0	m_2
0	1	1	1	m_3
1	0	0	0	m_4
1	0	1	1	m_5
1	1	0	1	m_6
1	1	1	1	m_7

To get sum of products solution,

- Identify all the fundamental products whose output is 1.
- Then OR the fundamental products.

$$Y = \bar{A}BC + A\bar{B}C + ABC + A\bar{B}\bar{C}$$

Alternate representation

$$Y = f(A, B, C) = \sum m(3, 5, 6, 7)$$

$\sum \rightarrow$ Summation

$f(A, B, C) \Rightarrow Y$ is a function of 3 Boolean variables A; B & C.

75

⇒ Product-of-Sums method:

With the SOP method, the fundamental product produces an output 1 for the corresponding input conditions are required for the simplification.

But with the Product-of-Sum (POS) method, the fundamental product produces an output 0 are required for the simplification. These fundamental products are also called Minterms.

A	B	C	Y	Minterm
0	0	0	$A+B+C = 0$	M ₀
0	0	1	$A+B+C = 1$	M ₁
0	1	0	$A+B+C = 1$	M ₂
0	1	1	$A+B+C = 0$	M ₃
1	0	0	$\bar{A}+\bar{B}+C = 1$	M ₄
1	0	1	$\bar{A}+\bar{B}+C = 1$	M ₅
1	1	0	$\bar{A}+\bar{B}+C = 0$	M ₆
1	1	1	$\bar{A}+\bar{B}+C = 1$	M ₇

Product of sum is a group of sums ANDed together.

To get POS solution

(i) Identify all the fundamental products whose output is 0.

(ii) Then AND the fundamental products

$$Y = (A+B+C) \cdot (\bar{A}+\bar{B}+C) \cdot (\bar{A}+\bar{B}+C)$$

Alternate representation

$$Y = F(A, B, C) = \overline{m}(0, 3, 6)$$

→ Symbolized Product (le) AND operation.

SOP Simplification

Ques 1. Minimize the expression using SOP method

$$Y = A\bar{B}C + \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + \bar{A}\bar{B}\bar{C}$$

Solution:

Step 1: Expression to K-map

1	1	1	0
1	1	0	0

Step 2: Grouping

	BC	$\bar{B}C$	$B\bar{C}$	$\bar{B}\bar{C}$	
G ₁	1	0	1	0	
G ₂	1	1	0	0	

$$\text{Step 3: } Y = G_1 + G_2$$

$$= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}\bar{B}C + A\bar{B}C + \bar{A}\bar{B}C + \bar{A}\bar{B}C$$

$$= \bar{A}\bar{B} + A\bar{B} + \bar{A}C$$

$$\boxed{Y = \bar{B} + \bar{A}C}$$



Q2. Reduce the following 4 variable function to its minimum SOP form using Kmap.

$$Y = \bar{A}\bar{B}C\bar{D} + A\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + A\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D}$$

Solution.

Step 1:

	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD	
$\bar{A}\bar{B}$	1	0	1	1	G_3
$\bar{A}B$	0	0	0	0	-
$A\bar{B}$	1	0	0	1	G_2
AB	1	0	1	1	-

Step 2:

$$Y = G_1 + G_2 + G_3$$

$$G_1 \Rightarrow Y_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} +$$

$$- \quad \bar{A}\bar{B}C\bar{D} + A\bar{B}C\bar{D}$$

$$= \bar{A}\bar{B}\bar{B}(C + \bar{C}) + \bar{A}\bar{B}\bar{D}(C + \bar{C})$$

$$= \bar{B}\bar{B}(C + \bar{A})$$

$$= \bar{B}\bar{D}$$

$$\begin{aligned} G_2 &= A\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D} + A\bar{B}(\bar{D} + A\bar{B}C\bar{D}) \\ &= A\bar{B}\bar{D} + A\bar{B}D \\ &= AB \end{aligned}$$

$$\begin{aligned} G_3 &= Y_3 = \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} \\ &= \bar{A}\bar{B}C + A\bar{B}C \\ &= BC \end{aligned}$$

$$\boxed{Y = \bar{B}\bar{D} + A\bar{D} + BC}$$

Q3 Reduce the foll function to its minimum SOP form using Kmap.

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D} + A\bar{B}C\bar{D}$$

$$\text{Ans: } \boxed{Y = \bar{A}\bar{C}\bar{D} + A\bar{B}C + ABC + ACD}$$

Q4 What is the simplified boolean equation for the foll logic equation expressed by minterms.

$$Y = f(A, B, C, D) = \sum m(7, 9, 10, 11, 12, 13, 14, 15)$$

Solution:

	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD	
$\bar{A}\bar{B}$	0	0	0	0	G_4
$\bar{A}B$	0	0	1	0	-
$A\bar{B}$	1	1	1	1	G_1
AB	1	1	1	1	G_3

G_2



$$\begin{aligned}
 Y &= Q_1 + Q_2 + Q_3 + Q_4 \\
 Q_1 = Y_1 &= AB\bar{C}D + A\bar{B}\bar{C}D + A\bar{B}CD + A\bar{B}C\bar{D} \\
 &= ABC + A\bar{B}C \\
 &= AB \\
 Q_2 = Y_2 &= AB\bar{C}D + A\bar{B}CD + A\bar{B}\bar{C}D + A\bar{B}C\bar{D} \\
 &= ABD + A\bar{B}D \\
 &= AD \\
 Q_3 = Y_3 &= ABCD + A\bar{B}C\bar{D} + A\bar{B}\bar{C}D + A\bar{B}C\bar{D} \\
 &= ABC + A\bar{B}C \\
 &= AC \\
 Q_4 = Y_4 &= A\bar{B}CD + A\bar{B}CD \\
 &= BCD
 \end{aligned}$$

77

$$Y = AB + AD + AC + BC$$

Q5 Simplify the logic function specified by the truth table using K-map. Y is output variable & A, B & C are input variables and implement using Gate.

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

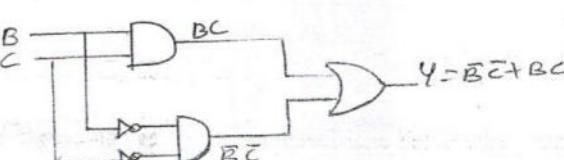
- Solution:

	$\bar{B}C$	$\bar{B}C$	BC	BC
\bar{A}	1	0	1	0
A	1	0	1	0

$$Y = \bar{A}\bar{B}C + A\bar{B}C + \bar{A}BC + ABC$$

$$Y = \bar{B}\bar{C} + BC$$

Logic Gate:





78

Q6 Reduce the foll function using K-map technique and implement using basic gates.

$$f(A, B, C, D) = \bar{A}\bar{B}D + A\bar{B}\bar{C}\bar{D} + \bar{A}BD + A\bar{B}CD$$

Solution:

Step 1:

$$f(A, B, C, D) = \bar{A}\bar{B}DC(\bar{C}) + A\bar{B}\bar{C}\bar{D} + \bar{A}BD(C\bar{C}) + A\bar{B}CD$$

$$= \bar{A}\bar{B}CD + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + \bar{A}BCD + \bar{A}B\bar{C}D + A\bar{B}C\bar{D}$$

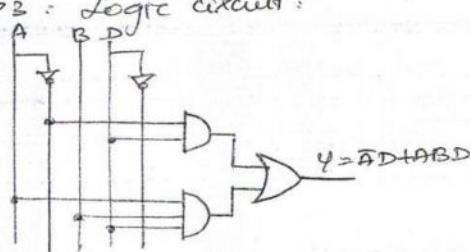
Step 2:

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	1	1	0
$\bar{A}B$	0	1	1	0
$A\bar{B}$	1	1	0	1
AB	0	0	0	0

$$\begin{aligned} Y &= \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + \\ &\quad \bar{A}B\bar{C}D + A\bar{B}\bar{C}\bar{D} + A\bar{B}CD \\ &= \bar{A}\bar{B}D + ABD + ABCD \end{aligned}$$

$$\boxed{Y = \bar{A}D + ABD}$$

Step 3: Logic circuit:



Q7 Reduce the foll function using K-map technique

$$f(\bar{A}, B, C, D) = \sum m(0, 1, 4, 8, 9, 10)$$

$$\text{Ans: } Y = \bar{A}\bar{C}\bar{D} + A\bar{B}\bar{D} + \bar{B}C$$

Don't care Conditions:

In some digital system, certain input conditions never occur during normal operations. Therefore, these corresponding output never appears. Since the output never appears, it is indicated by an X in the truth table.

The 'X' can be grouped along with the 1's. But the condition is, in a group the '1' should be new not X.

Q1 The Truth Table has high output for an input 0000, low output for 0001 to 1001 and don't care for 1010 to 1111. What is the simplest logic ckt with this truth table?

Solution:

Step 1 : Truth table

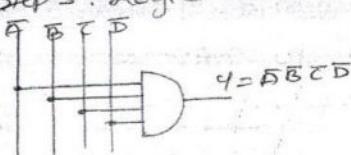
A B C D	Y
0 0 0 0	1
0 0 0 1	d
0 0 1 0	0
0 0 1 1	0
0 1 0 0	0
0 1 0 1	0
0 1 1 0	0
0 1 1 1	0
1 0 0 0	0
1 0 0 1	0
1 0 1 0	x
1 0 1 1	x
1 1 0 0	x
1 1 0 1	x
1 1 1 0	x
1 1 1 1	x

Step 2 : K map

	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
$\bar{A}\bar{B}$	1	0	0	0
$\bar{A}B$	0	0	0	0
$A\bar{B}$	x	x	x	x
AB	0	x	x	x

$$Y = \bar{A}B\bar{C}\bar{D}$$

Step 3 : Logic circuit



Q2 Give the simplest logic ckt for the following logic eqn where 'd' represents don't-care.

$$F(A,B,C,D) = \sum m(7) + d(10,11,12,13,14,15)$$

Solution:

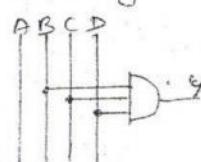
Step 1 : K-map

	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
$\bar{A}\bar{B}$	0	0	0	0
$\bar{A}B$	0	0	1	0
$A\bar{B}$	x	x	x	x
AB	0	0	x	x

Step 2 : Boolean eqn

$$Y = \bar{A}BCD + A\bar{B}CD$$

Step 3 : logic ckt



Q3 Find the reduced SOP form of the following function

$$f(A,B,C,D) = \sum m(1,3,7,11,15) + \sum d(0,2,4)$$



Solution:

	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD	
$\bar{A}\bar{B}$	X	1	1	X	Q_1
$\bar{A}B$	X	0	1	0	
$A\bar{B}$	0	0	1	0	
AB	0	0	1	0	Q_2

$$\begin{aligned}
 Y &= Q_1 + Q_2 \\
 Q_1 = Y_1 &= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD \\
 &= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C \\
 &= \bar{A}\bar{B} \\
 Q_2 = Y_2 &= \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD + A\bar{B}\bar{C}D + A\bar{B}CD \\
 &= \bar{A}CD + ACD \\
 &= \bar{C}D \\
 Y &= \bar{A}\bar{B} + \bar{C}D
 \end{aligned}$$

80

- Q4 Reduce using K-map

$$f(A, B, C, D) = \sum_m(5, 6, 7, 12, 13) + \sum_d(4, 9, 14, 15)$$

Solution:

0	0	0	0
X	1	1	1
1	1	X	X
0	X	0	0

Pair we can't make. Because
here X is now not 1.

$$Y = B$$

$$\text{Q5 } f(P, Q, R, S) = \sum_m(0, 1, 4, 8, 9, 10) + \sum_d(2, 11) \text{ Use K-map}$$

Solution:

	$\bar{P}\bar{S}$	$\bar{P}S$	PS	$P\bar{S}$
$\bar{P}\bar{Q}$	1	1	0	X
$\bar{P}Q$	1	0	0	0
$P\bar{Q}$	0	0	0	0
PQ	1	1	X	P

$$\begin{aligned}
 Q_1 &= \bar{P}\bar{Q}\bar{R}\bar{S} + \bar{P}\bar{Q}\bar{R}S + \bar{P}Q\bar{R}\bar{S} + P\bar{Q}\bar{R}S \\
 &= \bar{P}\bar{Q}R + P\bar{Q}R \\
 &= \bar{Q}R \\
 Q_2 &= \bar{P}\bar{Q}\bar{R}S + \bar{P}\bar{Q}R\bar{S} + P\bar{Q}\bar{R}S + P\bar{Q}R\bar{S} \\
 &= \bar{P}\bar{Q}S + P\bar{Q}S \\
 &= \bar{Q}S \\
 Q_3 &= \bar{P}\bar{Q}RS + P\bar{Q}RS \\
 &= PRS
 \end{aligned}$$

$$Y = \bar{Q}R + \bar{Q}S + PRS$$

$$\text{Q6 Simplify using K-map } f = w'xz + w'yx + x'yz + wx'y'z ; d = w'yz$$

Solution:

$$\begin{aligned}
 f &= \bar{w}xz(y+\bar{y}) + \bar{w}yz(x+\bar{x}) + \bar{x}yz(w+\bar{w}) + wx\bar{y}z \\
 &= \bar{w}xz + \bar{w}yz + \bar{w}xy + \bar{w}x\bar{y}z + w\bar{x}yz + w\bar{x}y\bar{z} + wx\bar{y}z
 \end{aligned}$$

$$\begin{aligned}
 d &= w'yz(x+\bar{x}) \\
 &= wxyz + w\bar{x}yz
 \end{aligned}$$



	$\bar{Y}Z$	$\bar{Y}\bar{Z}$	$\bar{Y}Z$	YZ	$\bar{Y}\bar{Z}$
$\bar{W}\bar{X}$	0	0	1	1	
$\bar{W}X$	0		1	0	
$W\bar{X}$	0	1	X	0	
WX	0	0	X	1	

$$\begin{aligned}
 Y_1 &= \bar{W}\bar{X}Y_2 + \bar{W}\bar{X}Y\bar{Z} + W\bar{X}Y_2 + W\bar{X}Y\bar{Z} \\
 &= \bar{W}\bar{X}Y + W\bar{X}Y = \bar{X}Y \\
 Y_2 &= \bar{W}X\bar{Y}Z + \bar{W}X\bar{Y}Z + W\bar{X}\bar{Y}Z + W\bar{X}Y\bar{Z} \\
 &= \bar{W}XZ + W\bar{X}Z \\
 &= XZ
 \end{aligned}$$

$$Y = \bar{X}Y + XZ$$

81

POS Simplifications:

Q1 Minimize the expression to minimised pos form using K-map -

$$Y = (A+B+C)(A+\bar{B}+\bar{C})(\bar{A}+\bar{B}+\bar{C})(\bar{A}+B+C)(A+B+C)$$

Solution :

$$\begin{aligned}
 A+B+\bar{C} &= M_1, A+\bar{B}+\bar{C} = M_3, \bar{A}+\bar{B}+\bar{C} = M_7, \bar{A}+B+C = M_4, \\
 A+B+C &= M_0
 \end{aligned}$$

K-map :

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	0	0	0	1
A	0	1	0	1

$$\begin{aligned}
 Y &= \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + \\
 &\quad \bar{A}BC + ABC \\
 &= \bar{B}\bar{C} + \bar{A}C + BC
 \end{aligned}$$

$$Y = \overline{\bar{B}\bar{C} + \bar{A}C + BC}$$

$$= (\bar{B}\bar{C}) + (\bar{A}C) + (BC)$$

$$/ Y = (B+C)(A+\bar{C})(\bar{B}+\bar{C})$$

Q2 Show the SOP & POS circuits for the karnaugh map given below.

0	0	0	0
0	0	0	1
1	1	1	1
1	1	1	1

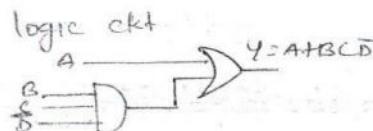
Solution: (i) SOP

K-map

0	0	0	0
0	0	0	1
1	1	1	1
1	1	1	1

expression

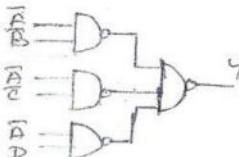
$$Y = A+B\bar{C}\bar{D}$$



(ii) POS

0	0	0	0
0	0	0	1
1	1	1	1
1	1	1	1

$$\begin{aligned}
 Y &= \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{A}\bar{D} \\
 &= (A+B)(A+C)(A+D)
 \end{aligned}$$





Q3 Give Simpliest Pos form of k-map.

Solution:

0	0	1	0
0	0	1	1
X	X	X	1
X	X	X	0

0	0	1	0
0	0	1	1
X	X	X	1
X	X	X	0

82

Q4 Minimize the following expression in the pos form.

$$y = (\bar{A} + \bar{B} + C + D) (\bar{A} + \bar{B} + \bar{C} + D) (A + \bar{B} + \bar{C} + \bar{D}) (A + B + C + D) \\ (A + \bar{B} + \bar{C} + D) (A + \bar{B} + \bar{C} + \bar{D}) (A + B + C + D) (\bar{A} + \bar{B} + C + \bar{D})$$

Solution:

AB	CD	$\bar{C}\bar{D}$	$C\bar{D}$	$C\bar{D}$
AB	0	1	1	1
$\bar{A}B$	1	1	0	0
AB	0	0	0	0
$\bar{A}B$	0	1	1	1

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D + \\ A\bar{B}B\bar{D} + A\bar{B}B\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + \\ ABC\bar{D} + ABC\bar{D} \\ = B\bar{C}\bar{D} + AB\bar{C} + ABC + ABC + ABC$$

$$Y = B\bar{C}\bar{D} + AB\bar{C} + BC$$

$$Y = (B + C + D) (\bar{A} + \bar{B}) (\bar{B} + \bar{C})$$

Q5 Reduce the following function using k-map technique.

$$f(A, B, C, D) = \overline{\text{IM}}(0, 2, 3, 8, 9, 12, 13, 15)$$

= Ans

$$Y = (\bar{A} + \bar{B} + \bar{D}) (A + B + \bar{C}) (\bar{A} + C) (A + B + D) \\ (\bar{A} + \bar{B} + \bar{D}) (A + B + \bar{C}) (\bar{A} + C) (B + C + D)$$

Q6 Reduce the following function using k-map technique and implement using basic gates.

$$f(A, B, C, D) = \overline{\text{IM}}(0, 3, 4, 7, 8, 10, 12, 14) + d(2, 6)$$

Solution:

Step 1:
K-map

0	1	0	X
0	1	0	X
0	1	1	0
0	1	1	0



Q3 Give Simplified POS form of k-map.

Solution:

0	0	1	0
0	0	1	1
X	X	X	1
X	X	X	0

0	0	1	0
0	0	1	1
X	X	X	1
X	X	X	0

82

Q4 Minimize the following expression in the POS form.

$$Y = (\bar{A} + \bar{B} + C + D) (\bar{A} + \bar{B} + \bar{C} + D) (\bar{B} + \bar{B} + C + \bar{D}) (A + B + C + D) \\ (A + \bar{B} + \bar{C} + D) (A + \bar{B} + \bar{C} + \bar{D}) (A + B + C + D) (A + \bar{B} + C + \bar{D})$$

Solution:

\bar{AB}	\bar{CD}	\bar{BC}	CD	$C\bar{D}$
\bar{AB}	(0)	1	1	1
\bar{AB}	1	1	0	0
AB	(0)	0	0	0
AB	(0)	1	1	1

$$Y = \bar{ABC}\bar{D} + \bar{ABC}\bar{D} + AB\bar{C}\bar{D} + AB\bar{C}D + \\ AB\bar{C}D + AB\bar{C}\bar{D} + \bar{ABC}\bar{D} + \bar{ABC}\bar{D} + \\ \bar{BC}\bar{D} + ABC\bar{D} \\ = B\bar{C}\bar{D} + AB\bar{C} + ABC + \bar{ABC} + ABC \\ Y = B\bar{C}\bar{D} + AB + BC \\ Y = (B + C + D)(\bar{A} + \bar{B})(\bar{B} + \bar{C})$$

Q5 Reduce the following function using K-map technique.

$$f(A, B, C, D) = \overline{\text{IM}}(0, 2, 3, 8, 9, 12, 13, 15)$$

= Ans

$$Y = (\bar{A} + \bar{B} + \bar{D}) (\bar{A} + B + \bar{C}) (\bar{A} + C) (\bar{A} + B + D) \quad 08 \\ (\bar{A} + \bar{B} + D) (\bar{A} + B + \bar{C}) (\bar{A} + C) (B + C + D)$$

Q6 Reduce the following function using K-map technique and implement using basic gates.

$$f(A, B, C, D) = \overline{\text{IM}}(0, 3, 4, 7, 8, 10, 12, 14) + d(2, 6)$$

Solution:

Step 1:
K-map

0	1	0	X
0	1	0	X
0	1	1	0
0	1	1	0

84

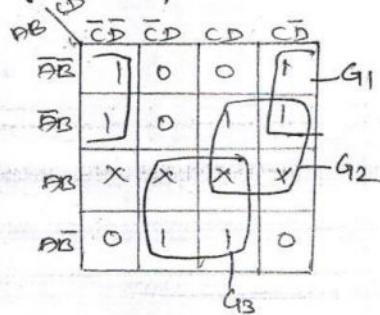
SEP	1000	0
OCT	1001	1
NOV	1010	0
DEC	1011	1
	1100	X
	1101	X
	1110	X
	1111	X

(i) Boolean expressions to Σ_m & Π_M

$$Y = \Sigma_m(0, 2, 4, 6, 7, 9, 11) + \Pi_m(12, 13, 14, 15)$$

$$Y = \Pi_M(1, 3, 5, 8, 10) + \Pi_m(12, 13, 14, 15)$$

(ii) K-map



$$Y_1 = \overline{A}B\overline{C}D + \overline{A}B\overline{C}\overline{D} + \overline{A}B\overline{C}D + \overline{A}B\overline{C}\overline{D}$$

$$= \overline{A}B\overline{C}D + \overline{A}B\overline{C}\overline{D}$$

$$= \overline{A}B\overline{D}$$

$$Y_2 = \overline{A}B\overline{C}D + \overline{A}B\overline{C}\overline{D} + A\overline{B}C\overline{D} + A\overline{B}C\overline{D}$$

$$= \overline{A}B\overline{C}D + A\overline{B}C\overline{D}$$

$$= BC$$

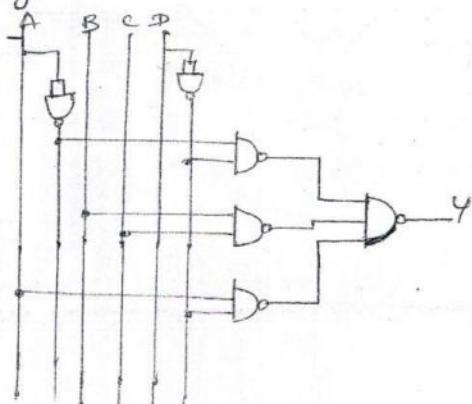
$$Y_3 = A\overline{B}C\overline{D} + A\overline{B}C\overline{D} + A\overline{B}\overline{C}D + A\overline{B}\overline{C}D$$

$$= AB\overline{D} + A\overline{B}D$$

$$= AD$$

$$\boxed{Y = \overline{A}B\overline{D} + B\overline{C} + AD}$$

v) logic circuit



SIMPLIFICATION BY QUINE-MCCLUSKY METHOD:

85

Reduction to logic equation by Karnaugh map method depends on the user's ability to identify patterns that give largest size. Also the method becomes difficult to adapt for simplification of 5 or more variables.

Quine-Mcclusky method is a systematic approach for logic simplification that does not have those limitations and also easily be implemented in a digital computer.

Determination of prime Implicants:

Quine-Mcclusky method involves preparation of 2 tables. One determines Prime Implicants and other selects essential Prime Implicants to get minimal expression.

Prime Implicants are expressions with least no of literals that represents all the terms given in a truth table.

Prime Implicants are examined to get essential Prime Implicants for a particular expression that avoids any type of duplication.

Ques 1. Solve the TruthTable by Using QM method.

ABCD	Y	Min term
0 0 0 0	1	m ₀
0 0 0 1	1	m ₁
0 0 1 0	1	m ₂
0 0 1 1	1	m ₃
0 1 0 0	0	m ₄
0 1 0 1	0	m ₅
0 1 1 0	0	m ₆
0 1 1 1	0	m ₇
1 0 0 0	0	m ₈
1 0 0 1	0	m ₉
1 0 1 0	1	m ₁₀
1 0 1 1	1	m ₁₁
1 1 0 0	1	m ₁₂
1 1 0 1	1	m ₁₃
1 1 1 0	1	m ₁₄
1 1 1 1	1	m ₁₅



Solution:

86

Step 1 :

- i) Find all the terms that gives output 1 from Truth Table and arrange them according to number of 1's.

And divide them as different groups according to the no. of 1's.

Stage 1	
ABCD	Minterms
G ₁ 0000	(0) ^v
0001	(1) ^v
0010	(2) ^v
0011	(3) ^v
G ₂ 1010	(10) ^v
1100	(12) ^v
1011	(11) ^v
G ₃ 1101	(13) ^v
1110	(14) ^v
G ₄ 1111	(15) ^v

Step 2 :

Stage 2	
ABCD	Minterms
G ₁ 000-	(0,1) ^v
00-	(0,2) ^v
00-1	(1,3) ^v
G ₂ 001-	(2,3) ^v
-010	(2,10) ^v
-011	(3,11) ^v
G ₃ 101-	(10,11) ^v
1-10	(10,14) ^v
110-	(12,13) ^v
11-0	(12,14) ^v
1-11	(11,15) ^v
G ₄ 11-1	(13,15) ^v
111-	(14,15) ^v

Compare each binary number with every term in the adjacent next higher category and if they differ by only one position, put that term in the next column with \sim in the position that they differed. And then group them according to number of 1's.

(o) If first group combines with (1) of second group to form (0,1) in stage 2, and can be represented by $\bar{A}B\bar{C}(000-)$.

Logic of this representation comes from the fact that minterm $\bar{A}\bar{B}\bar{C}\bar{D}(0)$ and $\bar{A}\bar{B}\bar{C}D(1)$ can be combined as $\bar{A}B\bar{C}(\bar{D}+D) = \bar{A}B\bar{C}$

Step 3 :

In stage 3, combine members of different groups of stage 2 in a similar way. Now it will have two \sim elements in each combination. This means each combination requires two literals to represent it.



Stages	
ABCD	Minterms
00--	(0, 1, 2, 3)
00--	(0, 2, 1, 3)
-01-	(2, 3, 10, 11)
-01-	(2, 10, 3, 11)
1-1-	(10, 11, 14, 15)
1-1-	(10, 14, 11, 15)
11--	(12, 13, 14, 15)
11--	(12, 14, 13, 15)

87

Stage 1 minterms should be covered by Stage 2 minterms. Same way Stage 2 minterms should be covered by Stage 3 minterms.

Check it one by one and put check mark (✓) or (X).

⇒ Selection of Prime Implicants: (Prime Implicant chart):-

Once we determined prime implicants that covers all the terms of a truth table, next we should select essential prime implicants and remove redundancy or duplication among them.

Prime Implicants	0	1	2	3	10	11	12	13	14	15
$\bar{A}\bar{B}$ (0, 1, 2, 3)	✓	✗	✓	✓						
$B\bar{C}$ (2, 3, 10, 11)			✓	✓	✓	✓				
$A\bar{C}$ (10, 11, 14, 15)					✓	✓			✓	✓
$A\bar{B}$ (12, 13, 14, 15)							✓	✗	✓	✓

Selection of essential prime implicants from this table is done by

to find minimum number of prime implicants that covers many minterms.

Here $\bar{A}\bar{B}$ & $A\bar{B}$ covers many minterms. So we should include them in final expression. They are essential prime implicant

2. $B\bar{C}$ & $A\bar{C}$ covers (10, 11) which are not included by others. So one of them has to be included in the list of essential prime implicants.

And the Y is

$$Y = \bar{A}\bar{B} + B\bar{C} + AB \\ \text{or} \\ \bar{A}\bar{B} + A\bar{C} + AB$$



Q2 Solve $f(a,b,c,d) = \Sigma m(0,1,2,5,6,7,8,9,10,14)$ by
Quine McCluskey method.

Solution:

Minterm	ABCD
m ₀	0000
m ₁	0001
m ₂	0010
m ₅	0101
m ₆	0110
m ₇	0111
m ₈	1000
m ₉	1001
m ₁₀	1010
m ₁₄	1110

⇒ Table 1: Determination of Prime Implicants:

	stage 1	stage 2	stage 3
	ABCD minterm	ABCD minterm	ABCD minterm
G ₁	0000 (0) ^v	000- (0,1) ^v	-00- (0,1,8,9)
	0001 (1) ^v	00-0 (0,2) ^v	-0-0 (0,2,8,10)
G ₂	0010 (2) ^v	-000 (0,8) ^v	-00- (0,8,1,9)
	1000 (8) ^v	0-01 (1,9) ^v	-0-0 (0,8,2,10)
G ₃	0101 (5) ^v	0-10 (2,6) ^v	--10 (2,6,10,14)
	0110 (6) ^v	-010 (2,10) ^v	--10 (2,10,6,14)
G ₄	1001 (9) ^v	100- (8,9) ^v	
	1010 (10) ^v	10-D (8,10) ^v	
	0111 (7) ^v	01-1 (5,17)	
	1110 (14) ^v	011- (6,17)	
		-110 (8,14) ^v	
		1-10 (10,14) ^v	

⇒ Table 2: Prime Implicant chart:

Prime Implicants	0	1	2	5	6	7	8	9	10	14
$\bar{B}C(0,1,8,9)$	✓	✓					✓	✓		
$\bar{B}D(0,2,8,10)$	✓		✓				✓		✓	✓
$C\bar{D}(2,6,10,14)$					✓					
$A\bar{E}DC(1,5)$				✓						
$\bar{A}BD(5,11)$				✓		✓				
$\bar{A}BC(6,11)$					✓		✓			

$\bar{B}C$ & $C\bar{D}$ covers all the minterms except 5 & 7. $\bar{A}BD$ covers both

$$\therefore Y = \bar{B}C + C\bar{D} + \bar{A}BD$$

89

Q3 Simplify the following Boolean function by choosing a 4x4 method.
 $f(A, B, C, D) = \sum(0, 2, 3, 6, 7, 8, 10, 12, 13)$

Solution:

Minterm	ABCD
m0	0000
m2	0010
m3	0011
m6	0110
m7	0111
m8	1000
m10	1010
m12	1100
m13	1101

⇒ Table 1 : Determination of Prime Implicants:

Stage 1 : Arrange the minterms according to number of 1's

Stage 2 : compare each binary number with every term in the adjacent next higher category and if they differ by only one position, put that term in Stage 2 with 'x' in the position that they differed.

Stages : Combine members of different groups

Stage 2 in a similar way.

Stage 1		Stage 2		Stage 3
	ABCD minterm		ABCD minterm	ABCD minterm
G1	0000 (0)✓	00-0	(0,2)✓	-0-0 (0,12,8,10)
	0010 (2)✓	-000	(0,8)✓	-0-0 (0,8,2,10)
G2	1000 (8)✓	001-	(2,3)✓	0-1- (2,3,6,7)
	0011 (3)✓	0-10	(2,6)✓	0-1- (2,6,3,9)
G3	0110 (6)✓	-010	(2,10)✓	
	1010 (10)✓	10-	(8,10)✓	
G4	1100 (12)✓	1-00	(8,12)X	
	0111 (7)✓	0-11	(3,7)✓	
	1101 (13)✓	011-	(6,11)✓	
		110-	(12,13)X	

Stage 1 minterms should be covered by Stage 2 minterms. and Stage 2 minterms should be covered by Stage 3 minterms.

⇒ Table 2: Prime Implicant chart:

Prime Implicants	0	2	3	6	7	8	10	12	13
ĀB̄ (8, 12)							✓		
AB̄C (12, 13)								✓	
B̄B̄ (0, 2, 8, 10)	✓							✓	
ĀC (2, 3, 6, 7)		✓	✓	✓	✓				

90

$$Y = \overline{B} \overline{D} + \overline{A} C + A \overline{B} \overline{C}$$

Q4. Using Q-M method, simplify the expression
 $f(A, B, C, D) = \sum m(0, 3, 5, 6, 7, 11, 14)$. Write the gate diagram
 for the Simplified equation using NAND-NAND gate.

Solution:

Minterms	ABCD
m0	0000
m3	0011
m5	0101
m6	0110
m7	0111
m11	1011
m14	1110

⇒ Table 1: Determination of Prime Implicants:

	Stage 1	Stage 2	Stage 3
G_1	ABCD minterms	ABCD minterms	ABCD minterms
	0000 (0) X	0-11 (3, 7)	-
G_2	0011 (3) ✓	-011 (3, 11)	-
	0101 (5) ✓	01-1 (5, 7)	-
G_3	0110 (6) ✓	011- (6, 7)	-
	0111 (7) ✓	-110 (6, 14)	-
	1011 (11) ✓		
	1110 (14) ✓		



⇒ Table 2 : Prime Implicant chart :

Prime Implicants	0	3	5	6	7	11	14
$\bar{A}B\bar{C}\bar{D}$ (0)	(V)						
$\bar{A}CD$ (3, 7)			(V)				(V)
$\bar{B}CD$ (3, 11)		(V)					
$\bar{A}BD$ (5, 7)				(V)			
$\bar{A}BC$ (6, 7)					(V)		
$\bar{B}CD$ (6, 14)	-				(V)	-	(V)

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{D} + \bar{A}C\bar{D} + B\bar{C}\bar{D}$$

Q5 Minimize the expression using Quirk-Mccluskey method

$$Y = \bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + AB\bar{C}D + A\bar{B}\bar{C}D + \bar{A}\bar{B}CD$$

Solution:

Minterms	ABCD
m ₄	0100
m ₅	0101
m ₁₂	1100
m ₁₃	1101
m ₉	1001
m ₂	0010

⇒ Table 1 : Determination of Prime Implicants :

	Stage 1	Stage 2	Stage 3
G ₁	ABCD minterm	ABCD minterm	ABCD minterm
	0010 (2) X	010- (4,5) V	10- (4,5,12,13)
	0100 (4) V	-100 (4,12) V	-10 - (4,12,5,13)
G ₂	0101 (5) V	-101 (5,13) V	
	1001 (9) V	1-01 (9,13) X	
	1100 (12) V	110- (12,13) V	
G ₃	1101 (13) V		

94

Prime Implicants	0	1	2	5	6	7
$\bar{A}\bar{B}$ (0,1)	✓	✓				
$\bar{A}C$ (0,2)	✓		✓			
$\bar{B}C$ (1,5)		✓				
BC (2,6)			✓		✓	
AC (5,7)				✓		
AB (6,7)					✓	✓

Type 2:

To cover 0, this time we choose $\bar{A}C$. It covers 0 & 2.

To cover we choose $\bar{B}C$. It covers 1 & 5.

To cover 6 & 7, we choose AB .

$$\therefore Y = \bar{A}C + \bar{B}C + AB$$

PETRICK'S METHOD :-

Petrick's method is a technique for determining all minimum SOP solutions from a prime implicant chart.

As the number of variables increases, the number of prime implicants and the complexity of the prime implicant chart may increase significantly.

In such cases, a large amount of trial and error may be required to find the minimum solutions.

Petrick's method is a more systematic way of finding all minimum solutions from a prime implicant chart than the method used previously.

Q) Give simplified logic equation using Petrick's method.
 $F = \sum m(0,1,2,5,6,7)$



Solution :

95

⇒ Table 1 : Determination of Prime Implicants :

	Stage 1	Stage 2
	ABC minterm	ABC minterm
G ₁	000 (0) ^v	00- (0,1)
	001 (1) ^v	0-0 (0,2)
G ₂	010 (2) ^v	-01 (1,5)
	011 (5) ^v	-10 (2,6)
-G ₃	101 (6) ^v	1-1 (5,7)
	110 (7) ^v	11- (6,4)
G ₄	111	

⇒ Table 2 : Prime Implicant chart using Palatt's method :

Prime Implicants	0	1	2	5	6	7
P ₁ ĀB̄ (0,1)	✓	✓				
P ₂ ĀZ (0,2)		✓				
P ₃ B̄C (1,5)			✓			
P ₄ BC (2,6)				✓		
P ₅ AC (5,7)					✓	
P ₆ AB (6,4)					✓	✓

We will form a logic function, P which is true when all of the minterms in the chart have been covered.

0 is covered by P₁ & P₂

1 is covered by P₁ & P₃

2 is covered by P₂ & P₄

5 is covered by P₃ & P₅

6 is covered by P₄ & P₆

7 is covered by P₅ & P₆

$$\therefore P = (P_1 + P_2)(P_1 + P_3)(P_2 + P_4)(P_3 + P_5)(P_4 + P_6)(P_5 + P_6) = 1 \quad \text{①}$$

The next step is to reduce P to a minimum SOP form.

First we will use ordinary distributive law

$$(x+y)(x+z) = x+yz$$

Proof

$$\begin{aligned}
 &= xx + xz + xy + yz \\
 &= x + xz + xy + yz \\
 &= x(1+z+y) + yz \quad [\because 1+z+y=1] \\
 &= x + yz
 \end{aligned}$$



SIMPLIFICATION USING MAP-ENTERED VARIABLES:

98

By using map-entered variables, Karnaugh map techniques can be extended to simplify functions with more than 4 or 5 variables.

- Q1. Simplify the following function using map-entered variable method. $F(A, B, C, D) = \overline{D}\overline{B}C + \overline{A}BC + \overline{A}B\overline{C}\overline{D} + ABD + (ABC)$

Solution:

Step 1: expression to K-map

	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
\overline{A}	0	1	1	D
A	0	X	D	0

Step 2: K-map Simplification

(i) when $D = 0$

	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
\overline{A}	0	1	1	0
A	0	X	0	0

$$Y = \overline{A}\overline{B}C + \overline{A}BC$$

$$Y = \overline{A}C$$

(ii) when $D = 1$

	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
\overline{A}	0	1	1	1
A	0	X	1	0

$$\begin{aligned} Y &= \overline{A}\overline{B}L + \overline{A}BL + \overline{A}BC + ABC + \\ &\quad \overline{ABC} + \overline{A}BC \\ &= \overline{AC} + A\overline{C} + \overline{AB} \\ &= C + \overline{AB} \end{aligned}$$

Here $D = 1 \therefore Y = D(C + \overline{AB})$

$$= CD + \overline{AB}D$$

$$Y = \overline{A}C + CD + \overline{AB}D$$

We can check the same question using K-map

$$F = \overline{A}\overline{B}C + \overline{A}BC + \overline{A}B\overline{C}D + ABCD + (ABC)$$

$$\begin{aligned} &= \overline{A}\overline{B}CD + \overline{A}\overline{B}C\overline{D} + \overline{A}BCD + \overline{ABC}\overline{D} + \overline{ABC}D + ABCD + \\ &\quad (ABC\overline{D} + A\overline{B}CD) \end{aligned}$$

$AB\bar{C}D$	$\bar{A}\bar{B}$	$\bar{C}D$	$\bar{C}\bar{D}$	G_3
$\bar{A}B$	0	0	1	1
$\bar{A}B$	0	1	1	1
$A\bar{B}$	0	0	1	0
$A\bar{B}$	0	0	X	X

G_1

99

$$Y_1 = \bar{A}\bar{B}C + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D}$$

$$= \bar{A}B C + \bar{A}B C$$

$$= \bar{A}C$$

$$Y_2 = \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}D + A\bar{B}C\bar{D} + A\bar{B}CD$$

$$= \bar{A}CD + ACD$$

$$= CD$$

$$Y_3 = \bar{A}B\bar{C}D + \bar{A}B\bar{C}D$$

$$= \bar{A}BD$$

$$\boxed{Y = \bar{A}C + CD + \bar{A}BD}$$

— X — X —



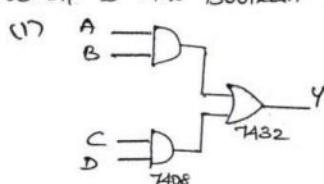
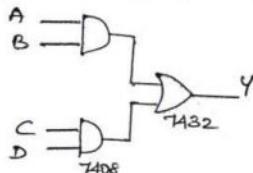
ADE Module - 3

CSE IIIrd sem

MODULE - 3 COMBINATIONAL CIRCUIT DESIGN AND SIMULATION USING GATES

What is the Boolean equation for the figures

(i)

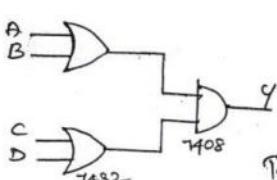


This circuit is called an AND-OR network. Because input AND gate drives an output OR gate.

$$Y = AB + CD$$

AND-OR network always produce sum-of-product (SOP) equations.

(ii)



This circuit is called an OR-AND network because OR gate drives AND gate.

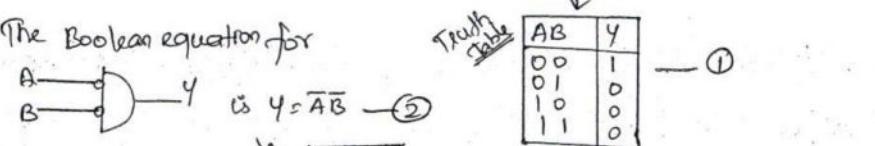
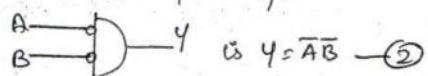
$$Y = (A+B) \cdot (C+D)$$

OR-AND network produces product of sum (POS) equations.

⇒ De Morgan's first theorem:

The Boolean equation for $\overline{A \rightarrow B} = Y$ is $Y = \overline{A} + \overline{B}$ (NOR) →

The Boolean equation for



Truth Table

AB	Y
00	1
01	0
10	0
11	0

→ ①

Truth Table

AB	Y
00	1
01	0
10	0
11	0

→ ②

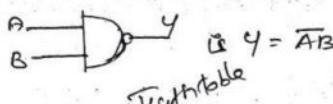
① = ②, so we can equate RHS & LHS

101

$A + \bar{B} = \bar{A} \cdot \bar{B}$ This identity is known as De-Morgan's first theorem. It says, the complement of a sum equals the product of the complements.

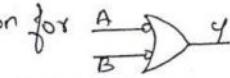
De-Morgan's Second Theorem:

The Boolean equation for



Truth Table

The Boolean equation for



is $Y = \bar{A} + \bar{B}$

Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

— ②

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

— D

① = ②

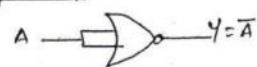
$\bar{A}B = \bar{A} + \bar{B}$ This identity is known as De-morgan's second theorem. It says, the complement of a product equals the sum of the complements.

→ Basic Gates:
AND, OR & NOT

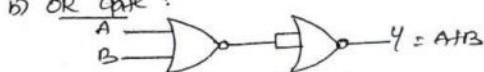
→ Universal Gates:
NOR & NAND

→ Universality of NOR Gate:
Universality is nothing but, all other logic gates can be obtained from NOR gates.

a) NOT Gate:



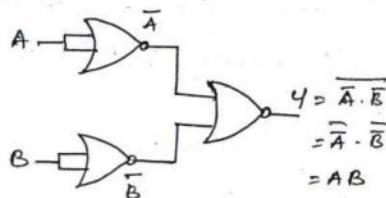
b) OR Gate:





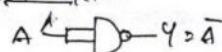
c) AND Gate:

102

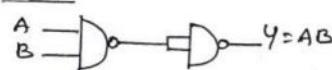


→ Universality of NAND gate:

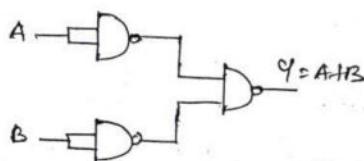
a) NPT Gate:



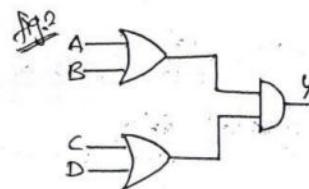
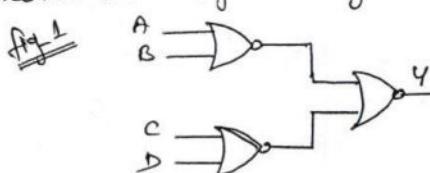
b) AND Gate



c) OR Gate



ex) Prove that Fig 1 is logically equivalent to Fig. 2



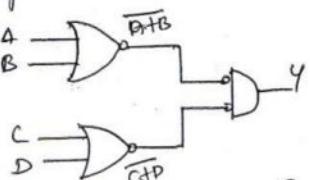
Solution

In figure 2.

$$Y = (A+B) \cdot (C+D) \rightarrow ①$$

In figure 1, the third NOR can be replaced by bubbled

AND.



The Boolean eqn of this is

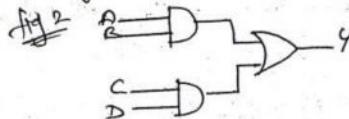
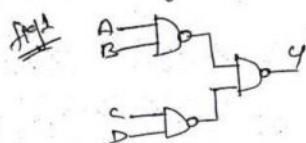
$$Y = (A+B) \cdot (C+D) \rightarrow ②$$

$$① = ②$$

Hence Proved.

103

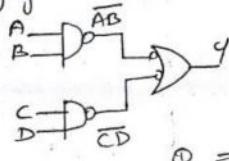
ex.2 prove fig 1 is equivalent to fig 2.



solution

$$\text{In fig 2, } Y = AB + CD \quad \text{---(1)}$$

In figure 1, the third NAND can be replaced by bubbled OR.

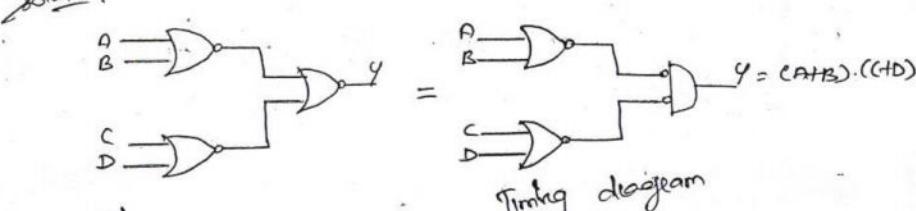


The Boolean eqn of this is

$$Y = AB + CD \quad \text{---(2)}$$

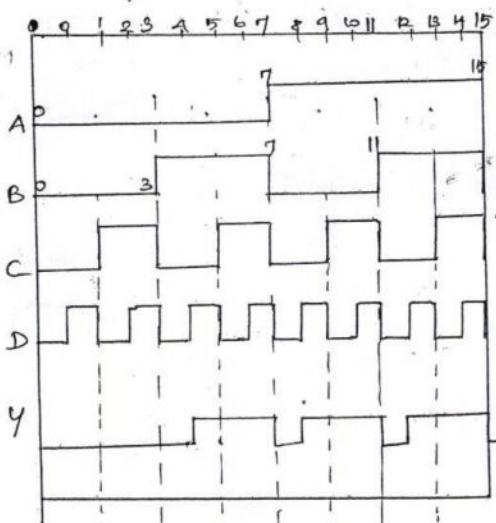
Hence proved

ex.3 what is the Truth table for the NOR-NOR circuit. Also convert that into timing diagram.



Truth table

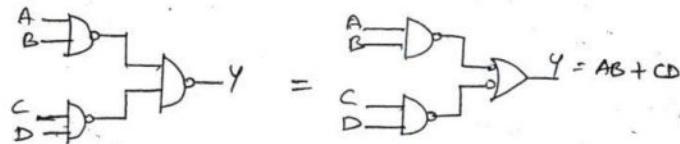
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1



104

Q. What is the Truth Table of NAND-NAND circuit. also convert that into timing diagram.

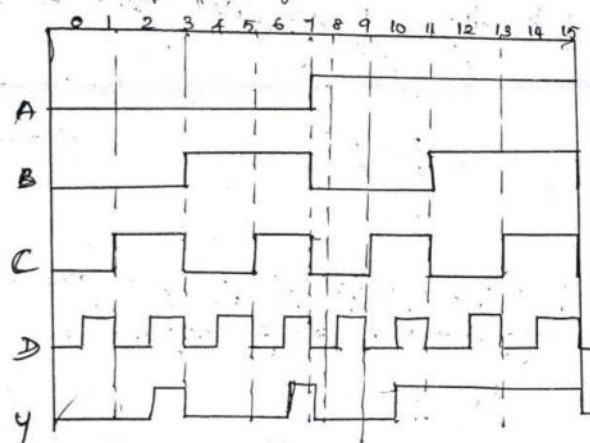
Solution:



Truth table:

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Timing diagram

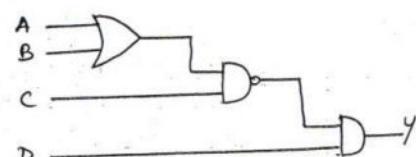


Ex-5 Implement $(A+B)(C+D)$ Using Universal gates.

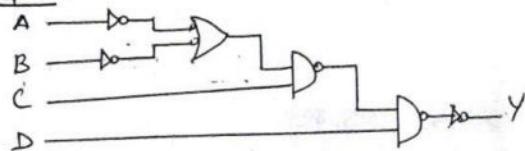
Universal gates are NAND & NOR

(i) Using NAND gates.

Step 1:

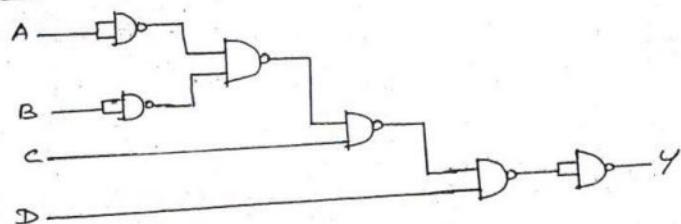


Step 2:





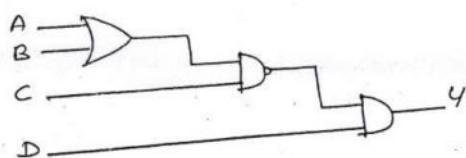
Step 8 :



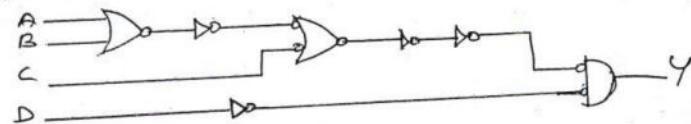
105

(ii) Using NOR Gates :

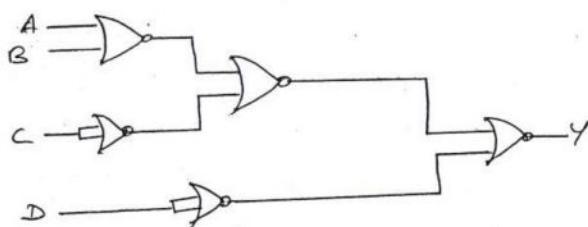
Step 1 :



Step 2 :



Step 3 :



Review of Combinational Circuit Design :

The first step in the design of a combinational switching circuit is usually to set up a truth table which specifies the outputs as a function of the input variables. For n input variables this table will have 2^n rows.

The next step is to derive simplified algebraic expressions for the output functions using Karnaugh maps, the Quine-McCluskey method or a similar procedure.



106

The resulting equations can then be simplified algebraically. The simplified algebraic expressions are then manipulated into the proper form, depending on the type of gates to be used in realizing the circuit.

When a circuit has 2 or more outputs, common terms in the output functions can often be used to reduce the total number of gates or gate inputs.

When designing circuits with 3 or more levels, looking for common terms on the Karnaugh maps may be of little value. In this case, the designer will often minimize the functions separately and then use ingenuity to factor the expressions in such a way to create common terms.

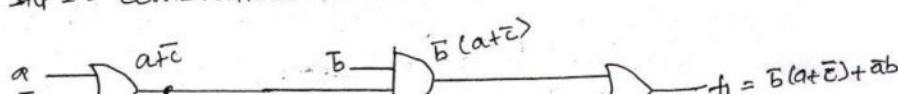
Minimum 2-levels AND-OR, NAND-NAND, OR-NAND and NOR-OR circuits can be realized using the minimum sum of products (SOP).

Minimum 2-levels OR-AND, NOR-NOR, AND-NOR and NAND-AND circuits can be realized using the minimum product of sum (POS).

Design of multi-level, multi-output NAND-gate circuits is most easily accomplished by first designing a circuit of AND & OR-gates. Usually, the best starting point is the minimum SOP expressions for the output functions. These expressions are then factored in various ways until an economical circuit of the desired form can be found.

If this circuit has an OR-gate at each output and is arranged so that an AND-gate or OR-gate output is never connected to the same type of gate, a direct connection to a NAND-gate circuit is possible. Conversion is accomplished by replacing all of the AND & OR-gates with NAND-gates and then inverting any literals which appear as input to the first, third, fifth... levels.

Step 2: Combinational circuit:



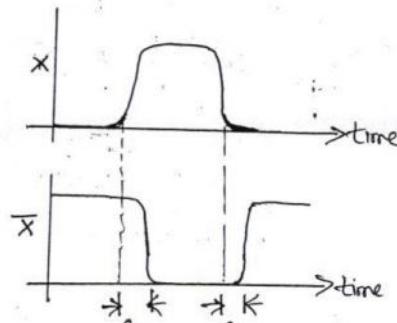
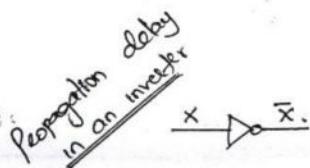
109



110

GATE DELAYS AND TIMING DIAGRAMS:

When the input to a logic gate is changed, the output will not change instantaneously. The transistors or other switching elements within the gate take a finite time to react to a change in input. So that the change in the gate output is delayed with respect to the input change.

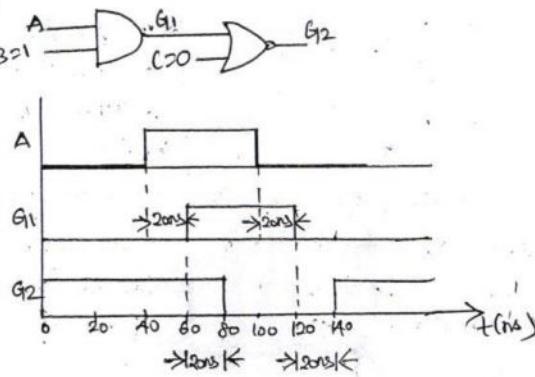


If the change in output is delayed by time ϵ , with respect to the input; then the gate has a propagation delay of ϵ .

Propagation delays for integrated circuit gates may be as short as a few nanoseconds, and in many cases these delays can be neglected. However, in the analysis of some types of sequential circuits, even short delays may be important.

Timing diagrams are frequently used in the analysis of sequential circuits. These diagrams show various signals in the circuit as a function of time.

Timing diagram
for AND-NOR circuit

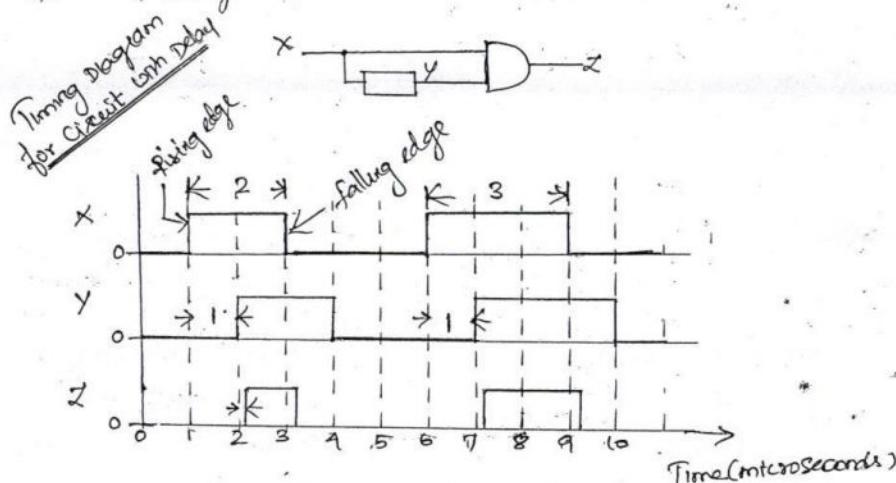




111

This is the timing diagram for a circuit with 2 gates. Let us assume that each gate has a propagation delay of 20ns. This timing diagram shows, what happens when gate inputs B & C are held at constant values 1 & 0 respectively.

Input A is changed to 1 at $t = 1\text{ microsecond}$ and then changed back to 0 at $t = 10\text{ microseconds}$. The output of gate G1 changes 20ns after A changes, and the output of gate G2 changes 20ns after G1 changes.



This circuit is having delay element. The input X consists of 2 pulses, the first of which is 2 microseconds wide and the second is 3 microseconds wide.

The delay element has an output Y which is same as the input except that it is delayed by 1 microsecond.

That is, Y changes to a value 1, after 1 microsecond of the rising edge of the X pulse, and returns to value 0, after 1 microsecond of the falling edge of the X pulse.

The output (Z) of the AND gate should be 1 during the time interval in which both X and Y are 1.



112

HAZARDS AND HAZARD COVERS :

The unwanted switching transients that may appear at the output of a circuit are called Hazards.

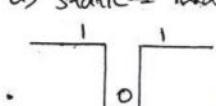
The main cause of hazards is the different propagation delays at different paths.

Hazards occur in the combinational circuits (are used in the asynchronous circuits), they may result in a transistor to a wrong stable state.

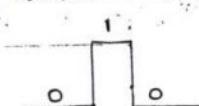
Hazard covers are additional terms in an equation that prevents occurring of them.

⇒ Types of Hazards:

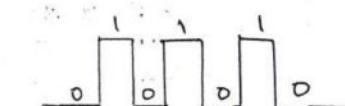
a) static-1 hazard



b) static-0 hazard



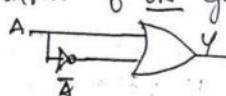
c) Dynamic hazards



(a) Static -1 Hazard:

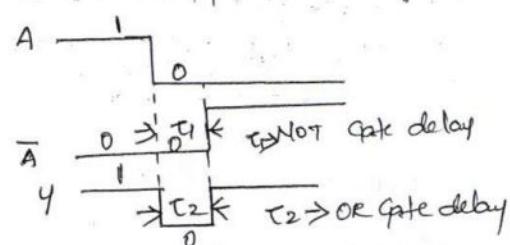
This type of Hazards occurs when $A = \bar{A}$ type "B" situation appears for a logic circuit for certain combination of other input and \bar{A} makes a transition $1 \rightarrow 0$.

An $A + \bar{A}$ condition should always generate 1 at the output of OR gate. i.e static-1



But the Not gate output takes finite time to change the state of it.

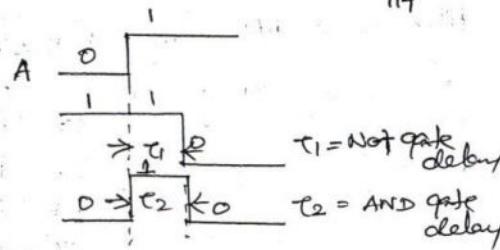
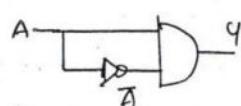
Thus for the OR gate there are 2 zeros appearing at its input for that small duration OR gate output becomes 0. The width of this zero is in nanosecond and it is called as glitch. For combinational circuit it may go unnoticed but in sequential circuit it may cause major malfunctioning.



113

How to remove static-1 hazard?

For this K-map



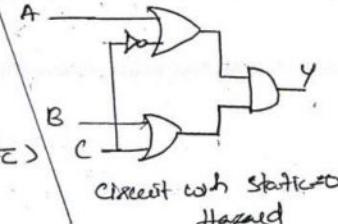
How to rectify Static-0 Hazard?

for this K-map

$\bar{A}\bar{B}$	$\bar{A}B$	$A\bar{B}$	AB
0 0	0 1	1 0	1 1
1 0	1 1	0 1	0 0
0 1	0 0	1 1	1 0
1 1	0 1	0 0	0 1

$$Y = (B + \bar{C})(A + \bar{C})$$

logic clk

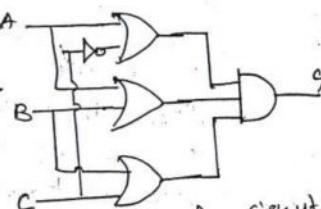


circuit w/ static-0 hazard

In this circuit if $B=0$ & $A=0$ and C makes a transition from $0 \rightarrow 1$ there will be static-0 hazard occurring at output. To prevent this we add one additional group

$\bar{A}\bar{B}$	$\bar{A}B$	$A\bar{B}$	AB
0 0	0 1	1 0	1 1
1 0	1 1	0 1	0 0
0 1	0 0	1 1	1 0
1 1	0 1	0 0	0 1

$$\rightarrow Y = (B + \bar{C})(A + \bar{C})(A + B)$$



hazard free circuit

c) Dynamic Hazard:

Dynamic hazard occurs when circuit output makes multiple transitions before it settles to a final value while the logic equation asks for only one transition.

An output transition designed as $1 \rightarrow 0$ may give $1 \rightarrow 0 \rightarrow 1 \rightarrow 0$ when such hazard occurs and $0 \rightarrow 1$ can behave like $0 \rightarrow 1 \rightarrow 0 \rightarrow 1$. The output of logic equation may be $Y = (A + \bar{A})A$ or $(A \cdot \bar{A}) + A$. These occurs in multi level clk's

having implicit static-1 and static-0 hazards

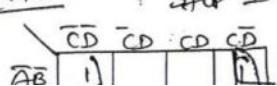
providing covers to such static-0 & static-1 hazards,

dynamic hazard can be prevented.

115

Ex: For a given boolean function, obtain the hazard free circuit $f(A, B, C) = \sum m(1, 3, 6, 7, 13, 15)$

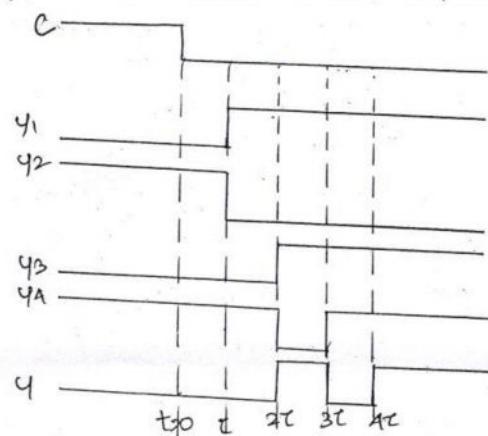
Solution: Step 1 : K map Simplification





117

The following timing diagram shows how a transition to 0 at input C for AB=11 causes dynamic hazard at the output



The Hazard can be prevented by using an additional two input AND gate fed by input A + B and replacing two input OR gate by a three input OR gate. The additional input of OR gate will be fed by output of the new AND gate.

SIMULATION AND TESTING OF LOGIC CIRCUITS :-

An important part of the logic design process is verifying that the final design is correct and debugging the design if necessary.

Logic circuit may be tested either by actually building them or by simulating them on a computer. Simulation is generally easier, faster and more economical.

As logic circuits become more and more complex, it is very important to simulate a design before building it. This is particularly true when the design is built in integrated circuit form, because fabricating an integrated circuit may take a long time and correcting errors may be very expensive.

118

Simulation is done for several reasons

→ Verification that the design is logically correct

→ Verification that the timing of the logic signal is correct

→ Simulation of faulty components in the circuit as an aid to finding tests for the circuit.

To use a computer program for simulating logic circuits,

→ first, specify the circuit components and connections

→ then, specify the circuit inputs and

→ finally, observe circuit outputs

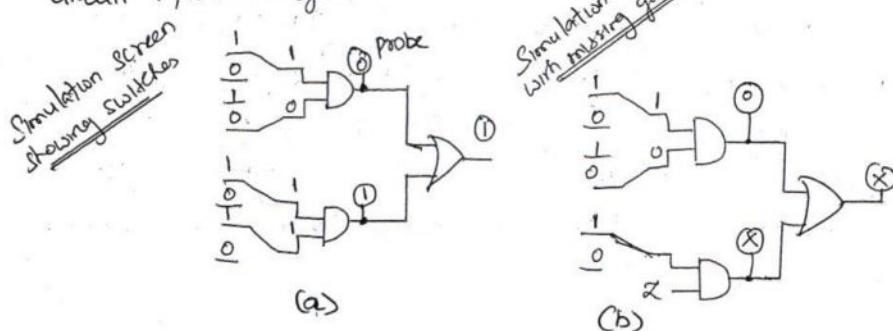
A simple simulator for combinational logic works as follows,

1. The circuit inputs are applied to the first set of gates in the circuit, and the outputs of those gates are calculated.

2. The outputs of the gates which changed in the previous step are fed into the next level of gate inputs. If the input to any gate has changed, then the output of gate is calculated.

3. Step 2 is repeated until no more changes in gate inputs occur. The circuit is then in a steady-state condition and the outputs may be read.

4. Step 1 through 3 are repeated everytime a circuit input changes.



119

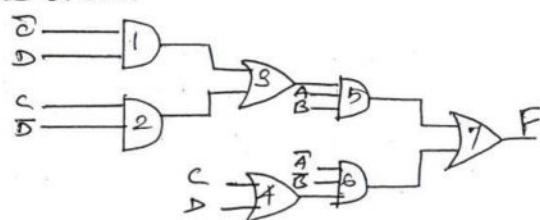
This is the typical simulation screen on a personal computer. The switches are set to 0 or 1 for each input. The probe indicates the value of each gate output.

120

If a circuit output is wrong for some set of input values, this may be due to several possible causes.

1. Incorrect design
2. Gates connected wrong
3. Wrong input signals to the circuit
4. Defective gates
5. Defective connecting wires

Ex-1 The function $F = AB(CD + C\bar{D}) + \bar{A}\bar{B}(C + D)$ is realized by the circuit



When $A=B=C=D=1$, the output F has the wrong value, and that gate's outputs are changed.

The reason for the incorrect value of F can be determined as follows,

1. The output of gate 7 is wrong. But this wrong output is consistent with the inputs to gate 7, that is $1+0=1$. \therefore One of the inputs to gate 7 must be wrong.

2. In order for gate 7 to have the correct output ($F=0$) both inputs must be 0. \therefore the output of stage 5 is wrong.

3. Either the output of stage 3 is wrong or the A or B input to gate 5 is wrong. Because $C\bar{D}+C\bar{D}=0$, the output of gate 3 is wrong.

4. The output of gate 3 is not consistent with the outputs of gates 1 & 2 because $0+0\neq 1$. Therefore either one of the inputs to gate 3 is connected wrong, gate 3 is defective or due to the input connections.

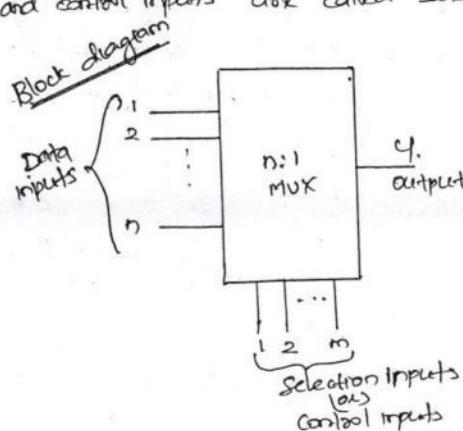


121

MUXES:

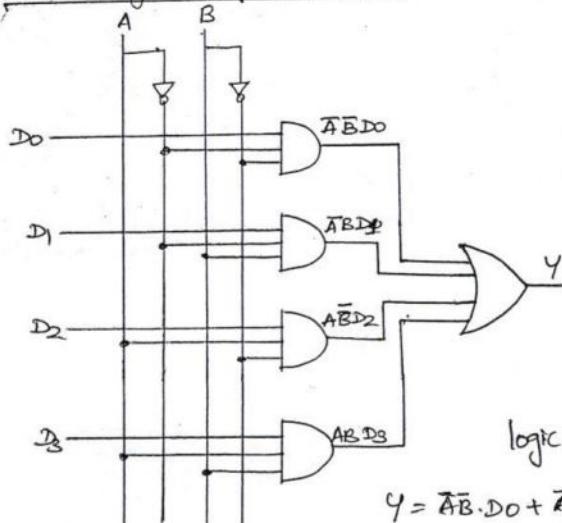
Multiplex → Many into one.

A multiplexer is a circuit with many inputs and only one output. By applying control signal we can steer any input to the output. Thus it is also called as data selector and control inputs are called select inputs.



Multiplexer has ' n ' input signals ' m ' control signals and 1 output signal.

Circuit diagram of a 1:1 MUX



Truth Table

A	B	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

logic equation of this circuit is

$$Y = \bar{A}\bar{B} \cdot D_0 + \bar{A}B \cdot D_1 + A\bar{B} \cdot D_2 + AB \cdot D_3$$

If $A=0, B=0$

$$\begin{aligned} Y &= \bar{0}\bar{0} \cdot D_0 + \bar{0}0 \cdot D_1 + 0\bar{0} D_2 + 00 D_3 \\ &= 1.1 \cdot D_0 + 1.0 D_1 + 0.1 D_2 + 0.0 D_3 \end{aligned}$$

$$\boxed{Y = D_0}$$

122

for $AB=00$, the first AND gate, to which D_0 is connected remains active and equal to D_0 and all other

128

The input bits are labeled D_0 to D_5 . Only one of these is transmitted to the output. That depends on $ABCD$ value.

When $ABCD = 0000$, the upper AND gate is enabled

\therefore data bit D_0 is transmitted to the output $Y = D_0$

The output can be written as

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} \cdot D_0 + \bar{A}\bar{B}\bar{C}D \cdot D_1 + \bar{A}\bar{B}C\bar{D} \cdot D_2 + \bar{A}B\bar{C}\bar{D} \cdot D_3 + \dots + A\bar{B}\bar{C}\bar{D} \cdot D_4 + ABC\bar{D} \cdot D_5$$

$\Rightarrow 8:1$ Multiplexer :

For 8 to 1 multiplexers we need 3 select lines, and there will be 8 AND gates each one having 2 inputs. 3 from select line and one from data inputs.

The final output is generated from an OR gate.

$$Y = \bar{A}\bar{B}\bar{C} \cdot D_0 + \bar{A}\bar{B}\bar{C} \cdot D_1 + \bar{A}\bar{B}C \cdot D_2 + \bar{A}BC \cdot D_3 + A\bar{B}\bar{C} \cdot D_4 + A\bar{B}C \cdot D_5 + \\ ABC \cdot D_6 + ABC \cdot D_7$$

for $ABC = 000$, multiplexer output $Y = D_0$

$$ABC = 011, \quad " \quad " \quad Y = D_3$$

\Rightarrow The 74150 :

In this we get the complement of the selected data bit rather than the data bit itself.

for instance $ABC = 011$, the output is D_1 . It has an inverter on the output that produces the complement of the selected data bit.

The 74150 is a 16 to 1 TTL multiplexer

Pin diagram

D_1	1	24	Vcc
D_2	2	23	D_8
D_5	3	22	D_9
D_4	4	21	D_{10}
D_3	5	20	D_{11}
D_2	6	19	D_{12}
D_1	7	18	D_B
D_0	8	17	D_A
Strobe	9	16	D_{15}
Y	10	15	D
A	11	14	C
GND	12	13	B

Truth table

A	B	C	D	Y
0	0	0	0	D_0
0	0	0	1	D_1
0	0	1	0	D_2
0	0	1	1	D_3
0	1	0	0	D_4
0	1	0	1	D_5
0	1	1	0	D_6
0	1	1	1	D_7
1	0	0	0	D_8
1	0	0	1	D_9
1	0	1	0	D_{10}
1	0	1	1	D_{11}
1	1	0	0	D_{12}
1	1	0	1	D_B
1	1	1	0	D_A
1	1	1	1	D_{15}



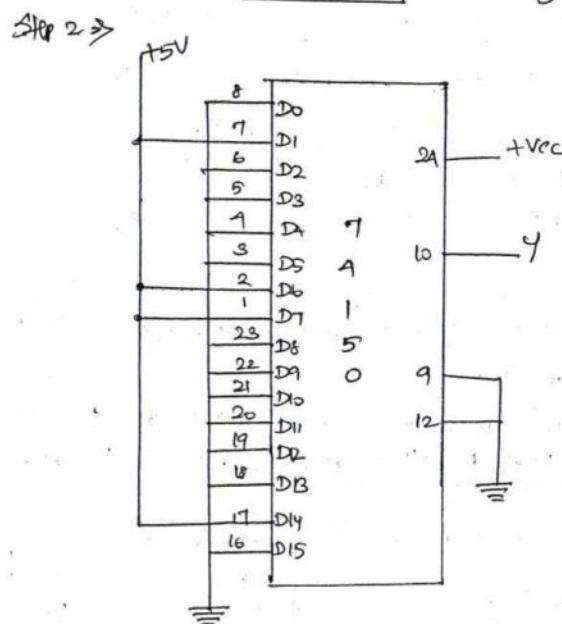
Q1 Implement the below Truth Table using 74150.

124

Solution

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Step 1 \Rightarrow Y



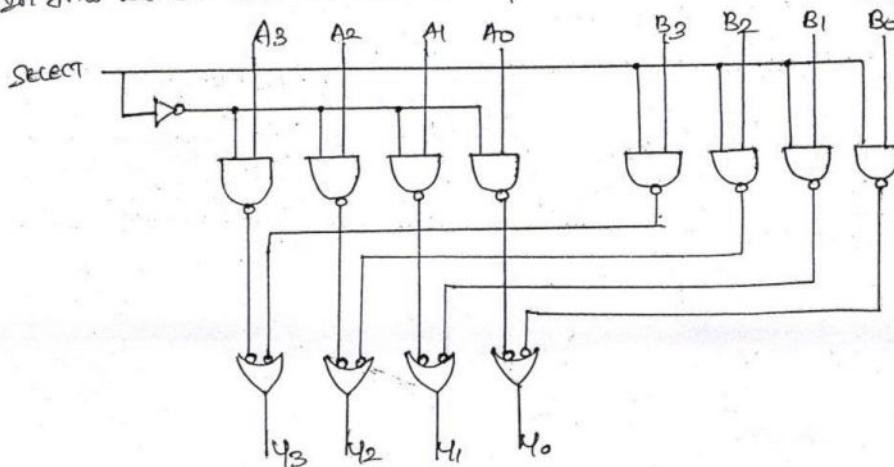
Universal logic Circuit:

Multiplexer Sometimes called Universal logic circuit

because 2ⁿ to 1 multiplexer can be used as a design solution for any n-variable Truth table.

125

⇒ Nibble Multiplexer: (Quad → 2 Input Multiplexer):
 Sometimes we may need to select one of the 2 inputs.
 In this we can use a nibble multiplexer.



→ The input nibble on left side is $A_3 A_2 A_1 A_0$, and right is $B_3 B_2 B_1 B_0$.

→ The control signal is labeled as SELECT. It determines which input nibble is transmitted to the output.

→ When SELECT is low, the four NAND gates on the left are activated. $\therefore Y_3 Y_2 Y_1 Y_0 = A_3 A_2 A_1 A_0$

When SELECT is high, the four NAND gates on the right are activated.

$$\therefore Y_3 Y_2 Y_1 Y_0 = B_3 B_2 B_1 B_0$$

IC 74157 is TTL nibble multiplexer

SELECT	1.	16	V _{CC}
A ₃	2	15	Strobe
B ₃	3	14	A ₀
Y ₃	4	13	B ₀
A ₂	5	12	Y ₀
B ₂	6	11	A ₁
Y ₂	7	10	B ₁
Gnd	8	9	Y ₁

Strobe must be low for
the activation of multiplexer



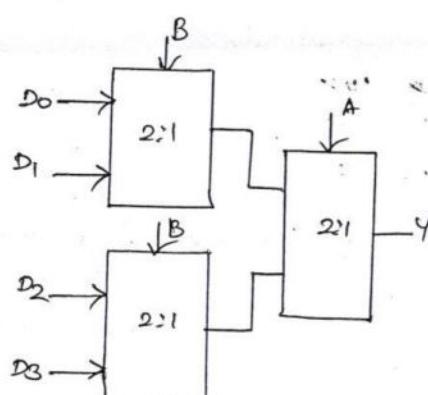
Q2 Show how a 4 to 1 multiplexer can be obtained using only 2:1 multiplexers. 126

Solution:

Logic equation for 2 to 1 mux $Y = \bar{A} \cdot D_0 + A \cdot D_1$

\therefore 4 to 1 mux $Y = \bar{AB} \cdot D_0 + \bar{AB}\bar{D}_1 + \bar{AD}_2 + A\bar{D}_3$

It can be rewritten as $Y = \bar{A}(\bar{B} \cdot D_0 + \bar{D}_1) + A(\bar{D}_2 + \bar{D}_3)$



\downarrow
2:1
 \downarrow
2:1

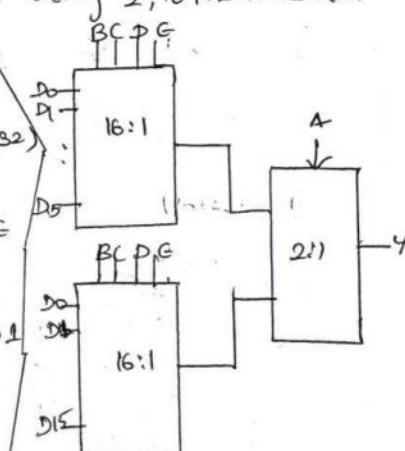
Q3 Design a 32 to 1 multiplexer using 2, 16 to 1 muxs and one 2 to 1 mux.

Solution

→ A 32 to 1 mux requires $(2^5 > 32)$
∴ Selection lines ABCDG

→ The lower 4 select lines BCDG
choose 16 to 1 MUX outputs.

→ The output of these 2, 16 to 1
MUX can be sent to third 2 to 1
MUX whose select line is A.



127

Q4 Implement the following Boolean function with an 8x1 multiplexer with A, B, D connected to selection lines S₂, S₁ & S₀ respectively.

$$F(A,B,C,D) = \sum(0,1,3,4,8,9,15)$$

Q8 $f(A, B, C, D) = \overline{ABD} + ACD + \overline{BCD} + \overline{A}\overline{C}D$ Implement Using 128
8:1 MUX
solution:



Q8. Implement the following using 8:1 MUX

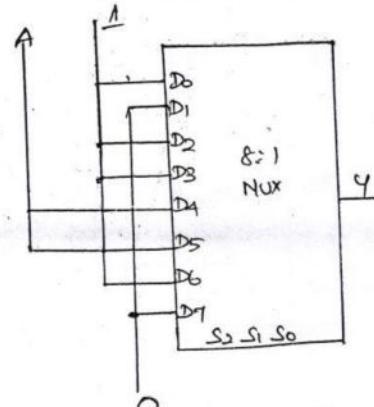
129

$$f(A, B, C, D) = \sum m(0, 2, 6, 10, 11, 12, 13) + \underline{d(3, 8, 14)}$$

Solution: Don't cares can be considered as 1 here.

	D0	D1	D2	D3	D4	D5	D6	D7
\bar{A}	①	②	③	1	5	⑥	7	
A	⑧	9	⑩	⑪	⑫	⑬	⑭	15
	1	0	1	1	1	1	0	

Multiplexer Implementation

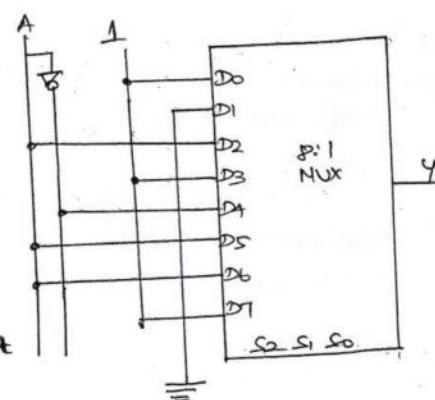


Q9. Implement the Boolean function expressed by POS if $f(A, B, C, D) = \prod (1, 2, 5, 6, 9, 12)$ Using 8 to 1 MUX.

Solution:

	D0	D1	D2	D3	D4	D5	D6	D7
\bar{A}	①	1	2	③	④	5	6	⑦
A	⑧	9	⑤	⑩	12	⑬	⑭	15
	1	0	1	1	1	1	1	1

MUX Implementation



Applications of Multiplexer:

- They are used as data selector to select one of many data inputs
- They can be used to implement combinational logic circuit.
- They are used in time multiplexing system
- Used in frequency Multiplexing System
- Used in A/D & D/A Converter
- Used in data acquisition systems.



Q10 Implement the following function using 4:1 MUX 180
 $f(A, B, C, D) = \sum m(0, 1, 2, 4, 6, 9, 12, 14)$

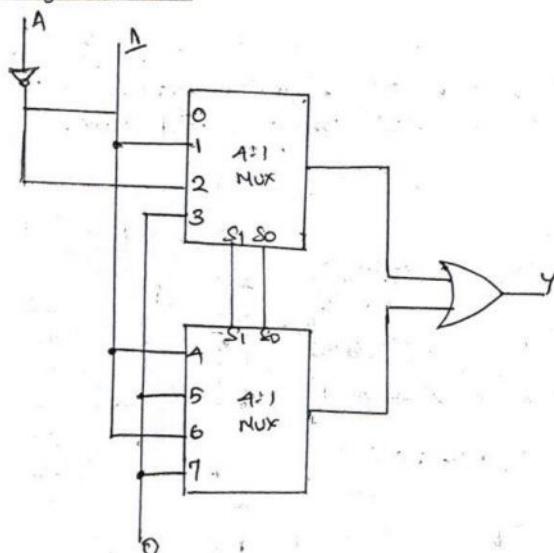
Solution

The function has four variables. To implement this function we require 8:1 multiplexer (i.e.) 2, 4:1 Multiplexers.

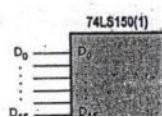
in Implementation Table :

	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
4	①	②	③	④	⑤	⑥	⑦	
A	8	⑨	10	11	⑫	13	⑭	15
	1	1	0	1	0	1	0	

(ii) Implementation Using two, 4:1 mux

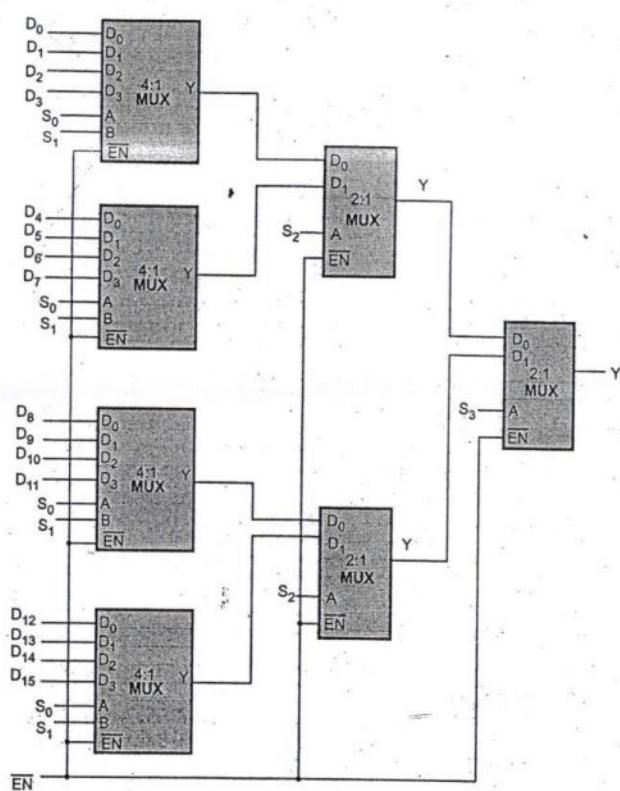


Q11 Construct 32 to 1 multiplexer Using 2 74LS150 ICs.



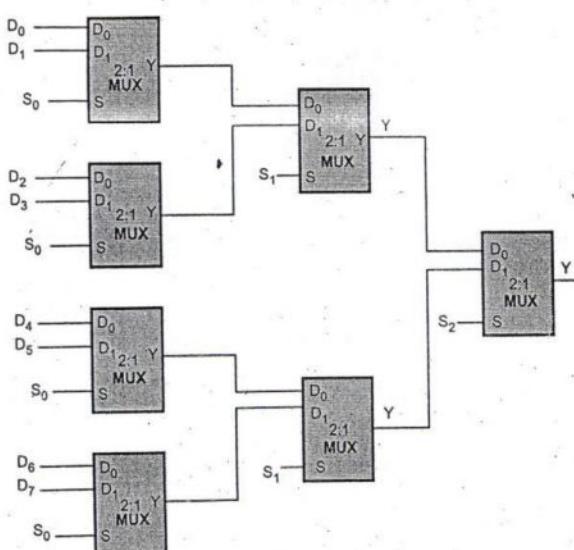
Q4 Construct 16:1 mux using 4:1 and 2:1 multiplexers 132

Solution



Q5 Construct 8:1 MUX using 2:1 multiplexers

Solution



DEMULTIPLEXERS :

A demultiplexer is a circuit that receives information on a single line and transmits this information on one of

133



Three State Buffers :-

18A

A three state (tri-state) device is a digital circuit that exhibits three states as below

1. logic 1
2. logic 0
3. High-impedance state

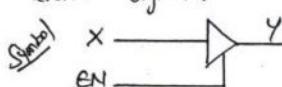
The high-impedance state means the output appears to be disconnected like an open circuit. In this state, the circuit has no logic significance. The three-state device has a control input that can place the gate into a high-impedance state. This represented by Z.

→ Types

There are 4 types of 3-state gates.

1. Bufif 1 :

This is a tri-state non-inverting buffer with active high enable signal.



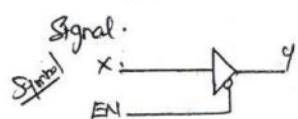
Truth Table

Inputs		Output
EN	X	Y
1	0	0
1	+	1
0	X	Z

There are 3 terminals for Bufif 1, input terminal X, Control input EN and output terminal Y. Bufif 1 gate behaves like a normal buffer if control input EN is 1. The output goes to a high-impedance state when EN is 0.

2. Bufif 0 :

This is a tri-state, non-inverting buffer with active low enable



T

Inputs		Output
EN	X	Y
0	0	0
0	1	1
1	X	Z

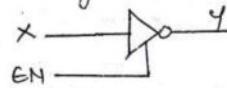
Bufif 0 gate behaves like a normal buffer if control input EN is 0. The output goes to a high-impedance state when EN is 1.



3. Notif 1 :

135

This is a tri-state inverting buffer with active high enable signal.

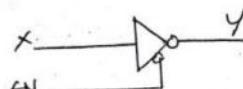


Inputs	Output
EN X	Y
1 0	1
1 1	0
0 X	Z

Notif 1 gate behaves like a normal inverter (NOT gate) if control input EN is 1. The output goes to a high impedance state when EN is 0.

4. Notif 0 :

This is a tri-state inverting buffer with active low enable signal

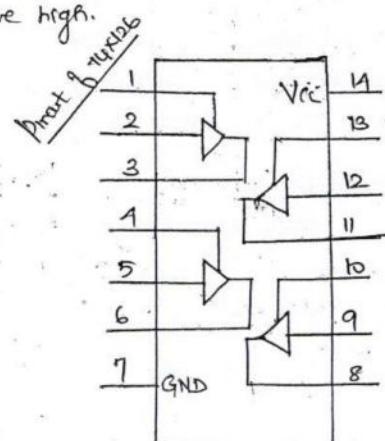
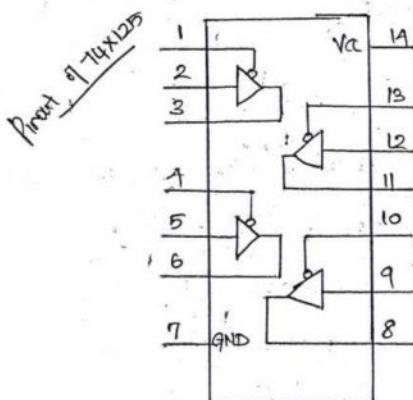


Inputs	Output
EN X	Y
0 0	1
0 1	0
1 X	Z

Notif 0 gate behaves like a normal inverter (NOT gate) if control input EN is 0. The output goes to a high-impedance state when EN is 1.

→ Tri-state Buffer ICs

The tri-state enable inputs in the 74X125 are active low and in the 74X126 are active high.



→ Integrated Circuit with Bi-directional Input-Output Pin

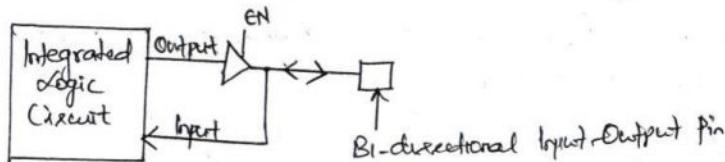
Integrated circuits are often designed using bi-directional pins for input and output. Bidirectional means that the



196

Same pin can be used as an input pin and as an output pin, but not both at the same time.

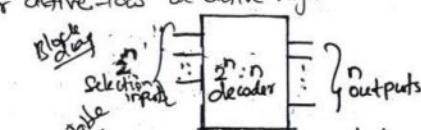
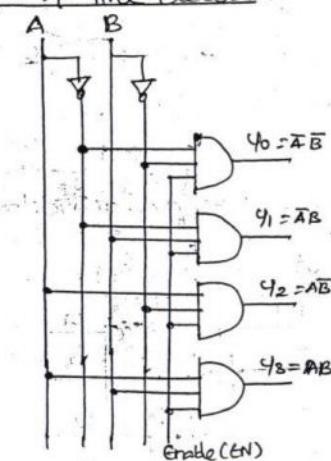
To accomplish this, the circuit output is connected to the pin through a three-state buffer. When the buffer is enabled, the pin is driven with the output signal. When the buffer is disabled, an external source can drive the input pin.



Decoder:

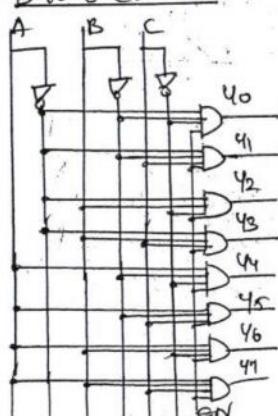
Decoder is identical to a demultiplexer without any data input. Its output can be either active-low or active-high

$\Rightarrow 2 \text{ to } 4$ line decoder:



Inputs			Outputs			
EN	A	B	Y ₃	Y ₂	Y ₁	Y ₀
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

$\Rightarrow 3 \text{ to } 8$ decoder:



Truth Table

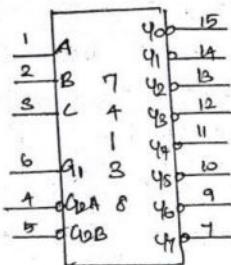
Inputs			Outputs							
EN	A	B	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀
0	X	X	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	1	0	0	0
1	1	0	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0
1	1	1	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0



⇒ 3 to 8 decoder IC 74138 :

137

Logic Symbol



74138 is a commercially available 3-to-8 decoder. It accepts three binary inputs (A, B, C) and when enabled, provides 8 individual active low outputs (Q_0-Q_7).
The device has 3 enable inputs.

→ 2 active low ($G_{2A} \& G_{2B}$)

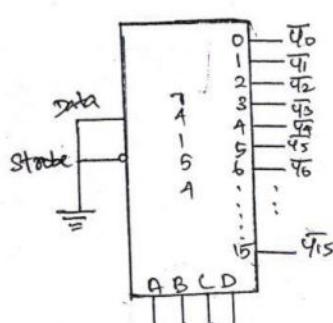
→ 1 active high (G_1)

Truth Table:

G_1 should be 1
 $G_{2A} + G_{2B} = 0$
to enable 74138.

Inputs				Outputs							
G_{2B}	G_{2A}	G_1	$C\bar{B}\bar{A}$	\bar{Q}_7	\bar{Q}_6	\bar{Q}_5	\bar{Q}_4	\bar{Q}_3	\bar{Q}_2	\bar{Q}_1	\bar{Q}_0
1	X	X	xxx	1	1	1	1	1	1	1	1
X	1	X	xx	1	1	1	1	1	1	1	1
X	X	0	xxx	1	1	1	1	1	1	1	0
0	0	1	000	1	1	1	1	1	1	1	0
0	0	1	001	1	1	1	1	1	1	1	0
0	0	1	010	1	1	1	1	1	1	0	1
0	0	1	011	1	1	1	1	1	1	0	1
0	0	1	100	1	1	1	1	0	1	1	1
0	0	1	101	1	1	1	0	1	1	1	1
0	0	1	110	1	0	1	1	1	1	1	1
0	0	1	111	0	1	1	1	1	1	1	1

⇒ 1 to 16 Decoder



The 74154 is called decoder-demultiplexer because it can be used either as decoder or demultiplexer.

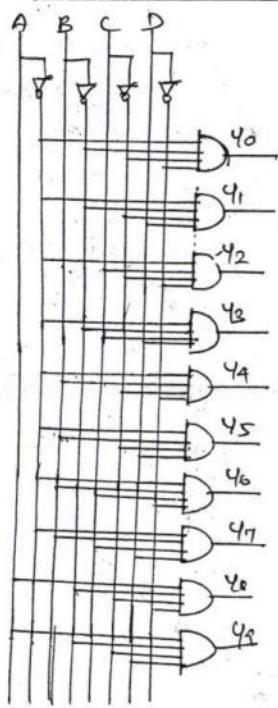
To use 74154 as decoder we should ground DATA & STORE inputs.

The output line is low, when it is active. If binary input is $ABCD = 0111$. Then the Q_7 is low, while all other outputs are high.



⇒ BCD to Decimal Decoder: (A to 10) decoder:

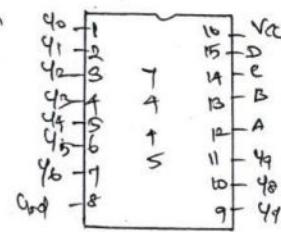
188



This circuit is called 1 of 10 decoder bcos only 1 of the 10 output line is high for instance when ABCD = 0011, only the 4s AND gate has all high outputs.

It is also called BCD to Decimal decoder. Because in all the ABCD possibilities, we can find that the subscript of the high output always equals the decimal equivalent of the BCD to Decimal converter.

Analog diagram



Y₀ to Y₉ are active low

Pins: It provides complementary output.

* The 7445 / 7442 :

Instead of building a BCD to decimal decoder with separate inverters and AND gate, we can use 7445 / 7442 ICs

Practical

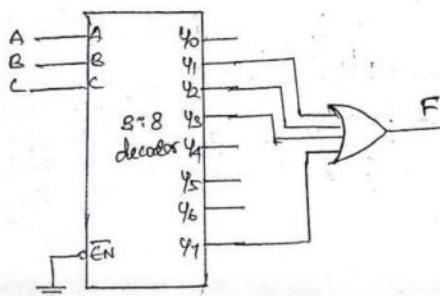
Inputs	Outputs													
	A	B	C	D	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇	Y ₈	Y ₉
0 0 0 0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0 0 0 1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0 0 1 0	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0 0 1 1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0 1 0 0	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0 1 0 1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
0 1 1 0	1	1	1	1	1	1	0	1	1	1	1	1	1	1
0 1 1 1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
1 0 0 0	1	1	1	1	1	1	1	1	0	1	1	1	0	1
1 0 0 1	1	1	1	1	1	1	1	1	1	0	1	1	1	0
1 0 1 0	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1 0 1 1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1 1 0 0	1	1	1	1	1	1	1	1	1	1	1	1	1	0
1 1 0 1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
1 1 1 0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1 1 1 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

139

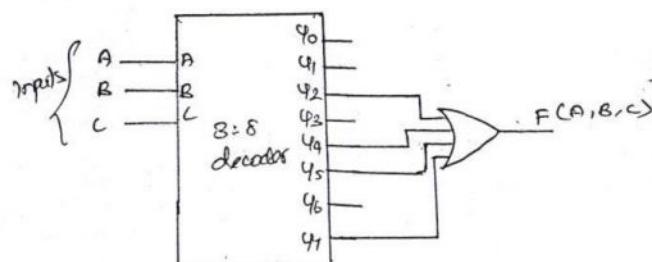
Implement the following functions using 8:8 decoder and external gates.

Q1 $F = \Sigma m(1, 2, 3, 7)$

Solution :-



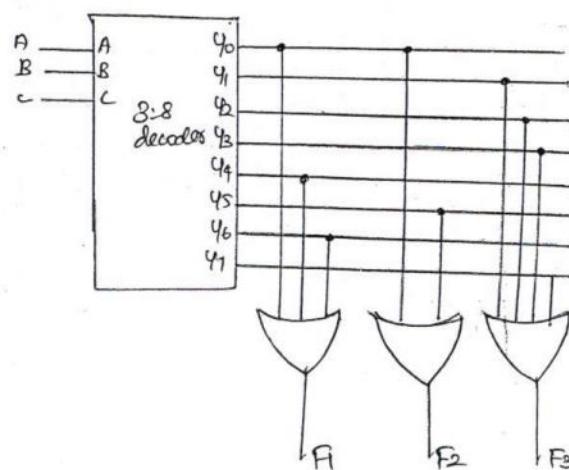
Q2 $F(A, B, C) = \Sigma m(2, 4, 5, 7)$



Q3 $F_1(A, B, C) = \Sigma m(0, 1, 6); F_2(A, B, C) = \Sigma m(0, 5); F_3(A, B, C) = \Sigma m(1, 2, 3, 7)$

Solution

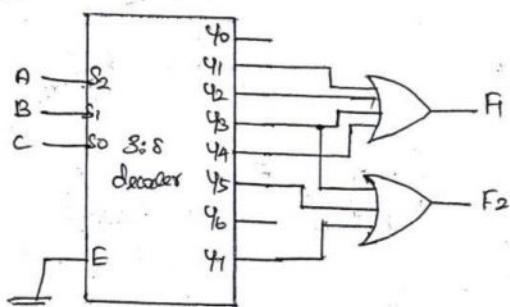
To get the required Boolean functions





Q4. $F_1(A, B, C) = \sum m(1, 2, 3, 4); F_2(A, B, C) = \sum m(3, 5, 7)$ 10

Solution



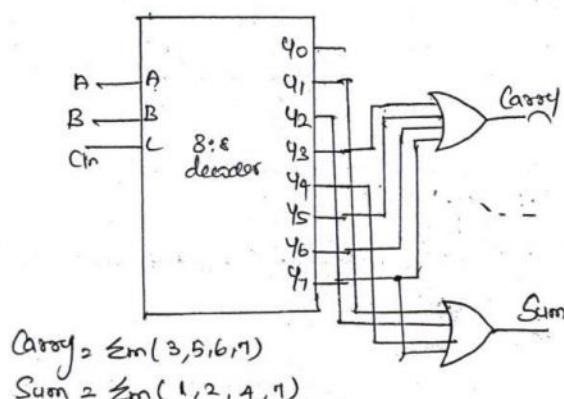
Q5 Implement a full adder using a 3-to-8 decoder.

Solution

* Step 1: Truth Table

Inputs	Outputs
A B Cin	Carry Sum
0 0 0	0 0
1 0 0	0 1
0 1 0	0 1
0 1 1	1 0
1 0 0	0 1
1 0 1	1 0
1 1 0	1 0
1 1 1	1 1

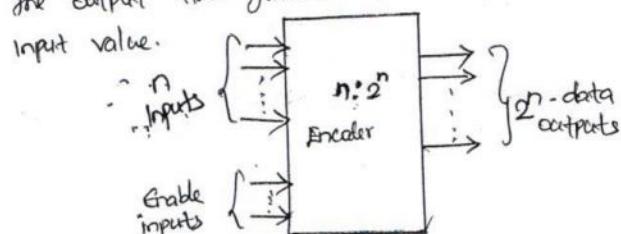
Step 2: Decoder Implementation



ENCODERS:-

An encoder is a digital circuit that performs the inverse operation of a decoder.

An encoder has 2^n input lines and n output lines. In encoder the output lines generate the binary code corresponding to the input value.





⇒ Decimal to BCD Encoder

141

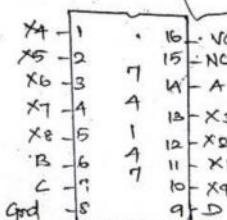
The decimal to BCD encoder usually has 10 input lines and 4 output lines. The decoded decimal data acts as an input for encoder and decoded BCD output is available on the 4 output lines.

* The 74141:

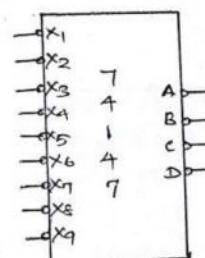
The 74141 is also called priority encoder. Because it gives priority to highest order input.

It has 9 input lines and 4 output lines. Both input and output lines are asserted active low.

Pin diagram
of 74141



Logic diagram
of 74141



→ NC - No connection
→ Active low ips & op's

It is important to note that there is no input line for decimal zero. When this condition occurs, all output lines are 1.

Truth table:

Priority encoder
 $x_2=0, x_1=0$ or 1
if $x_0=0 \& x_1=0$
the priority goes to
higher order.
i.e. x_0 will be
selected.

Decimal value	Inputs								Outputs				
	x_1	x_2	x_3	x_4	x_5	x_6	x_7	x_8	x_9	A	B	C	D
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	0
2	x	0	1	1	1	1	1	1	1	1	1	0	1
3	x	x	0	1	1	1	1	1	1	1	1	0	0
4	x	x	x	0	1	1	1	1	1	1	0	1	1
5	x	x	x	x	0	1	1	1	1	1	0	1	0
6	x	x	x	x	x	0	1	1	1	1	0	0	1
7	x	x	x	x	x	x	0	1	1	1	0	0	0
8	x	x	x	x	x	x	x	0	1	0	1	1	1
9	x	x	x	x	x	x	x	x	0	0	1	1	0

→ when all x inputs are high, all outputs are high. 142

→ when x_9 is low, the ABCD output is 0110 (equivalent to 9 if its complemented $\Rightarrow 1001$).

⇒ Octal-to-Binary Encoders:-

143

It has 8 inputs, one for each octal digits and 3 output that converts the corresponding binary code. In



When a digital system is designed using a PLD, changes in the design can easily be made by changing the programming of the PLD without having to change the wiring in the system. 144

PROGRAMMABLE LOGIC ARRAY:

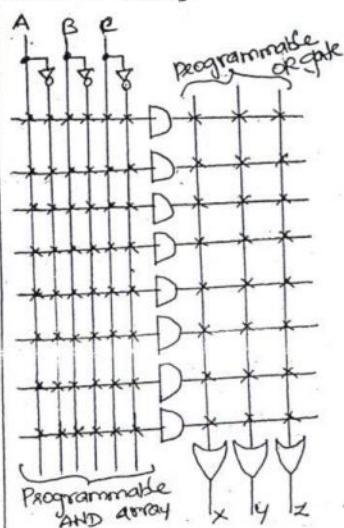
PLA is another design solution to implement sum of product equations. It consists of Programmable AND array followed by Programmable OR array.

Programmable AND array is used to implement product terms and these product terms are decoded by Programmable OR array. The Y_p signals are presented to an array of AND gates, while the O/Ps are taken from an array of OR gates.

PLAs, along with ROMs and PALs are included in the classification of ICs called Programmable logic devices (PLDs).

In PLA, the input AND gate array and OR gate array are feasible linked and programmable. It is also more complicated to utilize since the number of feasible links is doubled.

A PLA having 3 input variables (A,B,C) & 3 O/P variables (X,Y,Z).



Eight AND gates are required to decode the 8 possible Y_p states.

In this case, there are 3 OR gates that can be used to generate logic functions at the output.

There could be additional OR gates at the O/P if required.

Q Implement the following function using PLA:-

$$X = \overline{ABC} + AB\overline{C} + BC ; Y = \overline{ABC} + A\overline{B}\overline{C} ; Z = \overline{BC}$$

Solution:

145

7-Segment decoder using PLA:

Suppose it is desired to use a PLA to recognize each of the 10 decimal digits represented in binary form.

146

Q4.

147
A combinational circuit is defined by the functions
 $F_1(A,B,C) = \Sigma m(3,5,7)$, $F_2(A,B,C) = \Sigma m(4,5,7)$. Implement the
functions using minimum number of product terms and

* The first column gives the list of Product terms numerically.

140

Step 1: K-map Simplification:

f1				
$\bar{b}\bar{c}$	$\bar{b}c$	$b\bar{c}$		
\bar{a}	1 1 1 0	1 1 0 0	0 0 0 0	
a	1 0 0 0	0 0 0 0	0 0 0 0	

$$f_1 = \bar{b}\bar{c} + \bar{a}c$$

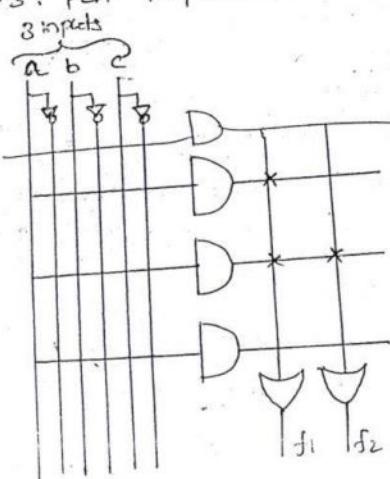
f2				
$\bar{b}\bar{c}$	$\bar{b}c$	$b\bar{c}$		
\bar{a}	0 1 1 1	1 0 0 0	1 1 1 1	
a	1 1 0 0	0 0 0 0	0 0 0 0	

$$f_2 = \bar{a}\bar{b} + \bar{b}c + \bar{a}b$$

Step 2: PLA Palabram Table

Product terms	Inputs			Outputs	
	a	b	c	f1	f2
$\bar{b}\bar{c}$	-	0	0	1	-
$\bar{a}c$	0	-	1	1	1
$a\bar{b}$	1	0	-	-	1
$\bar{a}b$	0	1	-	-	1

Step 3: PLA Implementation



Implement the following function Using PLA.

$$A(x, y, z) = \sum m(1, 2, 4, 6)$$

$$B(x, y, z) = \sum m(0, 1, 6, 7)$$

$$C(x, y, z) = \sum m(2, 6)$$

Step 1: K-map Simplification.

X	Y	Z	A	B	C
0	0	0	0	1	0
0	0	1	1	1	0
0	1	0	1	0	1
0	1	1	0	0	0
1	0	0	1	0	0
1	0	1	0	0	0
1	1	0	1	1	1
1	1	1	0	1	0

150

For A

+ M ₂		
X	$\bar{y}\bar{z}$	$\bar{y}z$
\bar{x}	0 (1) 0	0 (1)
x	1 0 0	0 1

$$A = \bar{x}\bar{y}z + x\bar{z} + y\bar{z}$$

For B

$\bar{y}\bar{z}$ $\bar{y}z$ $y\bar{z}$ yz		
X	$\bar{y}\bar{z}$	$\bar{y}z$
\bar{x}	0 (1) 0	0 0
x	0 0 1	0 1

$$B = \bar{x}\bar{y} + xy$$

For C

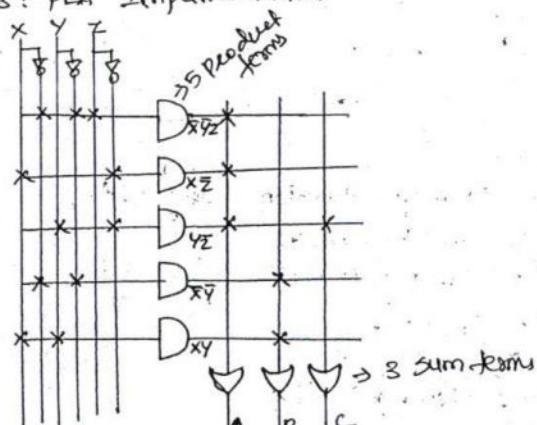
$\bar{y}\bar{z}$ $\bar{y}z$ $y\bar{z}$ yz		
X	$\bar{y}\bar{z}$	$\bar{y}z$
\bar{x}	0 0 0	0 1
x	0 0 0	0 1

$$C = y\bar{z}$$

Step 2 : PLA program table.

Product term	Inputs			Outputs		
	X	Y	Z	A	B	C
$\bar{x}\bar{y}z$	0	0	1	1	-	-
$x\bar{z}$	1	-	0	1	-	-
$\bar{y}z$	-	1	0	1	-	1
$\bar{x}y$	0	0	-	-	1	-
xy	1	1	-	-	1	-

Step 3 : PLA Implementation





Q8 Design a BCD to excess-3 code converter and
Implement using suitable PLA. 151

Solution:

Step 1: Truth table.

Decimal	BCD				Excess-3 code			
	B ₃	B ₂	B ₁	B ₀	E ₃	E ₂	E ₁	E ₀
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Step 2: K-map Simplification

		For E ₃			
		B ₃ B ₂	B ₃ B ₂	B ₂ B ₁	B ₂ B ₁
E ₃	B ₃ B ₂	0	0	0	0
E ₃	B ₃ B ₂	0	1	1	1
E ₃	B ₂ B ₁	X	X	X	X
E ₃	B ₂ B ₁	1	1	X	X

$$E_3 = B_3 + B_2B_0 + B_2B_1$$

		For E ₂			
		B ₃ B ₂	B ₃ B ₂	B ₂ B ₁	B ₂ B ₁
E ₂	B ₃ B ₂	0	1	1	1
E ₂	B ₃ B ₂	1	0	0	0
E ₂	B ₂ B ₁	(X)	X	X	X
E ₂	B ₂ B ₁	0	1	(X)	X

$$E_2 = B_2 \bar{B}_1 \bar{B}_0 + \bar{B}_2 B_0 + B_2 B_1$$

		For G ₁			
		B ₃ B ₂	B ₃ B ₂	B ₂ B ₁	B ₂ B ₁
G ₁	B ₃ B ₂	1	0	1	0
G ₁	B ₃ B ₂	1	0	1	0
G ₁	B ₂ B ₁	(X)	X	X	X
G ₁	B ₂ B ₁	1	0	(X)	X

$$G_1 = \bar{B}_1 B_0 + B_1 B_0$$

		For E ₀			
		B ₃ B ₂	B ₃ B ₂	B ₂ B ₁	B ₂ B ₁
E ₀	B ₃ B ₂	1	0	0	1
E ₀	B ₃ B ₂	1	0	0	1
E ₀	B ₂ B ₁	(X)	X	X	X
E ₀	B ₂ B ₁	1	0	X	X

$$E_0 = \overline{B_0 B_1 B_2 B_3}$$

$$E_0 = \overline{B_0}$$

Step 3: PLA program Table:-

Product	Inputs	Outputs
---------	--------	---------

Q1 What are the different types of PLDs and implement the 7-segment decoder using PLA.

Solution:

PLDs are classified as

1. PROMs \rightarrow Programmable Read Only Memories
2. PLAs \rightarrow Programmable Logic Arrays
3. PAL \rightarrow Programmable Array logic
4. FPGA \rightarrow Field Programmable Logic Devices
5. CPLDs \rightarrow Complex Programmable Logic Devices

\rightarrow 7 segment decoder using PLA

Step 1:

Truth Table

Digit	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

Step 2: K-map Simplification:-

		For a				
		CD	00	01	11	10
AB	00	1	0	1	1	
		01	0	1	1	1
AB	11	X	X	X	X	
		10	1	1	X	X

$$a = A + C + BD + \overline{BD}$$

		For b				
		CD	00	01	11	10
AB	00	1	1	1	1	
		01	1	0	1	0
AB	11	X	X	X	X	
		10	1	1	X	X

$$b = \overline{B} + \overline{C}\overline{D} + CD$$

		For c				
		CD	00	01	11	10
AB	00	1	(1)	1	0	
		01	1	1	1	1
AB	11	X	X	X	X	
		10	1	1	X	X

$$c = B + \overline{C} + D$$



(152)

		For d				For e				For f									
		AB	CD	00	01	11	10	AB	CD	00	01	11	10	AB	CD	00	01	11	10
00		1	0	1	1			00	1	0	0	1			00	1	0	0	0
01		0	1	0	1			01	0	0	0	1			01	1	1	0	1
11	X	X	X	X	X			11	X	X	X	X			11	X	X	X	X
10	1	1	X	X	X			10	0	X	X	X			10	1	1	X	X

$d = \overline{B}\overline{D} + C\overline{D} + B\overline{C}D + \overline{B}C + A$

$e = \overline{B}\overline{D} + CD$

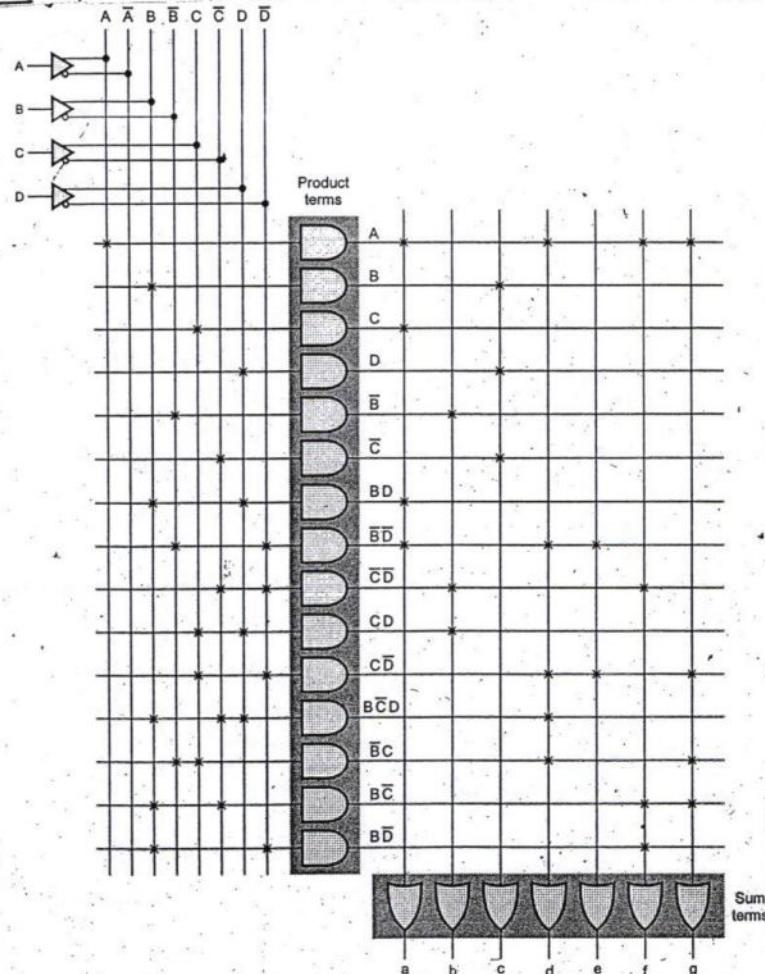
$f = A + \overline{C}\overline{D} + B\overline{C} + B\overline{D}$

For g

		AB	CD	00	01	11	10
00		0	0	1	1		
01		1	1	0	1		
11	X	X	X	X	X		
10	1	1	X	X	X		

$g = A + B\overline{C} + \overline{B}C + CD$

Step 2 : PLA Implementation



Q10: Implement the following Boolean function using an appropriate PLA. (153)

$$F_1(A+B, C) = \sum m(0, 1, 2), F_2(A, B, C) = \sum m(1, 6)$$



(1)

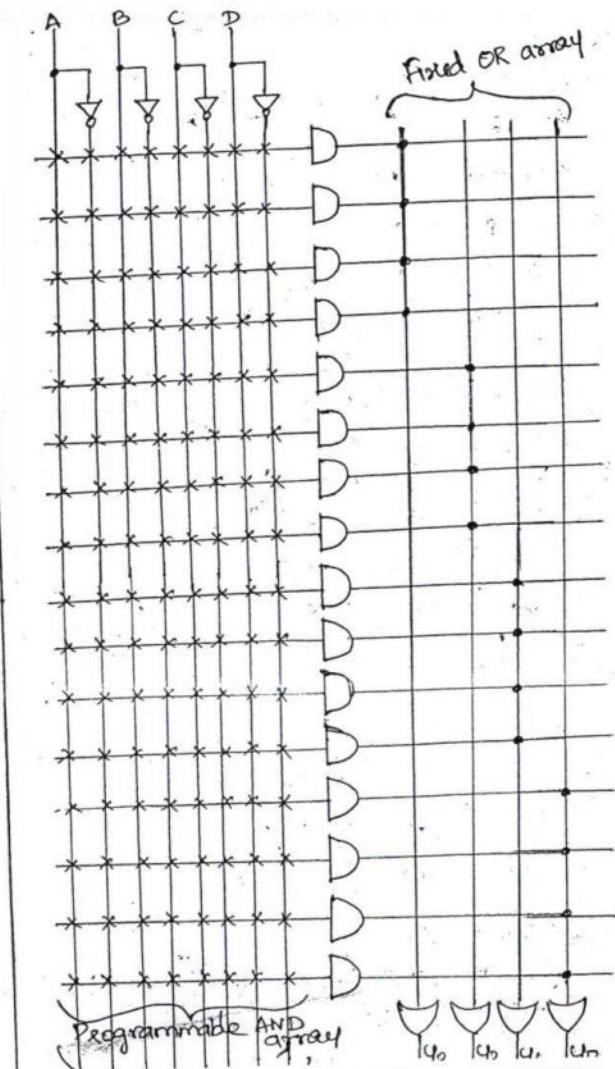
15A

PROGRAMMABLE ARRAY LOGIC

Programmable Array Logic (PAL) is a programmable array of logic gates on a single chip. PALs are another design solution, similar to a sum-of-products solution, product-of-sums solution and multiplexer logic.

⇒ Programming of PAL

A PAL is different from a PROM because it has a Programmable AND array and a fixed OR array.



155

This PAL has 4 inputs and 4 outputs. The X's on the input side are fusible links while the solid black bulletts on the output side are fixed connections.

With a PROM programmer, we can burn in the desired fundamental products, which are then ORed by the fixed output connections.

Q1

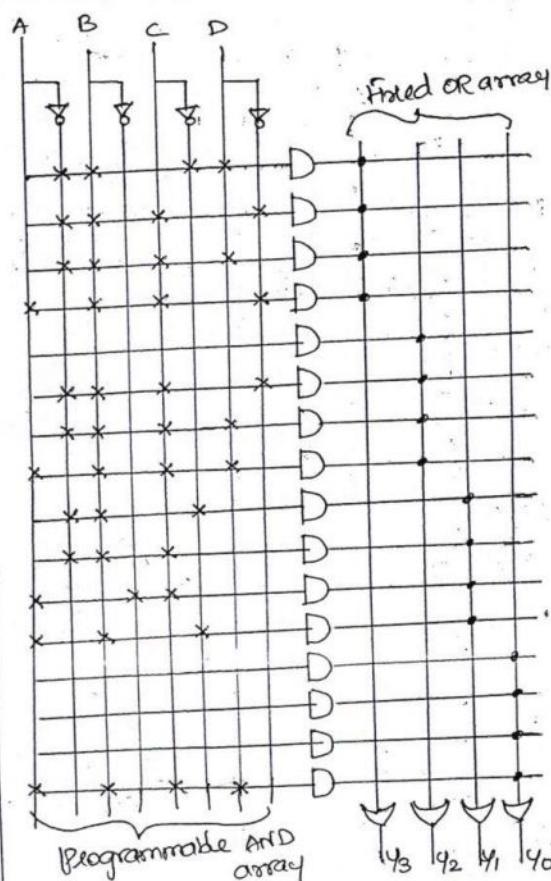
$$Y_0 = AB CD$$

$$Y_1 = \bar{A} \bar{B} \bar{C} + \bar{A} BC + A \bar{B} C + ABC$$

$$Y_2 = \bar{A} \bar{B} \bar{C} \bar{D} + \bar{A} B \bar{C} D + A B \bar{C} D$$

$$Y_3 = \bar{A} \bar{B} \bar{C} \bar{D} + \bar{A} B \bar{C} \bar{D} + \bar{A} B C \bar{D} + A B C \bar{D}$$

For these Boolean functions, How to Program a PAL ?



⇒ Commercially Available PALs:

Commercially available PALs typically have more pins. Here are sample of some TTL PALs available from National Semiconductor Corporation.

10H8 ; 10 input and 8 output AND-OR
16H2 ; 6 input and 2 output AND-OR
1AL4 ; 14 input and 4 output AND-OR-INVERT

Here, 'H' stands for active-high output
'L' " active-low "

- ✓ 10H8, 16H2 Produce active high outputs bcoz they are AND-OR PALs.
- ✓ 1AL4 Produce an active low o/p bcoz its an AND-OR-INVERT ckt.

Q2 Implement the following Boolean functions using PAL.

$$(i) W(A,B,C,D) = \sum m(0,2,6,7,8,9,12,13)$$

$$(ii) X(A,B,C,D) = \sum m(0,2,6,7,8,9,12,13,14)$$

$$(iii) Y(A,B,C,D) = \sum m(2,3,8,9,10,12,13)$$

$$(iv) Z(A,B,C,D) = \sum m(1,3,4,6,9,12,14)$$

Soln:

Let us simplify the four functions for minimum number of terms.

Step 1: K-map Simplification

For W

AB	CD	CD	CD	CD
$\bar{A}\bar{B}$	1	0	0	C
$\bar{A}B$	0	0	1	1
$A\bar{B}$	1	1	0	0
AB	1	1	0	0

$$W =$$

$$W = \bar{A}\bar{B}\bar{D} + \bar{A}BC + AC$$

For X

AB	CD	CD	CD	CD
$\bar{A}\bar{B}$	1	0	0	C
$\bar{A}B$	0	0	1	1
$A\bar{B}$	1	1	0	1
AB	1	1	0	0

$$X =$$

$$X = \bar{A}\bar{B}\bar{D} + \bar{A}BC + A\bar{C} + BCD$$

157

For 4

0	0	0
0	0	0
1	1	0
1	1	0
		1

$$Y = \bar{A}\bar{B}C + \bar{B}CD + AC$$

2nd for 3

0	<u>D</u>	<u>D</u>	0
1	0	6	1
1	0	0	1
0	1	0	

$$Z = \bar{A}\bar{B}D + \bar{B}\bar{C}D + B\bar{D}$$

Step 2: Programming a PAL.

