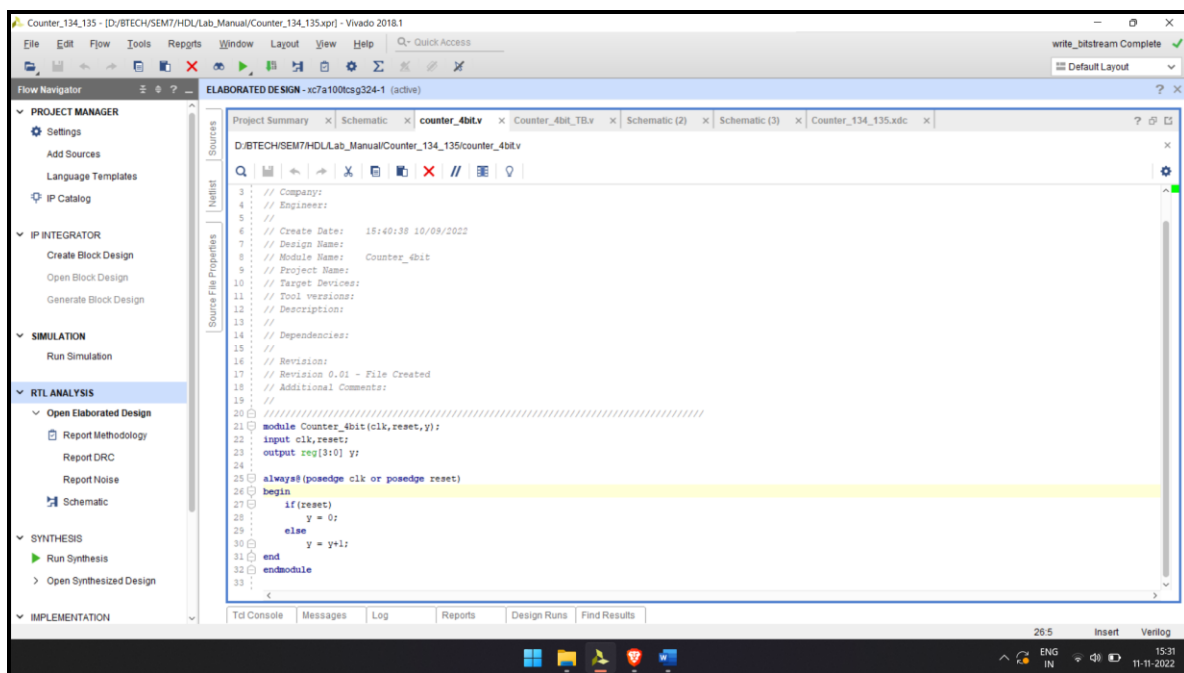
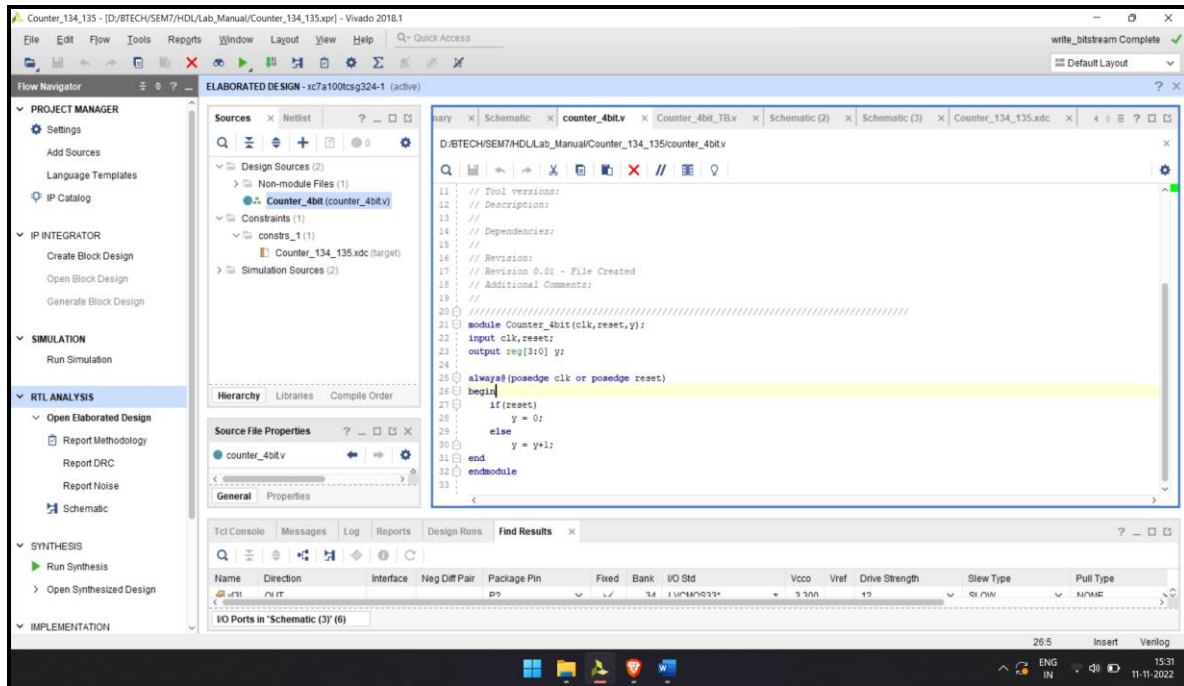
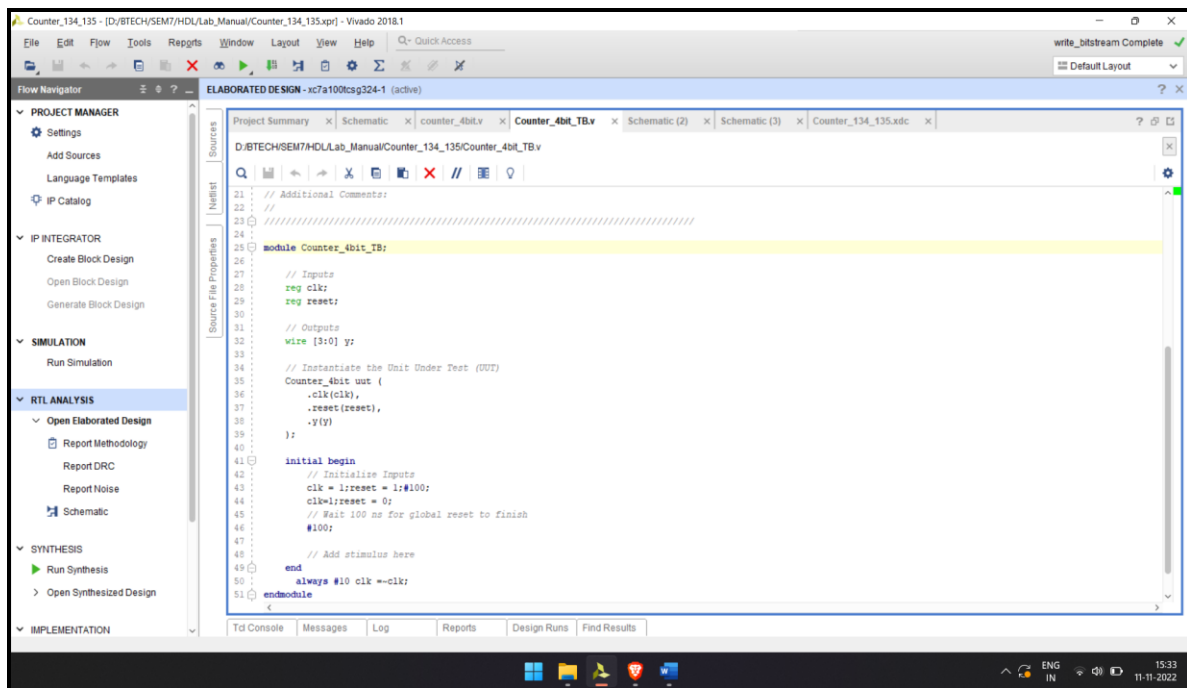


COUNTER

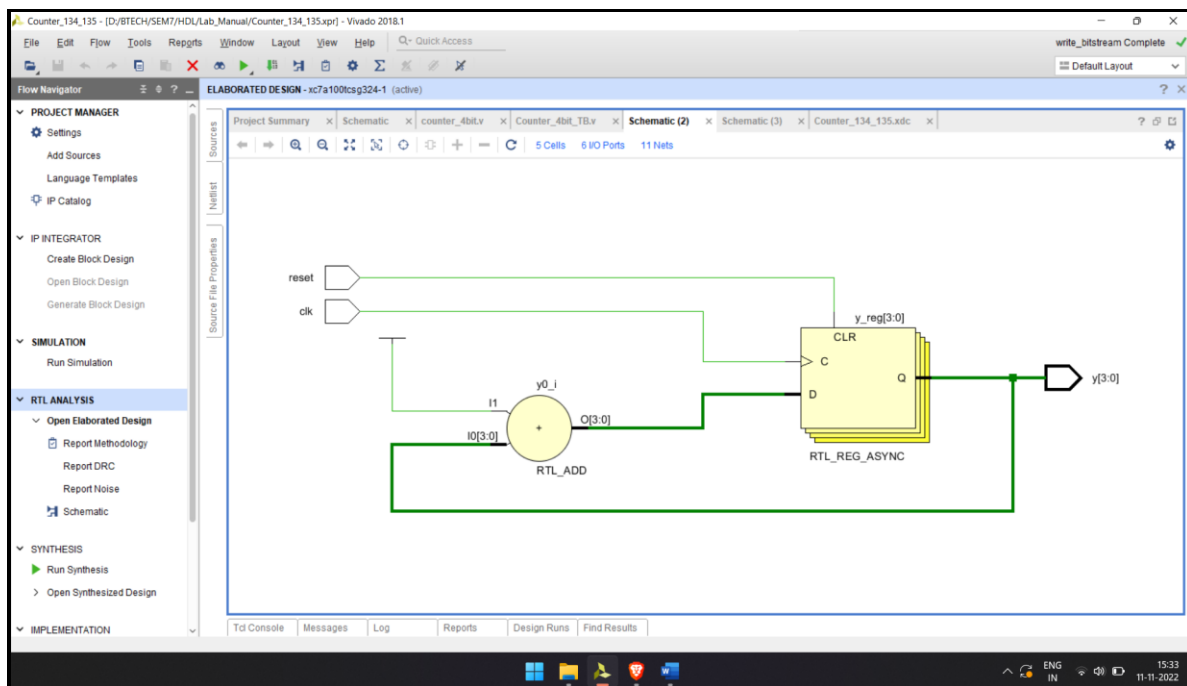
Verilog Code:



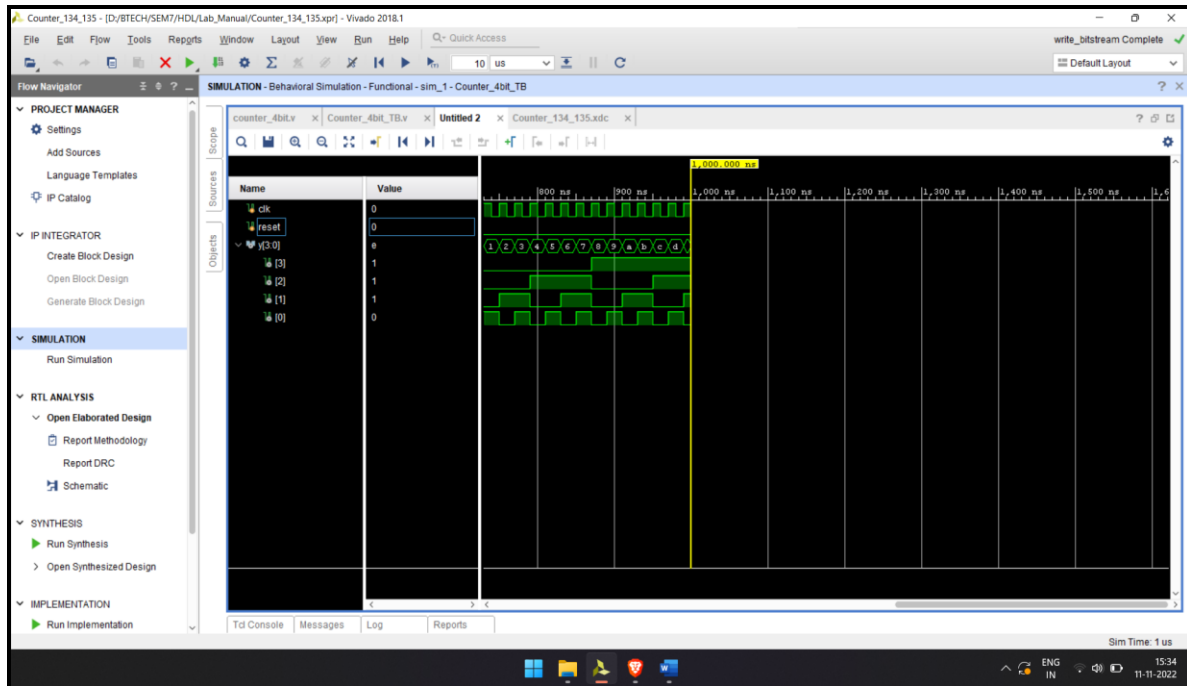
TestBench:



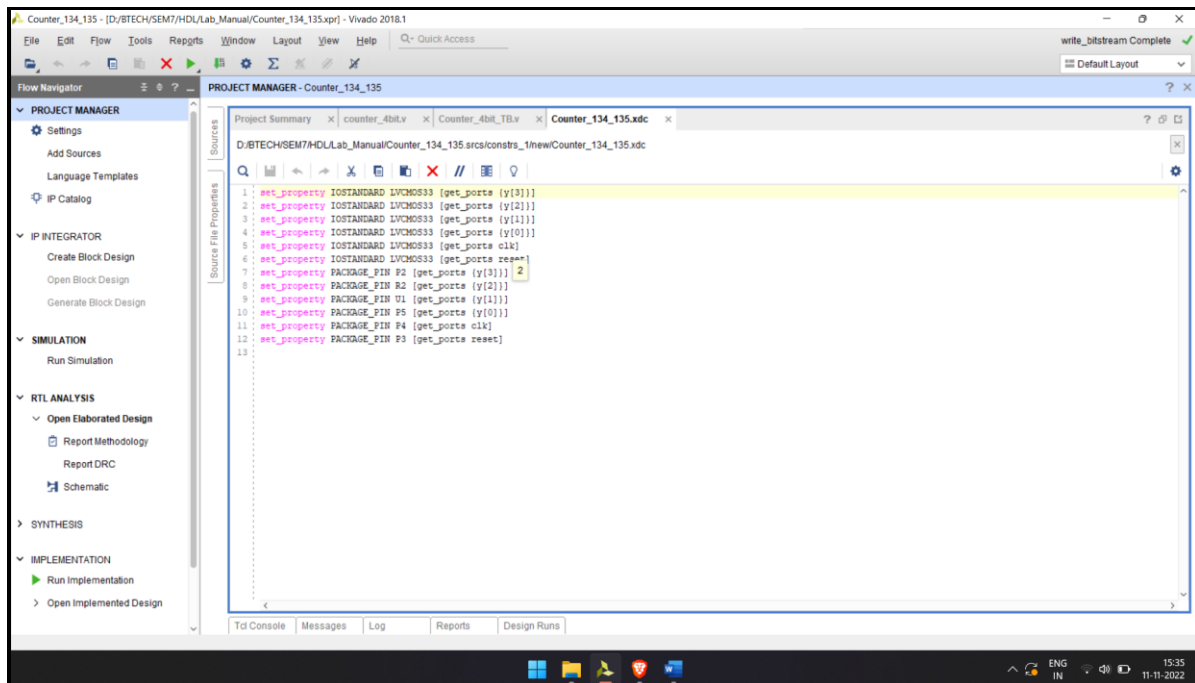
RTL Schematic:



Simulation:



XDC file:



Design Summary:

The screenshot shows the Vivado 2018.1 Project Manager window for the project 'Counter_134_135'. The 'Project Summary' tab is active, displaying the following information:

- Settings:**
 - Project name: Counter_134_135
 - Project location: D:/BTECH/SEM7/HDL/Lab_Manual/Counter_134_135.xpr
 - Product family: Artix-7
 - Project part: xc7a100tcsq324-1
 - Top module name: Counter_4bit
 - Target language: Verilog
 - Simulator language: Mixed
- Synthesis:**
 - Status: Complete
 - Messages: No errors or warnings
 - Part: xc7a100tcsq324-1
 - Strategy: Vivado Synthesis Defaults
 - Report Strategy: Vivado Synthesis Default Reports
- Implementation:**
 - Status: Complete
 - Messages: 3 warnings
 - Part: xc7a100tcsq324-1
 - Strategy: Vivado Implementation Defaults
 - Report Strategy: Vivado Implementation Default Reports
 - Incremental compile: None
- DRC Violations:**
 - Summary: 1 warning
 - Implemented DRC Report
- Timing:**
 - Worst Negative Slack (WNS): NA
 - Total Negative Slack (TNS): NA
 - Number of Failing Endpoints: NA
 - Total Number of Endpoints: NA
 - Implemented Timing Report

The bottom status bar shows the date and time as 11-11-2022 15:35.

Hardware Complete:

The screenshot shows the Vivado 2018.1 Hardware Manager window for the project 'Counter_134_135'. The 'Hardware' tab is active, displaying the following information:

- Hardware:**
 - Name: xc7a100t_0 (1)
 - Status: Connected
 - Programmer: XADC (System Monitor)
- Hardware Device Properties:**
 - Name: xc7a100t_0
 - Part: xc7a100t
- Reports:**
 - Report: impl_1_place_report_utilization_0
 - Report Type: Report on utilization of resources on the targeted device (report_utilization)
 - Options: str = false; pacitru = false; hierarchical = false

The bottom status bar shows the date and time as 11-11-2022 16:09.