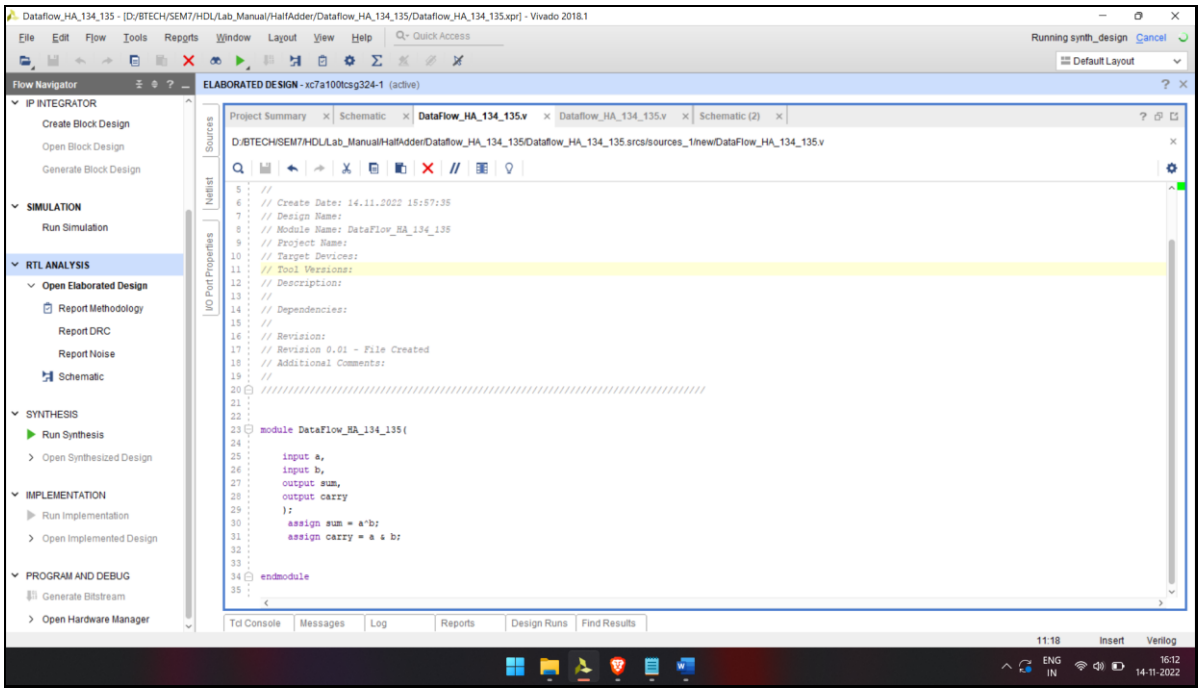
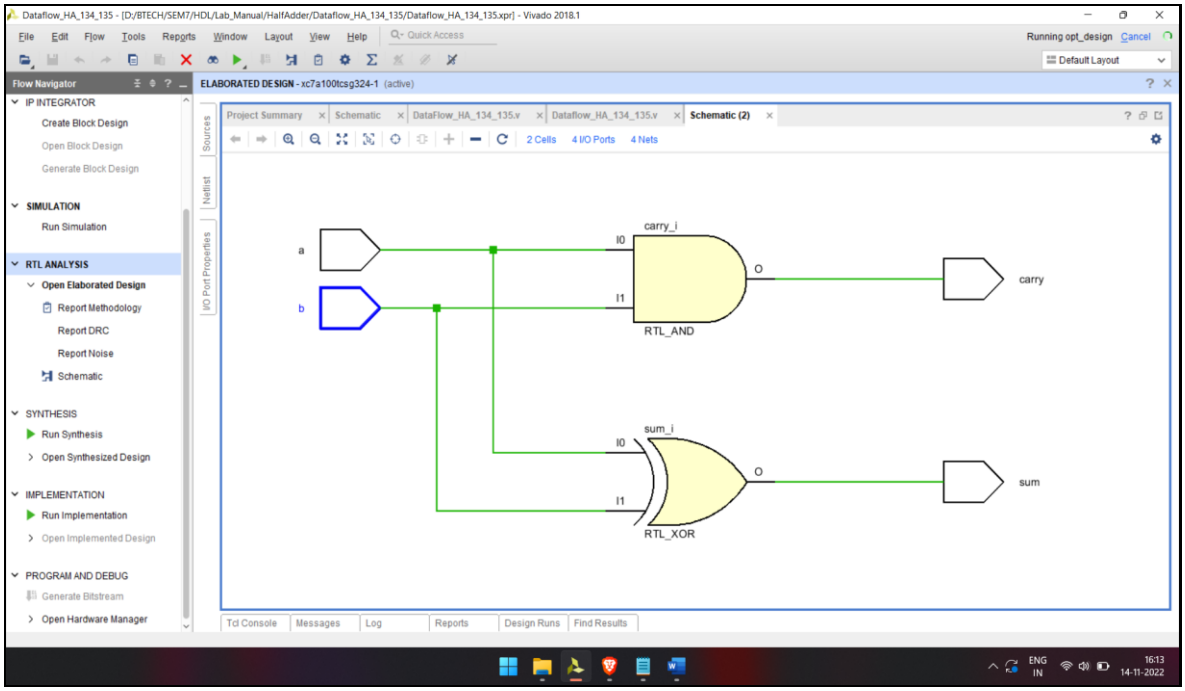
HALF ADDER- DATAFLOW MODEL

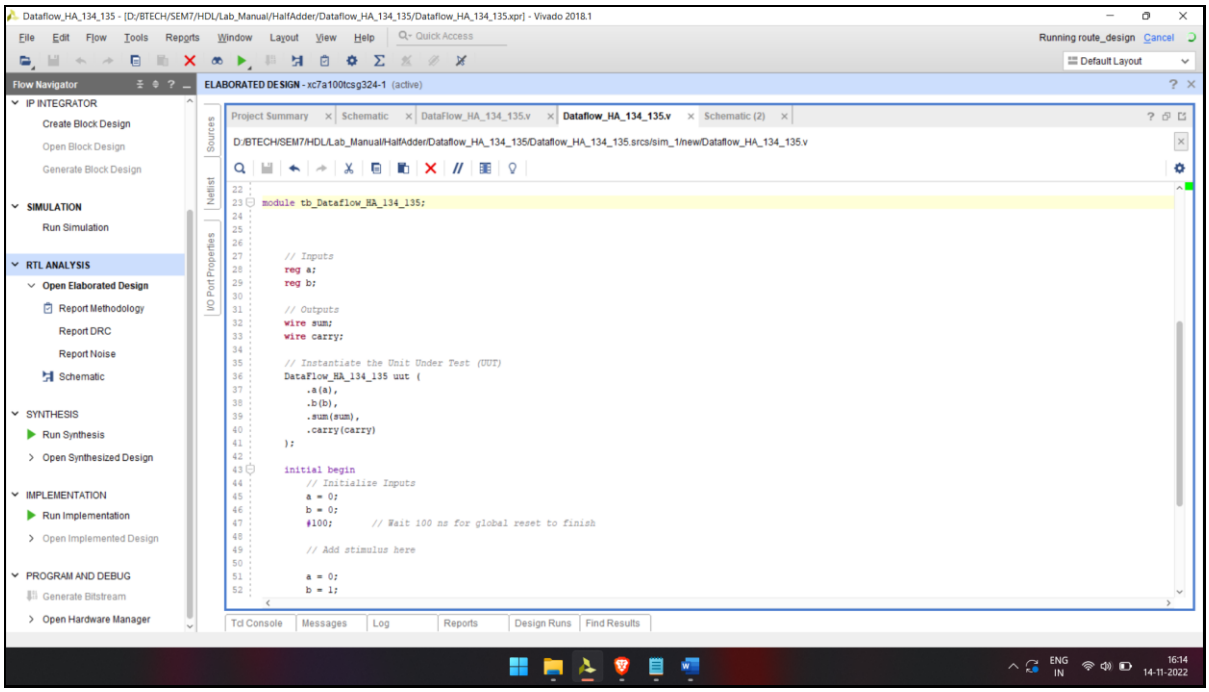
Verilog Code:



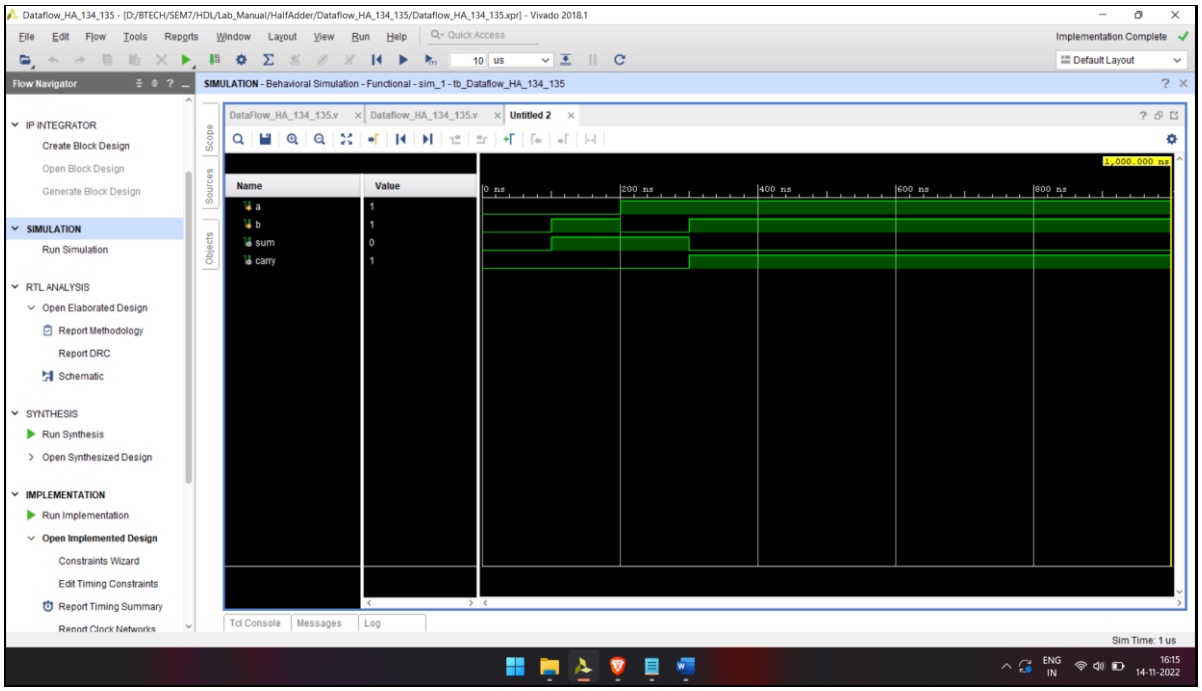
RTL :



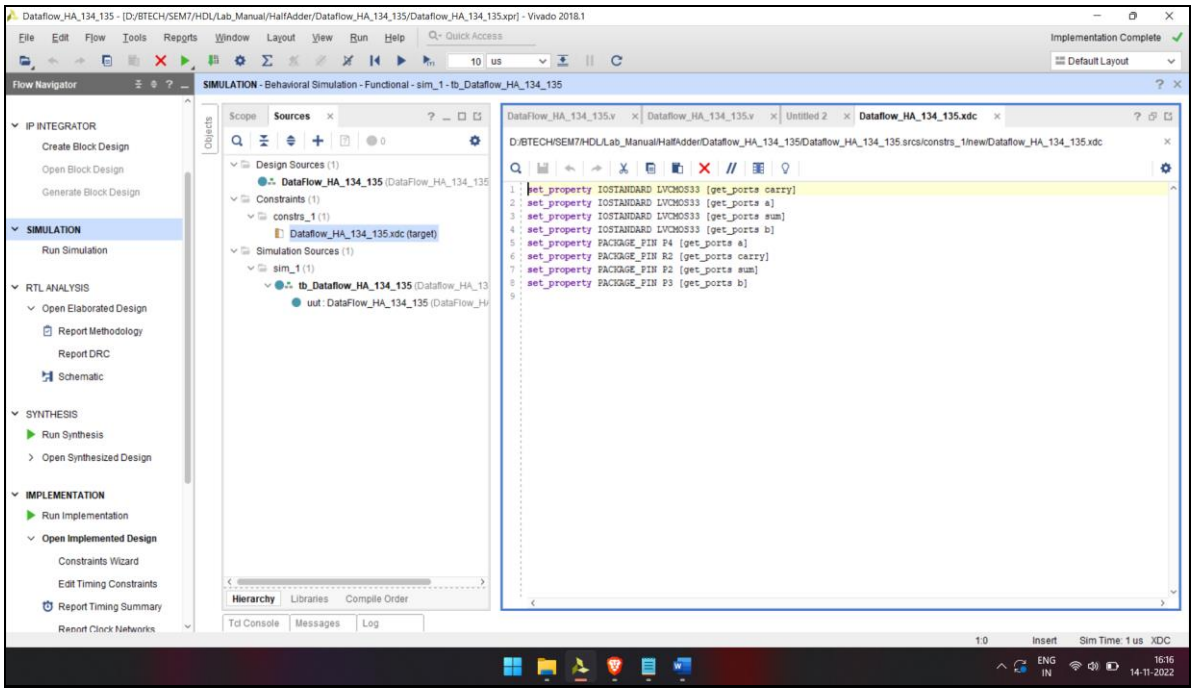
Test Bench



Simulation:



XDC File



Design Summary: