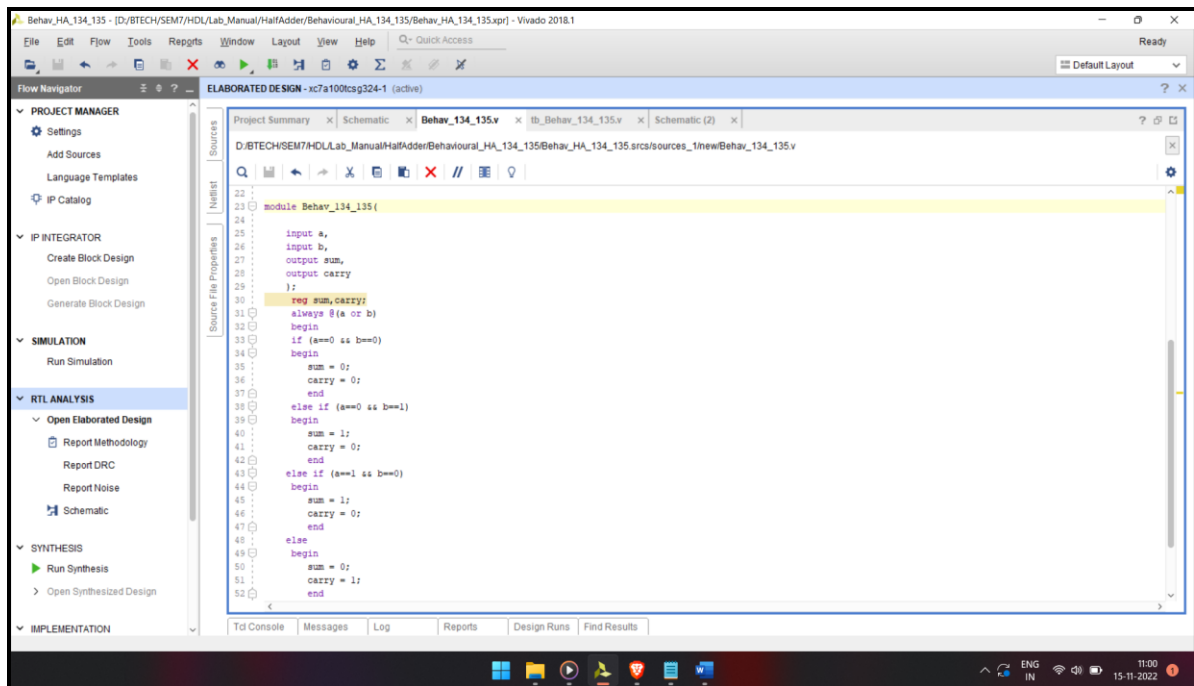


# HALF ADDER

## Behavioural Model

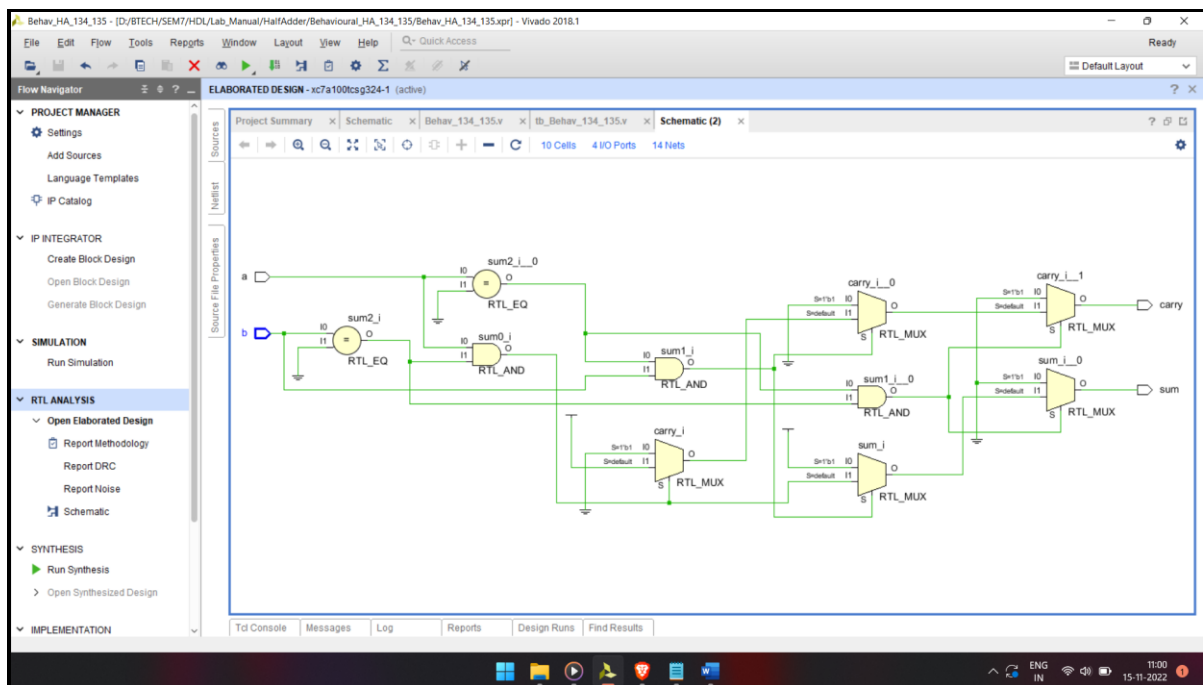
Verilog code



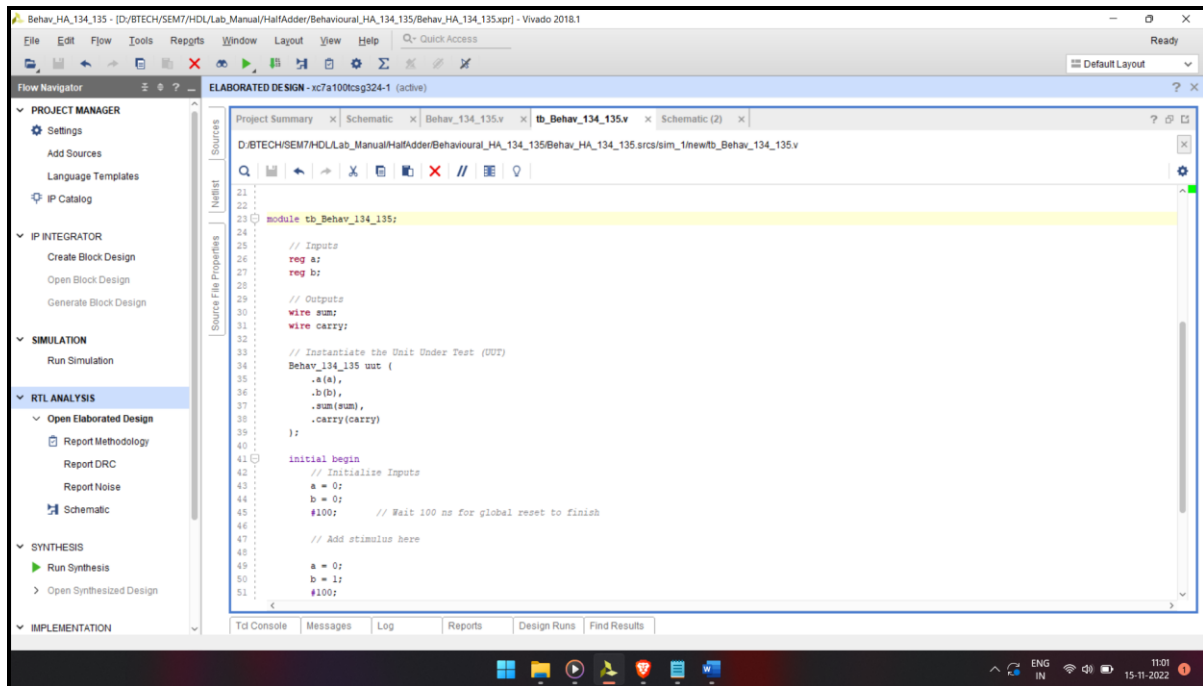
The screenshot shows the Vivado IDE interface with the Verilog code for a Half Adder Behavioral Model. The code is as follows:

```
22 module Behav_134_135(  
23     input a,  
24     input b,  
25     output sum,  
26     output carry  
27 );  
28     reg sum,carry;  
29     always @(a or b)  
30     begin  
31         sum = 0;  
32         carry = 0;  
33         if (a==0 && b==0)  
34             sum = 0;  
35         else if (a==0 && b==1)  
36             sum = 1;  
37         else if (a==1 && b==0)  
38             sum = 1;  
39         else if (a==1 && b==1)  
40             sum = 0;  
41             carry = 1;  
42         end  
43     end  
44     sum  
45     carry  
46 end
```

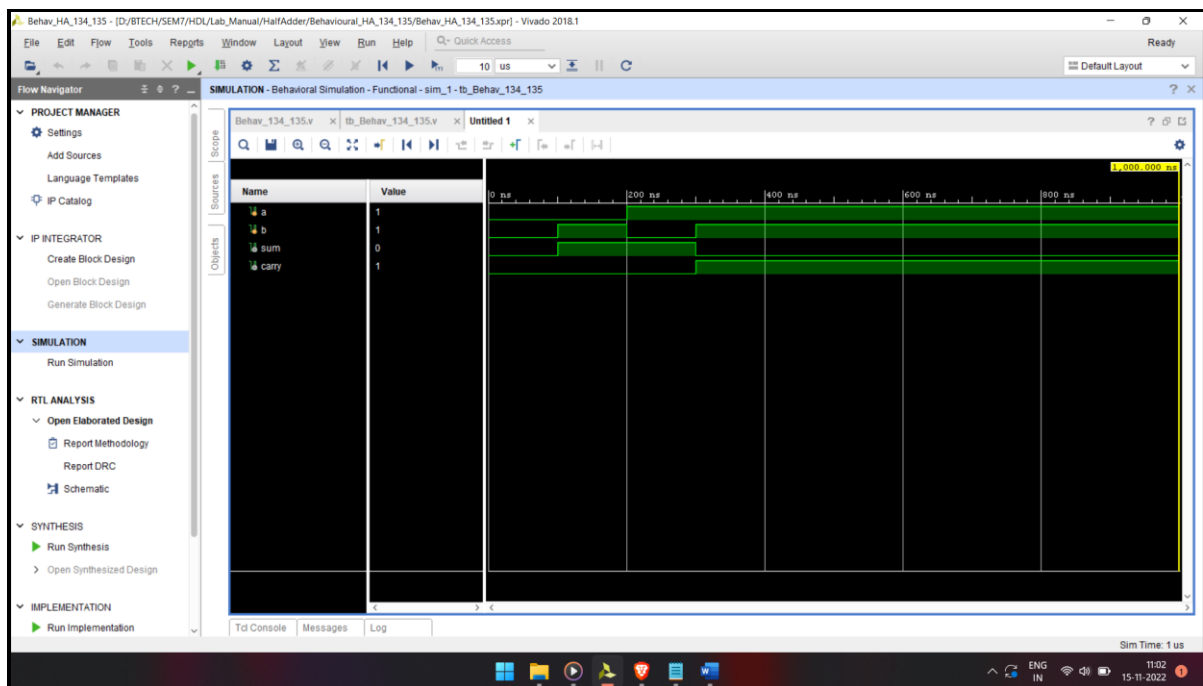
RTL



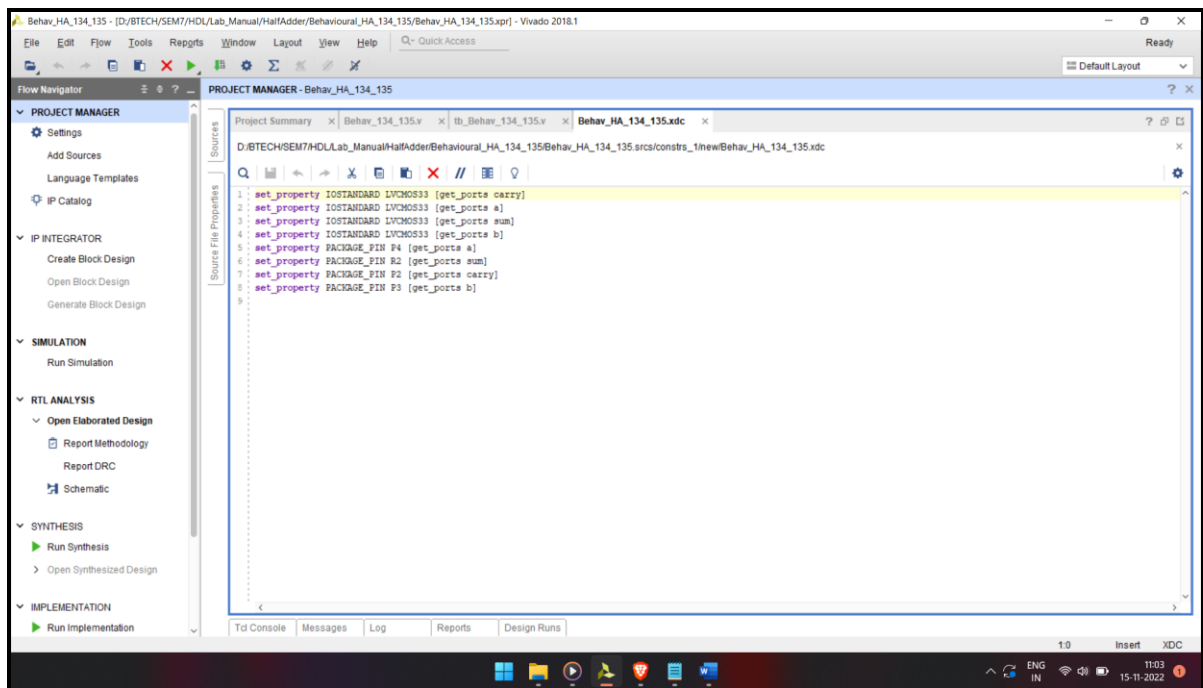
## Test Bench



## Simulation



## XDC File



## Design Summary

