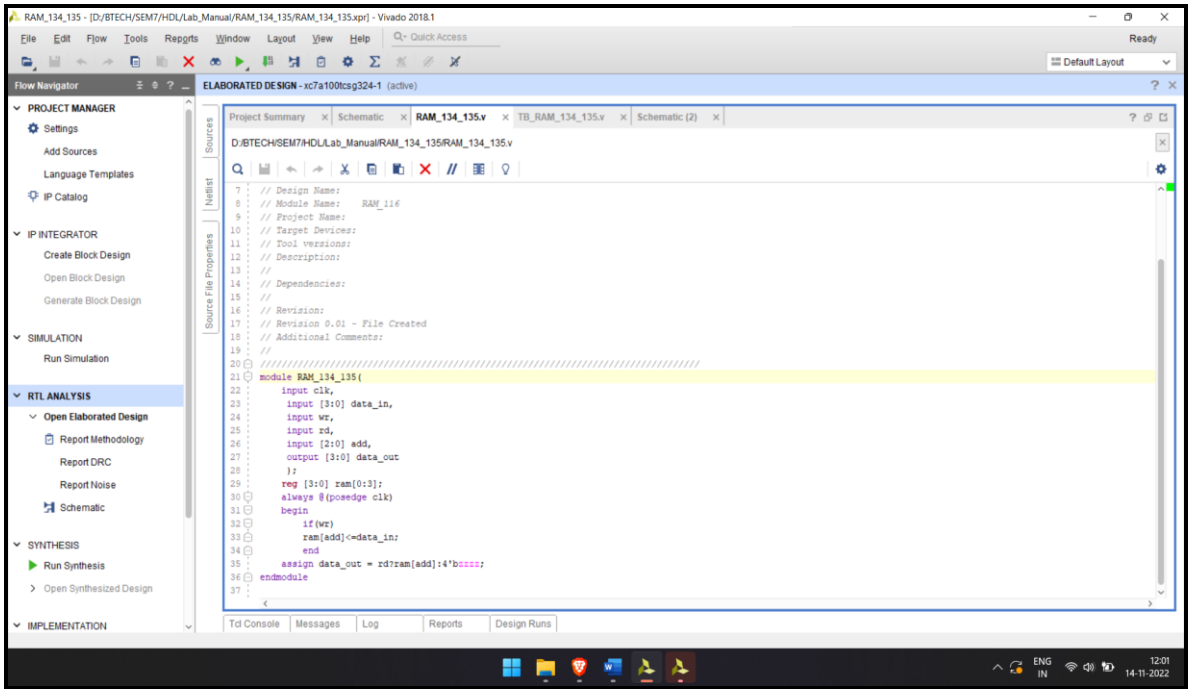
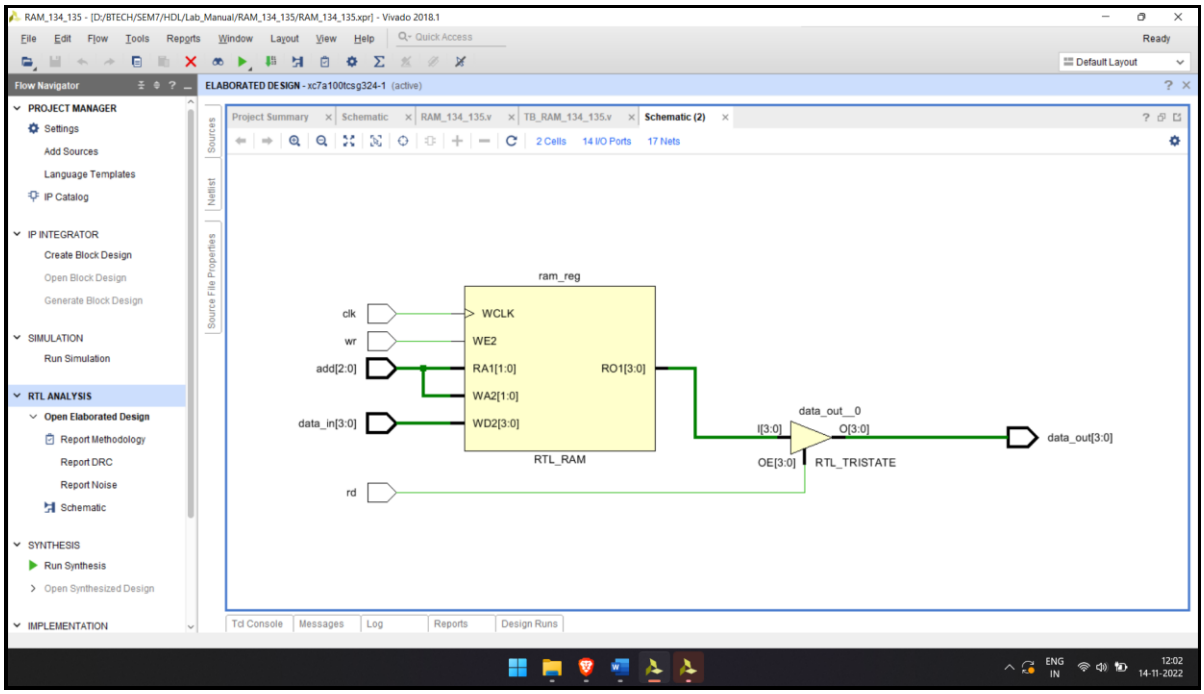
LAB NO.10

RAM

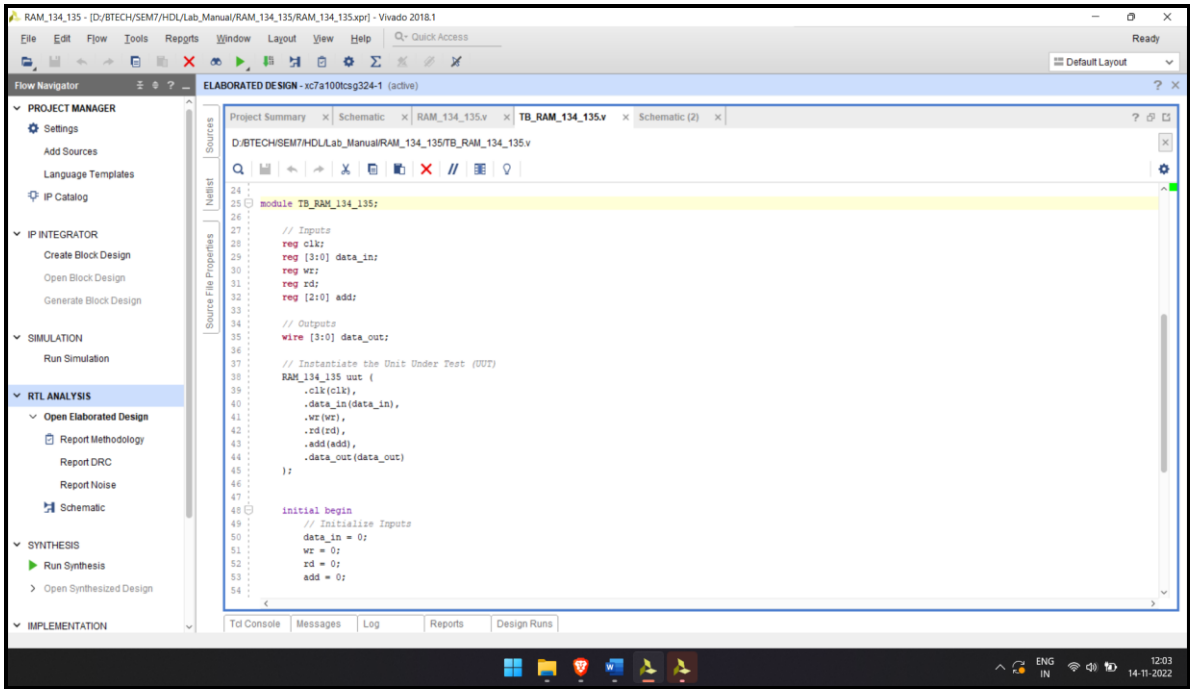
Verilog Code



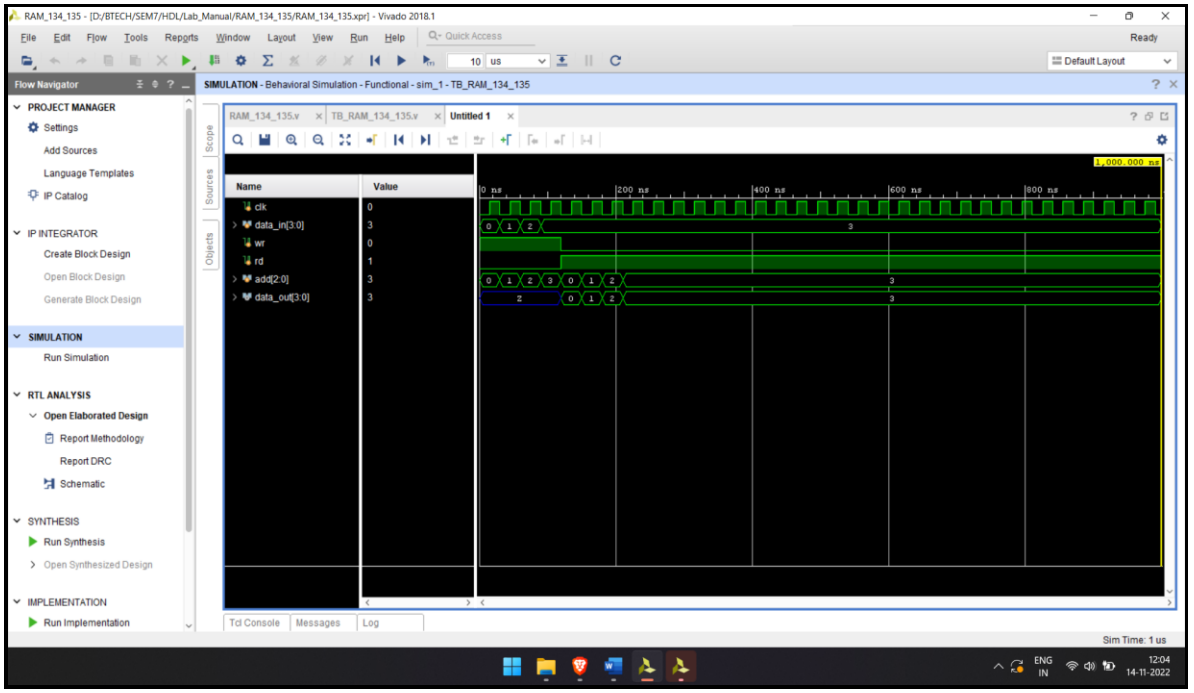
RTL design



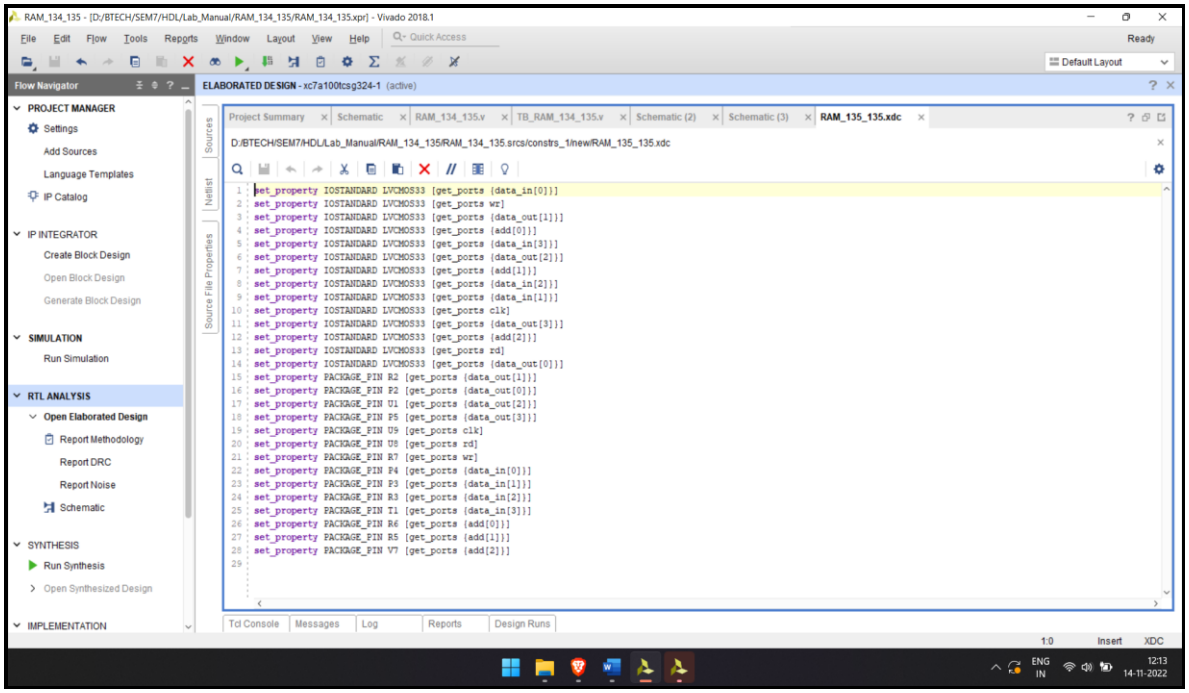
Test Bench



Simulation



XDC



Design Summary