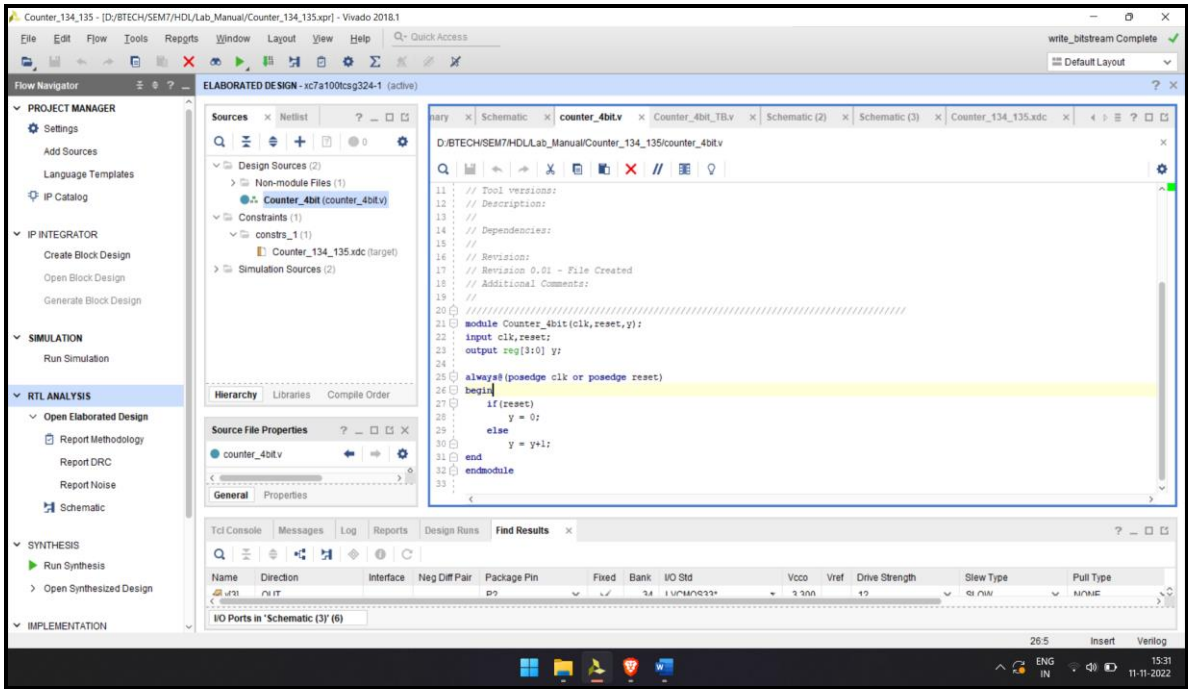
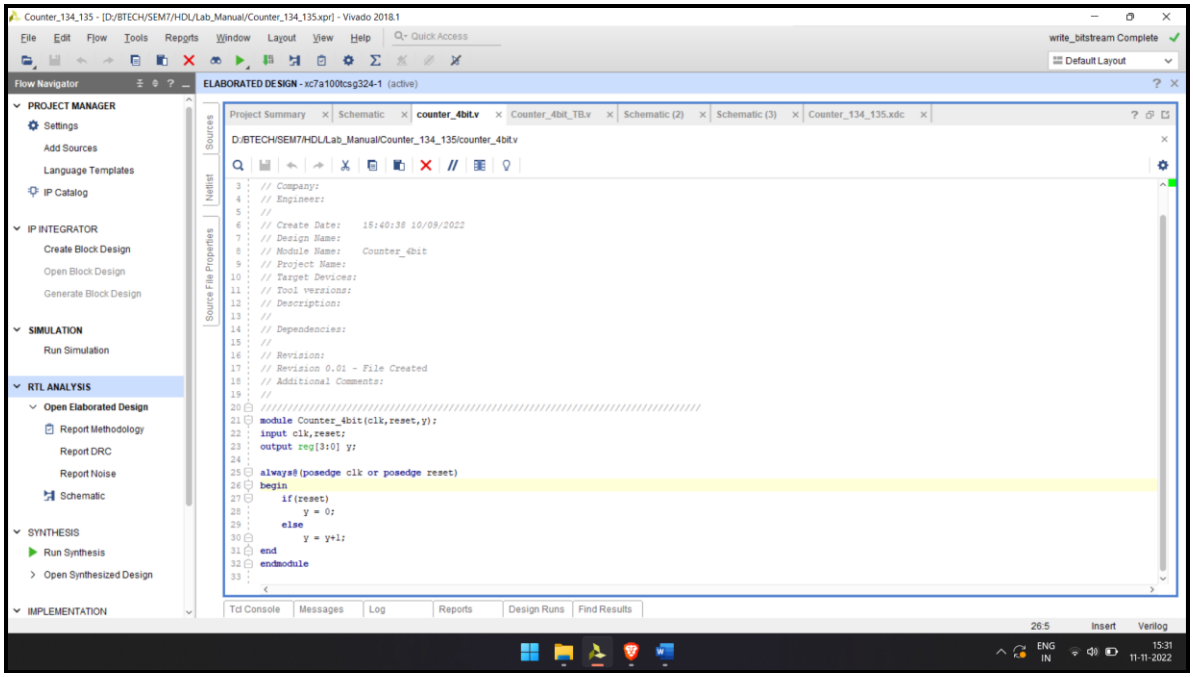
LAB No: 07

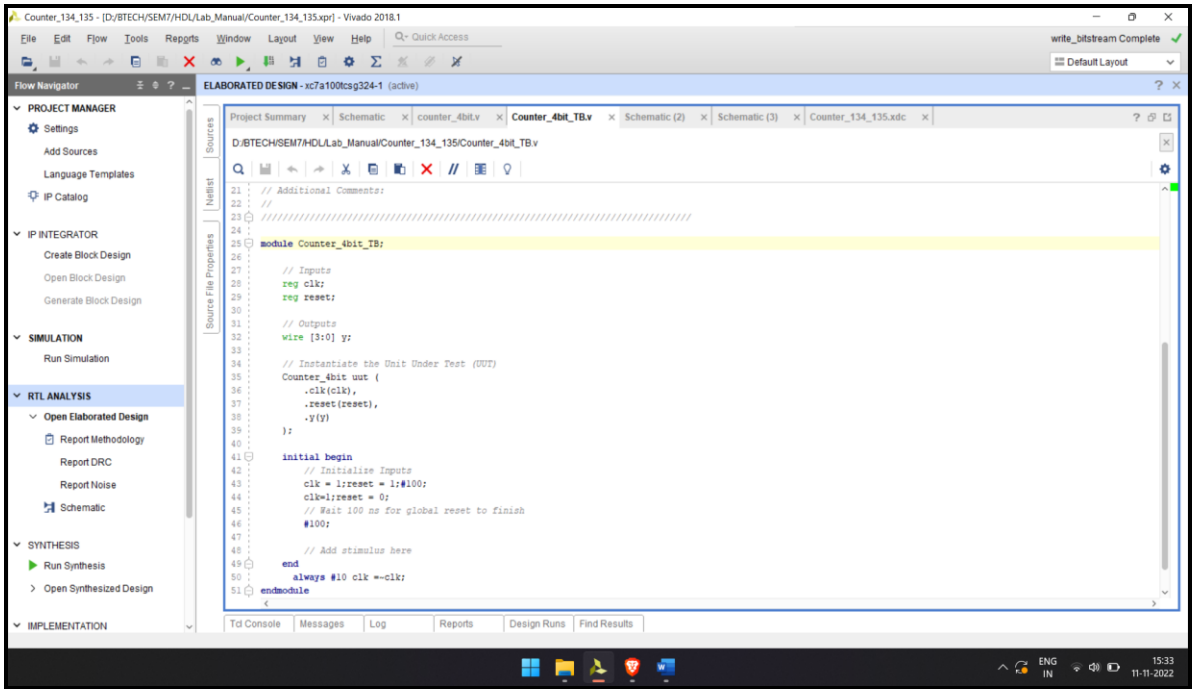
COUNTER

Verilog Code:

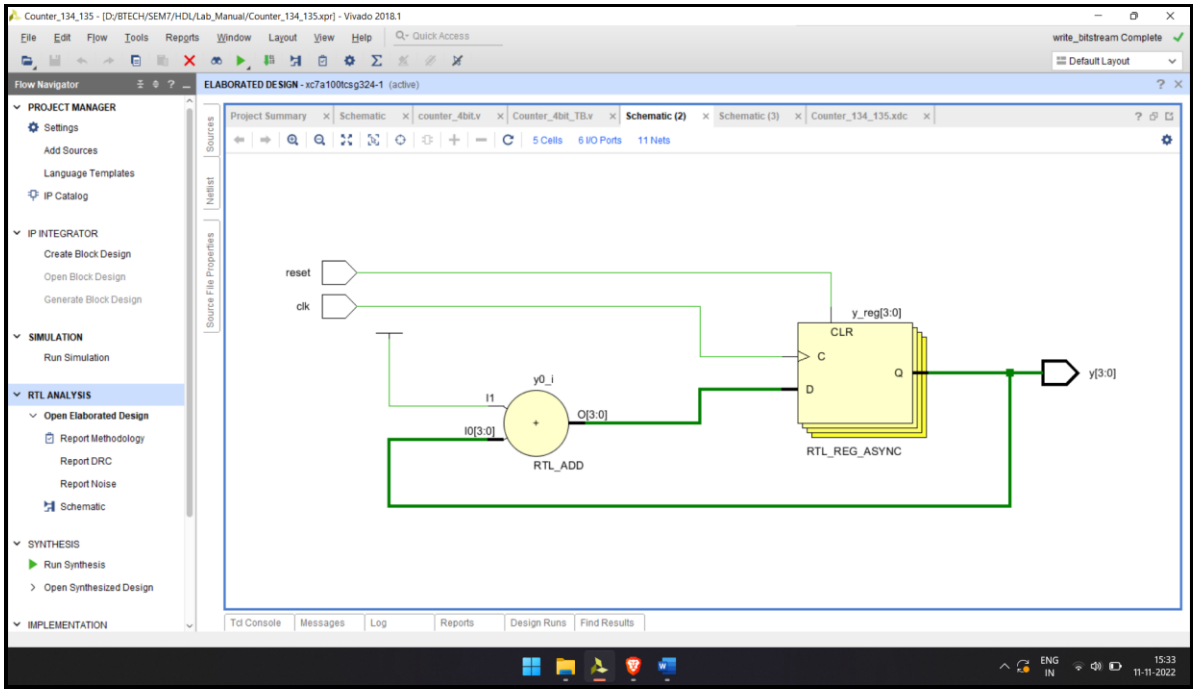




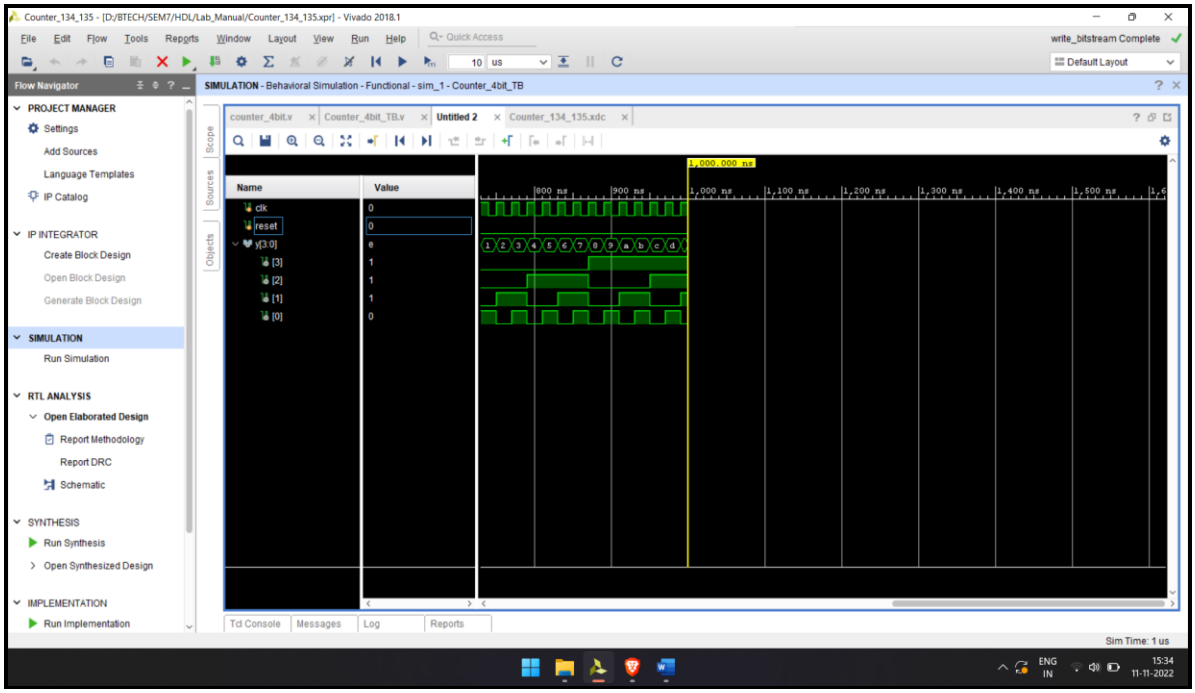
TestBench:



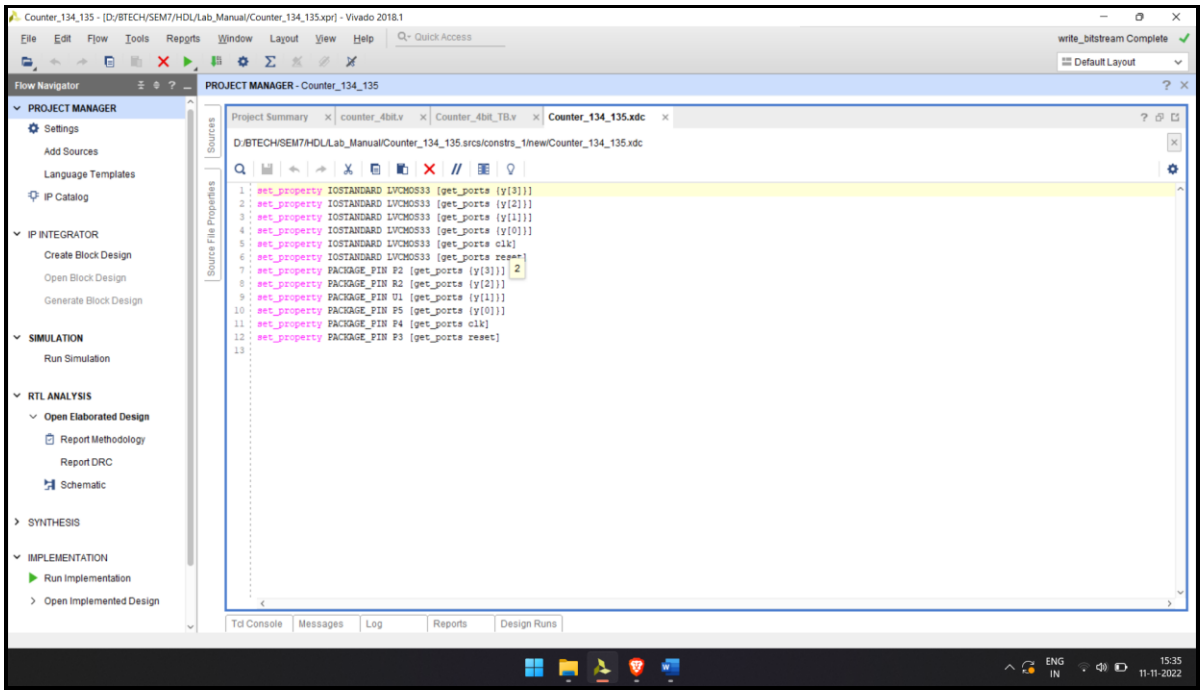
RTL Schematic:



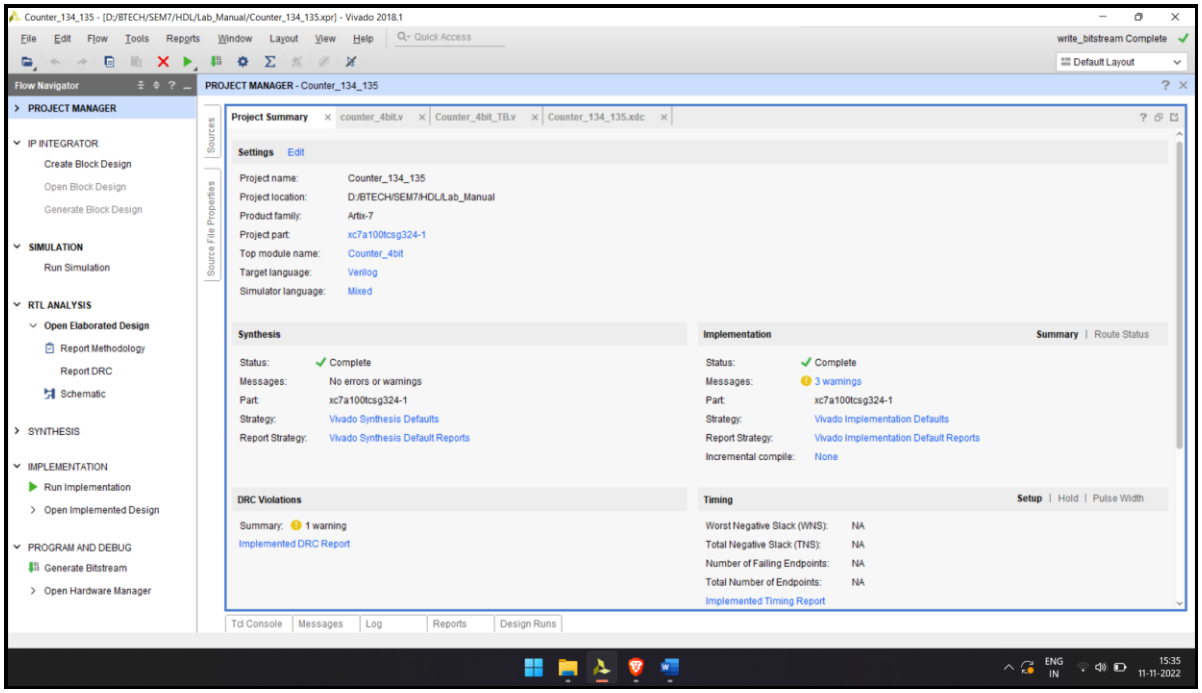
Simulation:



XDC file:



Design Summary:



Hardware Complete: