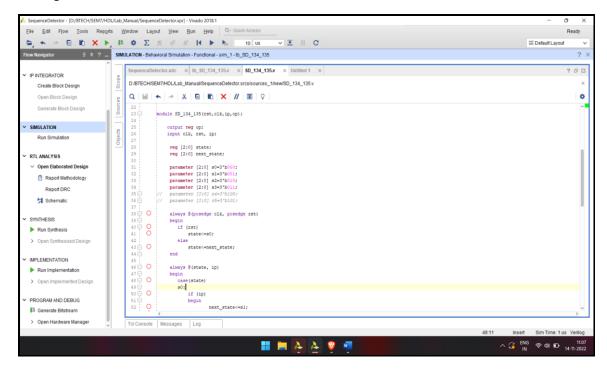
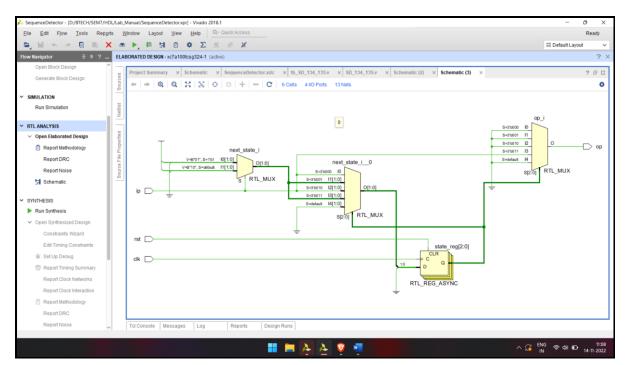
LAB NO.08

SEQUENCE DETECTOR

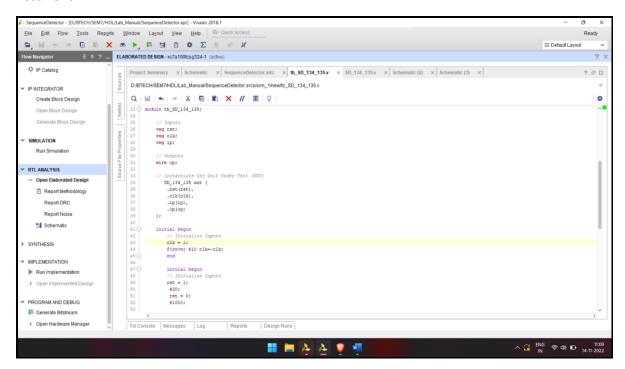
Verilog Code:



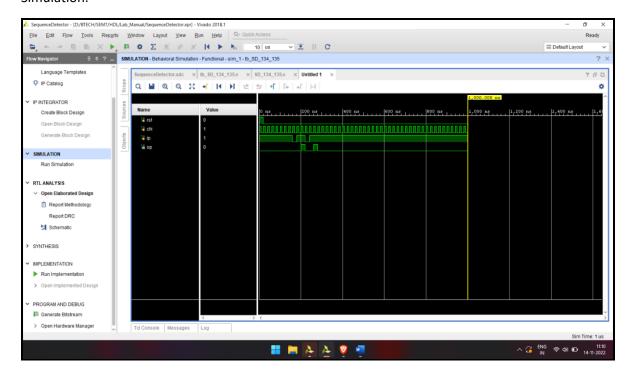
RTL



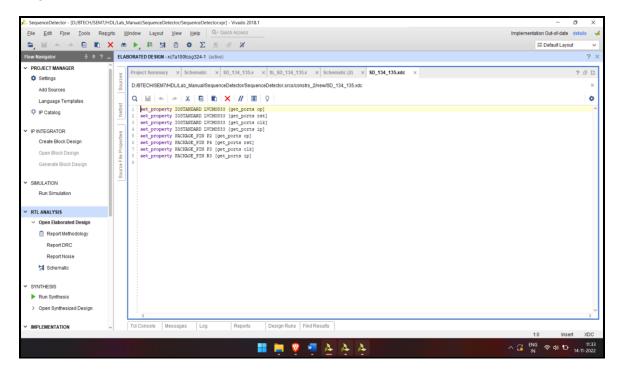
Test Bench:



Simulation:



XDC



Design Summary:

