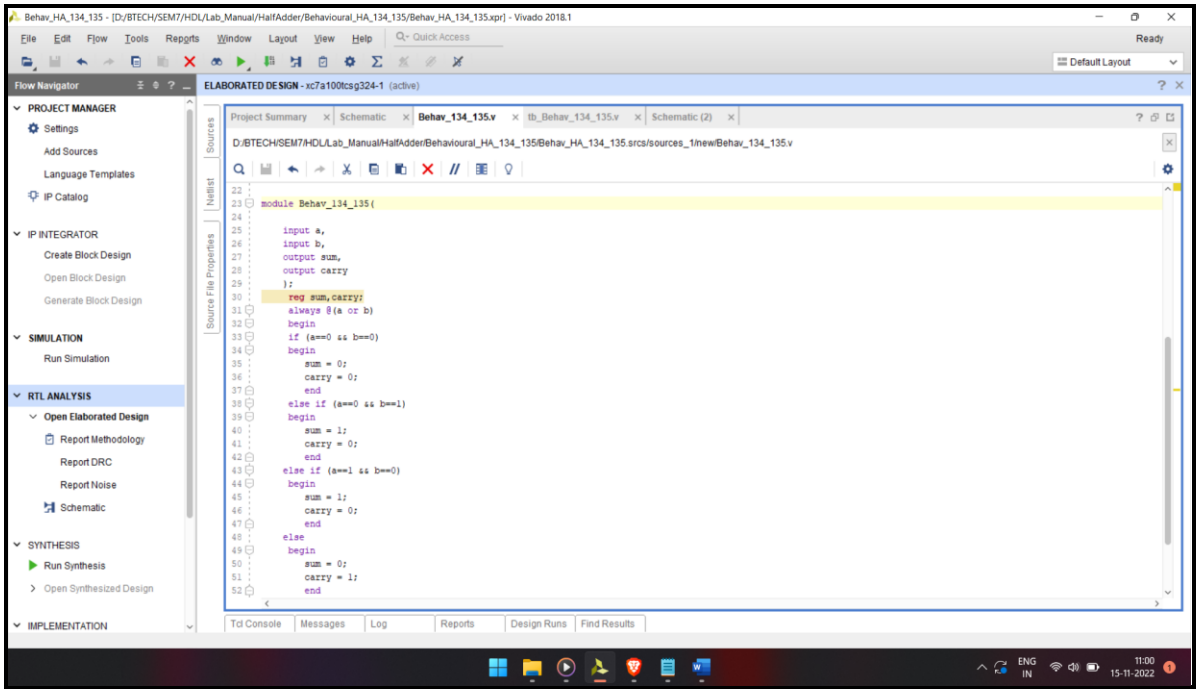
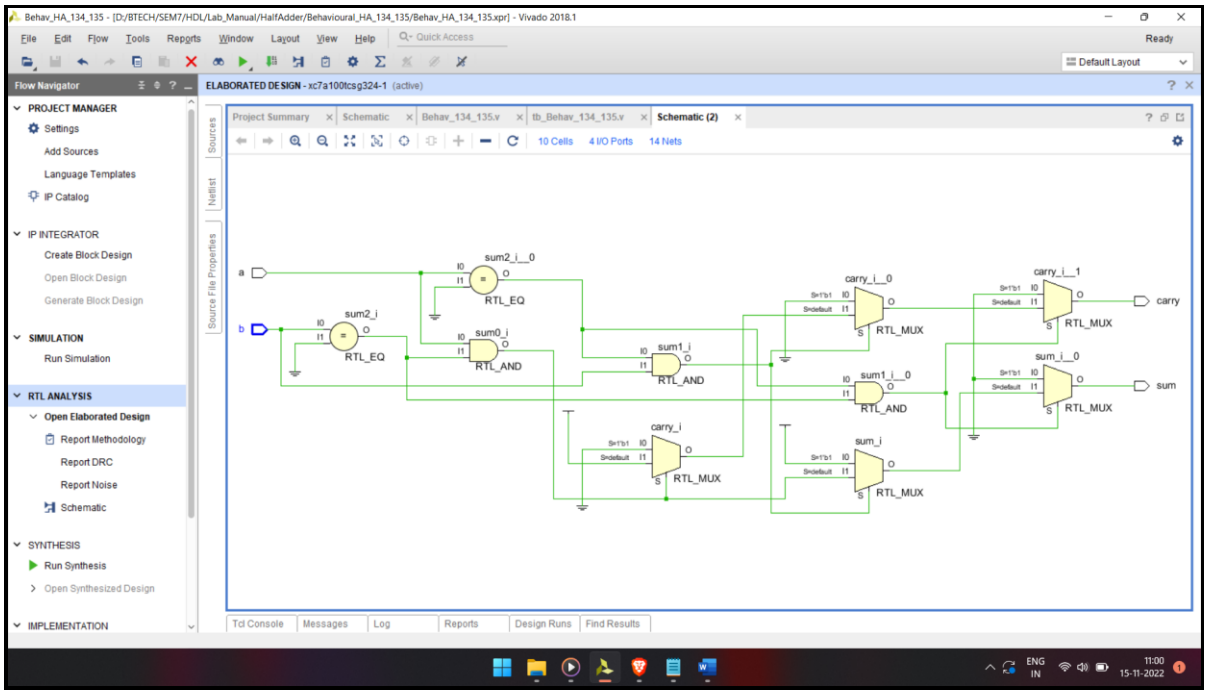
HALF ADDER

Behavioural Model

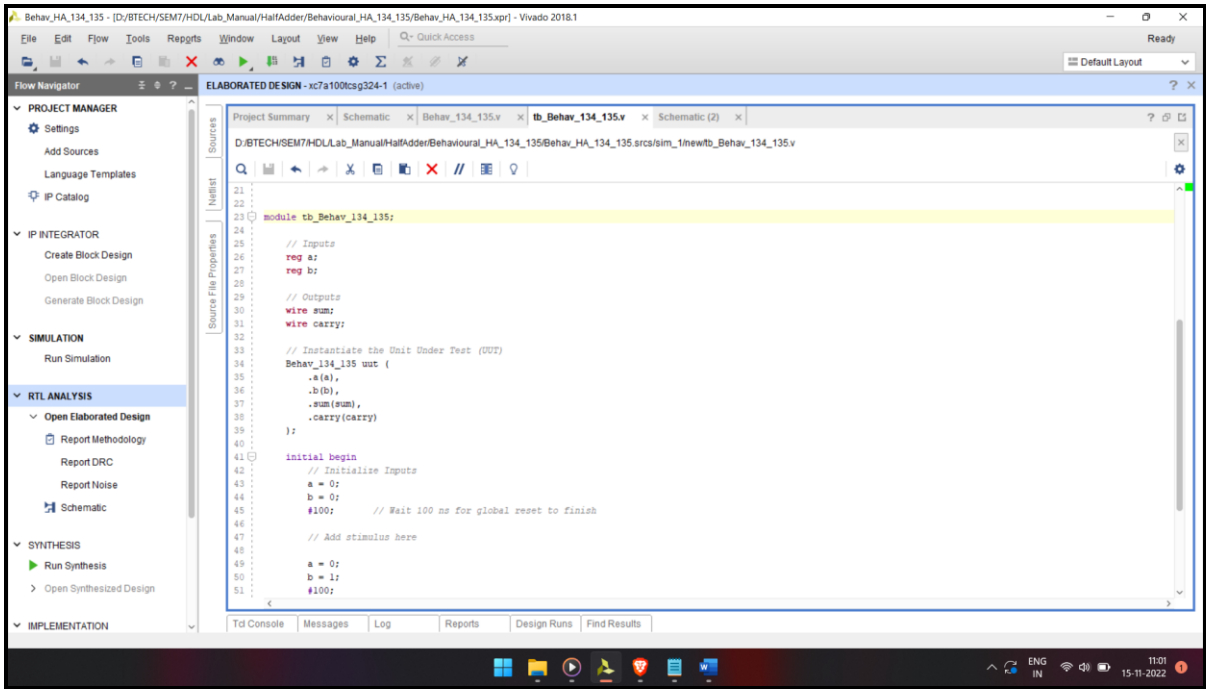
Verilog code



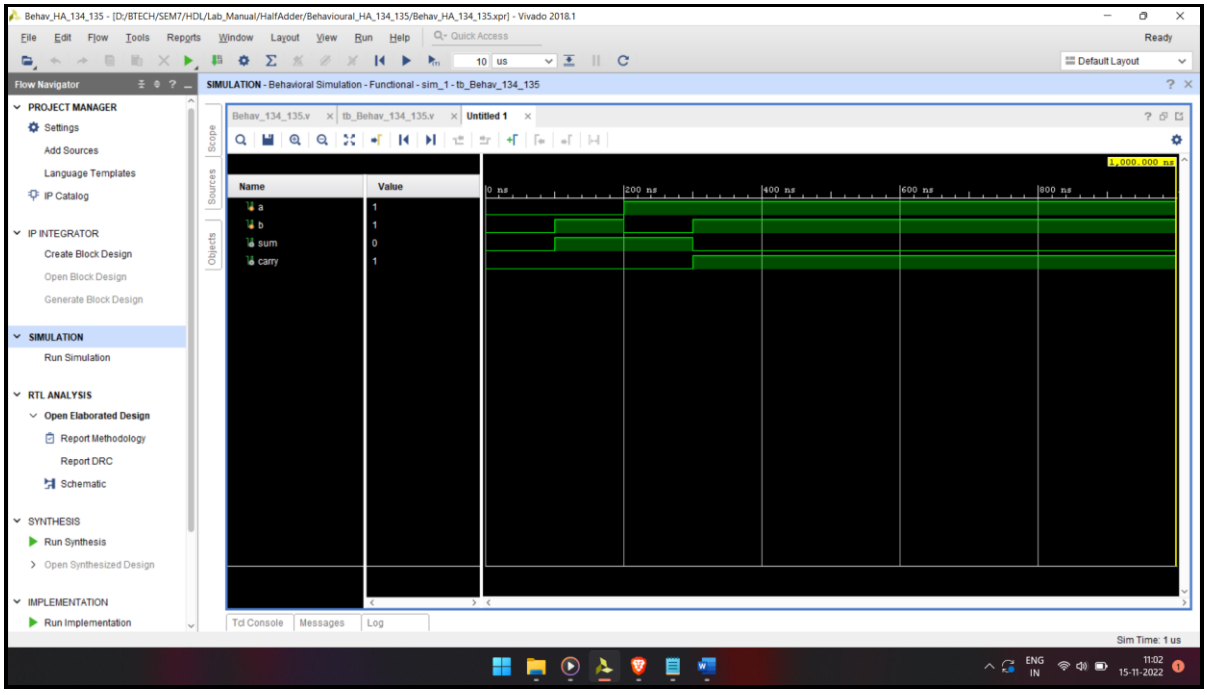
RTL



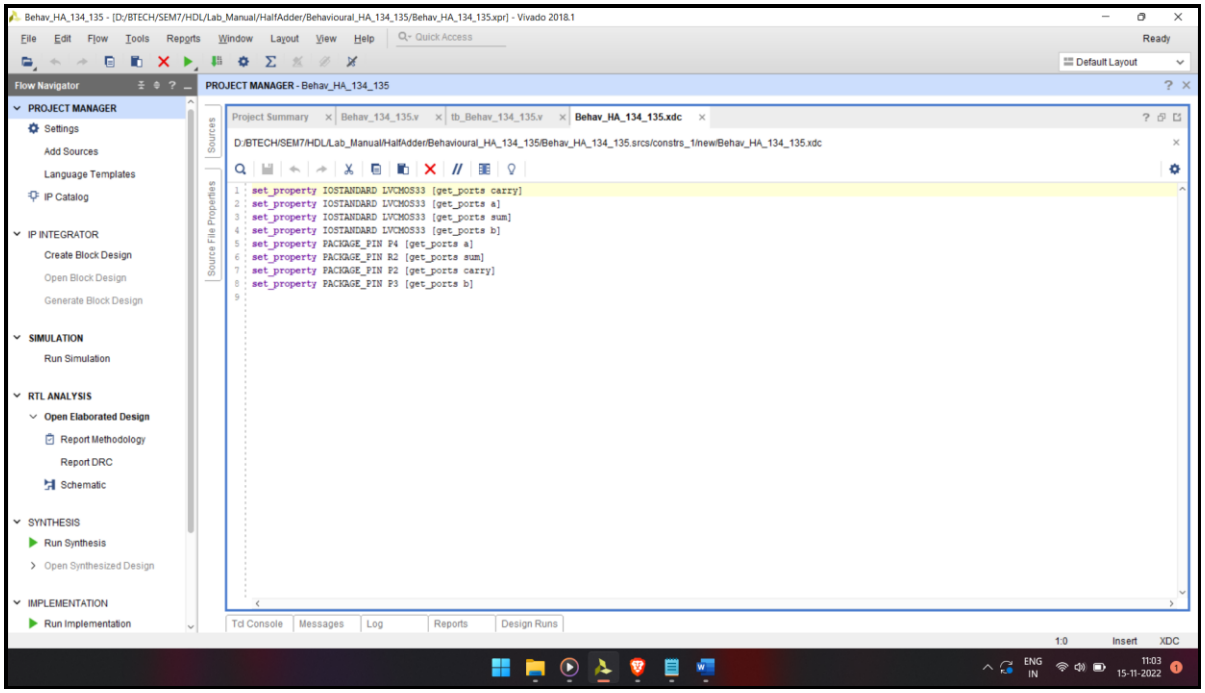
Test Bench



Simulation



XDC File



Design Summary