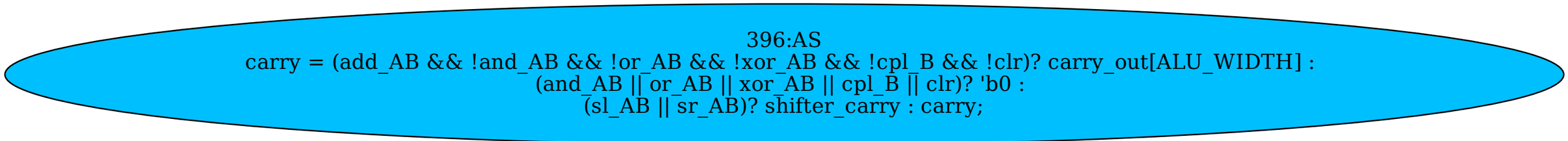
396:AS
carry = (add_AB && !and_AB && !or_AB && !xor_AB && !cpl_B && !clr)? carry_out[ALU_WIDTH] :
(and_AB || or_AB || xor_AB || cpl_B || clr)? 'b0 :
(sl_AB || sr_AB)? shifter_carry : carry;