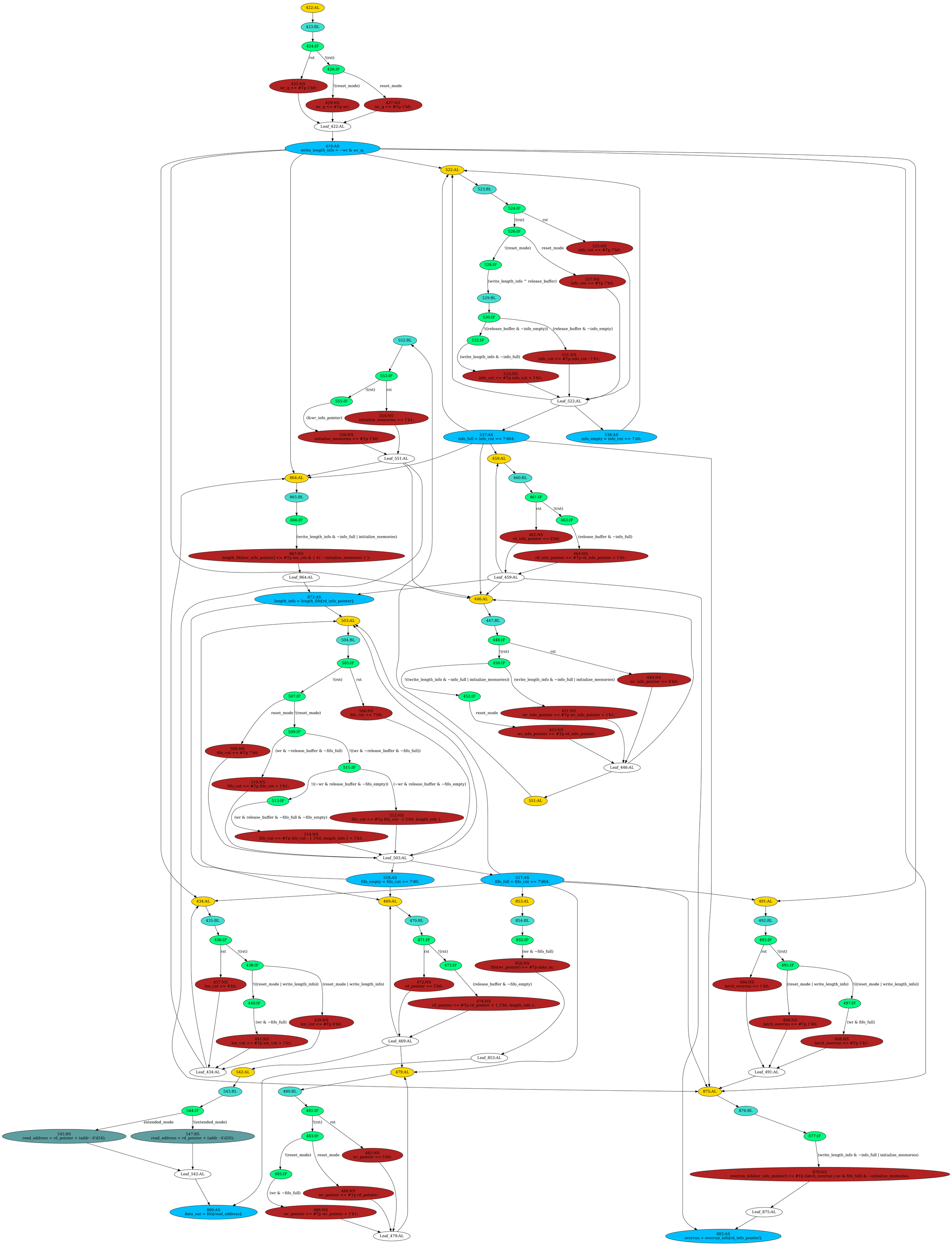
422:AL
423:BL
424:IF
rst
!(rst)
426:IF
425:NS
wr_q <= #Tp 1'b0;
!(reset_mode)
reset_mode
429:NS
wr_q <= #Tp wr;
427:NS
wr_q <= #Tp 1'b0;
Leaf_422:AL
419:AS
write_length_info = ~wr & wr_q;
522:AL
523:BL
524:IF
!(rst)
rst
526:IF
!(reset_mode)
reset_mode
525:NS
info_cnt <= #Tp 7'h0;
528:IF
(write_length_info ^ release_buffer)
527:NS
info_cnt <= #Tp 7'h0;
529:BL
530:IF
!((release_buffer & ~info_empty))
(release_buffer & ~info_empty)
532:IF
(write_length_info & ~info_full)
531:NS
info_cnt <= #Tp info_cnt - 1'b1;
533:NS
info_cnt <= #Tp info_cnt + 1'b1;
Leaf_522:AL
537:AS
info_full = info_cnt == 7'd64;
538:AS
info_empty = info_cnt == 7'd0;
552:BL
553:IF
!(rst)
rst
555:IF
(&wr_info_pointer)
554:NS
initialize_memories <= 1'b1;
556:NS
initialize_memories <= #Tp 1'b0;
Leaf_551:AL
459:AL
460:BL
461:IF
rst
!(rst)
463:IF
462:NS
rd_info_pointer <= 6'h0;
(release_buffer & ~info_full)
464:NS
rd_info_pointer <= #Tp rd_info_pointer + 1'b1;
Leaf_459:AL
864:AL
865:BL
866:IF
(write_length_info & ~info_full | initialize_memories)
867:NS
length_fifo[wr_info_pointer] <= #Tp len_cnt & { 4{ ~initialize_memories } };
Leaf_864:AL
872:AS
length_info = length_fifo[rd_info_pointer];
446:AL
447:BL
448:IF
!(rst)
rst
450:IF
!((write_length_info & ~info_full | initialize_memories))
(write_length_info & ~info_full | initialize_memories)
449:NS
wr_info_pointer <= 6'h0;
452:IF
reset_mode
451:NS
wr_info_pointer <= #Tp wr_info_pointer + 1'b1;
453:NS
wr_info_pointer <= #Tp rd_info_pointer;
Leaf_446:AL
503:AL
504:BL
505:IF
!(rst)
rst
507:IF
reset_mode !(reset_mode)
506:NS
fifo_cnt <= 7'h0;
509:IF
508:NS
fifo_cnt <= #Tp 7'h0;
(wr & ~release_buffer & ~fifo_full)
!((wr & ~release_buffer & ~fifo_full))
511:IF
510:NS
fifo_cnt <= #Tp fifo_cnt + 1'b1;
!((~wr & release_buffer & ~fifo_empty))
(~wr & release_buffer & ~fifo_empty)
513:IF
(wr & release_buffer & ~fifo_full & ~fifo_empty)
512:NS
fifo_cnt <= #Tp fifo_cnt - { 3'h0, length_info };
514:NS
fifo_cnt <= #Tp fifo_cnt - { 3'h0, length_info } + 1'b1;
Leaf_503:AL
551:AL
518:AS
fifo_empty = fifo_cnt == 7'd0;
517:AS
fifo_full = fifo_cnt == 7'd64;
434:AL
435:BL
436:IF
rst
!(rst)
438:IF
437:NS
len_cnt <= 4'h0;
!((reset_mode | write_length_info))
(reset_mode | write_length_info)
440:IF
(wr & ~fifo_full)
439:NS
len_cnt <= #Tp 4'h0;
441:NS
len_cnt <= #Tp len_cnt + 1'b1;
Leaf_434:AL
542:AL
543:BL
544:IF
extended_mode
!(extended_mode)
545:BS
read_address = rd_pointer + (addr - 6'd16);
547:BS
read_address = rd_pointer + (addr - 6'd20);
Leaf_542:AL
860:AS
data_out = fifo[read_address];
469:AL
470:BL
471:IF
rst
!(rst)
473:IF
472:NS
rd_pointer <= 5'h0;
(release_buffer & ~fifo_empty)
474:NS
rd_pointer <= #Tp rd_pointer + { 2'h0, length_info };
Leaf_469:AL
480:BL
481:IF
!(rst)
rst
483:IF
!(reset_mode)
reset_mode
482:NS
wr_pointer <= 5'h0;
485:IF
(wr & ~fifo_full)
484:NS
wr_pointer <= #Tp rd_pointer;
486:NS
wr_pointer <= #Tp wr_pointer + 1'b1;
Leaf_479:AL
853:AL
854:BL
855:IF
(wr & ~fifo_full)
856:NS
fifo[wr_pointer] <= #Tp data_in;
Leaf_853:AL
479:AL
491:AL
492:BL
493:IF
rst
!(rst)
495:IF
494:NS
latch_overrun <= 1'b0;
(reset_mode | write_length_info)
!((reset_mode | write_length_info))
497:IF
496:NS
latch_overrun <= #Tp 1'b0;
(wr & fifo_full)
498:NS
latch_overrun <= #Tp 1'b1;
Leaf_491:AL
875:AL
876:BL
877:IF
(write_length_info & ~info_full | initialize_memories)
878:NS
overrun_info[wr_info_pointer] <= #Tp (latch_overrun | wr & fifo_full) & ~initialize_memories;
Leaf_875:AL
883:AS
overrun = overrun_info[rd_info_pointer];