541:AL
542:NS rx_data_done_r <= rx_data_done;
Leaf_541:AL
661:AL
544:AL
662:NS wr_done_r <= rx_data_done_r;
545:NS rx_data_done_r2 <= rx_data_done_r;
Leaf_661:AL
Leaf_544:AL
554:AL
555:NS send_zero_length_r <= send_zero_length;
664:AL
665:NS wr_done <= wr_done_r;
Leaf_554:AL
Leaf_664:AL
725:AL
728:BL next_state = state; mreq_d = 1'b0; mwe_d = 1'b0; rd_first = 1'b0; dtmp_sel = 1'b0; wr_last_en = 1'b0;
736:CS
state
787:CA
833:CA
849:CA
886:CA
810:CA
737:CA
868:CA
764:CA
788:BL mwe_d = 1'b1;
834:BL mwe_d = 1'b1;
850:BL mreq_d = 1'b1;
887:BL
811:BL mwe_d = 1'b1; wr_last_en = 1'b1;
738:BL
869:BL mreq_d = 1'b1;
765:BL
795:IF
801:IF
796:IF
803:IF
841:IF
846:IF
863:IF
864:IF
858:IF
857:IF
866:IF
901:IF
897:IF
903:IF
895:IF
894:IF
896:IF
818:IF
820:IF
826:IF
828:IF
830:IF
819:IF
758:IF
745:IF
754:IF
746:BL
749:IF
747:IF
748:IF
876:IF
877:IF
882:IF
884:IF
772:IF
773:IF
777:IF
779:IF
(abort === 1'bx)
!(abort)
abort
(rx_data_done_r2 === 1'bx)
rx_data_done_r2
mack_r
(mack_r === 1'bx)
(sizd_is_zero || abort)
!((sizd_is_zero || abort))
(rd_next === 1'bx)
(adrb_is_3 && rd_next)
(sizd_is_zero === 1'bx)
(adrb_is_3 === 1'bx)
(wr_done === 1'bx)
wr_last
!(wr_last)
wr_done
(wr_last === 1'bx)
(tx_dma_en_r && !abort && !send_zero_length_r)
rst
(rx_dma_en_r && !abort)
(rx_dma_en_r === 1'bx)
(tx_dma_en_r === 1'bx)
!(mack_r)
795:SS
804:BL wr_last_en = 1'b1; next_state = MEM_WR1;
801:BS next_state = IDLE;
796:SS
841:SS
846:BS next_state = IDLE;
863:BS rd_first = 1'b1;
864:BS next_state = IDLE;
866:BS next_state = MEM_RD2;
857:SS
858:SS
901:BS next_state = IDLE;
903:BS next_state = MEM_RD2;
897:SS
895:SS
894:SS
896:SS
818:SS
820:SS
826:BS next_state = IDLE;
828:BS next_state = MEM_WR2;
830:BS next_state = IDLE;
819:SS
759:BL next_state = MEM_RD1;
755:BL next_state = WAIT_MRD;
749:SS
747:SS
748:SS
876:SS
877:SS
882:BS next_state = IDLE;
884:BS next_state = MEM_RD3;
772:SS
773:SS
777:BS next_state = IDLE;
779:BS next_state = MEM_WR;
781:BL dtmp_sel = 1'b1; mreq_d = 1'b1;
Leaf_725:AL
602:AS siz_dec = rd_first & mack_r | rd_next & (sizd_c != 14'h0);
720:AL
722:IF
(!rst)
!((!rst))
722:NS state <= IDLE;
723:NS state <= next_state;
Leaf_720:AL
594:AL
596:IF
598:IF
(tx_dma_en || tx_dma_en_r)
!((tx_dma_en || tx_dma_en_r))
596:NS sizd_c <= 14'h3fff;
598:NS sizd_c <= size;
600:IF
siz_dec
600:NS sizd_c <= sizd_c - 14'h1;
Leaf_594:AL
604:AS sizd_is_zero_d = sizd_c == 14'h0;
625:AL
699:AL
606:AL
626:NS idma_done <= rx_data_done_r | sizd_is_zero_d;
701:IF
607:NS sizd_is_zero <= sizd_is_zero_d;
Leaf_625:AL
703:IF
Leaf_606:AL
701:NS send_data_r <= 1'b0;
!(rd_first)
rd_first
705:IF
703:NS send_data_r <= 1'b1;
((sizd_c == 14'h1) && rd_next || sizd_is_zero_d)
705:NS send_data_r <= 1'b0;
Leaf_699:AL
707:AS send_data = send_data_r | send_zero_length_r;
524:AL
525:NS mwe <= mwe_d;
Leaf_524:AL
Leaf_648:AL
651:AL
652:NS word_done_r <= word_done & !word_done_r;
Leaf_651:AL
516:AS mreq = mreq_d & !mack_r | word_done_r;
527:AL
528:NS mack_r <= mreq & mack;
Leaf_527:AL
548:AL
549:NS tx_dma_en_r <= tx_dma_en;
Leaf_548:AL
551:AL
552:NS rx_dma_en_r <= rx_dma_en;
Leaf_551:AL
694:AS adrb_is_3 = adr_cb[1:0] == 2'h3;
622:AS siz_inc = rx_data_valid_r;
613:AL
615:IF
!((!rst))
(!rst)
618:IF
rx_dma_en_r
!(rx_dma_en_r)
615:NS sizu_c <= 11'h0;
620:IF
618:NS sizu_c <= 11'h0;
siz_inc
620:NS sizu_c <= sizu_c + 11'h1;
Leaf_613:AL
535:AL
536:NS rx_data_valid_r <= rx_data_valid;
Leaf_535:AL
587:AS adr_incb = rx_data_valid_r | rd_next;
Leaf_576:AL
583:AL
584:IF
!(adr_incb)
adr_incb
585:BS adrb_next = adr_cb;
584:BS adrb_next = adr_cb + 3'h1;
Leaf_583:AL
576:AL
578:IF
!((!rst))
(!rst)
580:IF
578:NS adr_cb <= 3'h0;
!((rx_dma_en_r || tx_dma_en_r))
(rx_dma_en_r || tx_dma_en_r)
581:NS adr_cb <= adrb_next;
580:NS adr_cb <= adr[2:0];
633:AL
634:NS dtmp_sel_r <= dtmp_sel;
Leaf_633:AL
588:AS adr_incw = !dtmp_sel_r & mack_r;
658:AL
659:NS wr_last <= (adr_cb[1:0] != 2'h0) & !rx_data_valid_r & wr_last_en;
Leaf_658:AL
538:AL
539:NS rx_data_st_r <= rx_data_st;
Leaf_538:AL
648:AL
637:AL
649:NS word_done <= (adr_cb[1:0] == 2'h3) & rx_data_valid_r | wr_last;
638:IF
!(dtmp_sel_r)
dtmp_sel_r
640:IF
638:NS dtmp_r <= mdin;
rx_data_valid_r
641:BL
644:IF
645:IF
642:IF
643:IF
(adr_cb[1:0] == 2'h2)
(adr_cb[1:0] == 2'h3)
(adr_cb[1:0] == 2'h0)
(adr_cb[1:0] == 2'h1)
644:NS dtmp_r[23:16] <= rx_data_st_r;
645:NS dtmp_r[31:24] <= rx_data_st_r;
642:NS dtmp_r[07:00] <= rx_data_st_r;
643:NS dtmp_r[15:08] <= rx_data_st_r;
Leaf_637:AL
655:AL
656:IF
word_done
656:NS dout_r <= dtmp_r;
Leaf_655:AL
519:AS mdout = dout_r;
569:AL
570:IF
adr_incw
!(adr_incw)
570:BS adrw_next = adr_cw + { { SSRAM_HADR{ 1'b0 } }, 1'b1 };
571:BS adrw_next = adr_cw;
Leaf_569:AL
562:AL
563:NS last_buf_adr <= adr + { { SSRAM_HADR + 2 - 13{ 1'b0 } }, buf_size };
Leaf_562:AL
565:AL
566:IF
!(((adrw_next == last_buf_adr) && dma_en))
((adrw_next == last_buf_adr) && dma_en)
567:BS adrw_next1 = adrw_next;
566:BS adrw_next1 = { SSRAM_HADR + 1{ 1'b0 } };
Leaf_565:AL
558:AL
559:IF
(rx_dma_en_r || tx_dma_en_r)
!((rx_dma_en_r || tx_dma_en_r))
559:NS adr_cw <= adr[SSRAM_HADR+2:2];
560:NS adr_cw <= adrw_next1;
Leaf_558:AL
692:AS fill_buf1 = adr_cw[0] & mack_r;
522:AS madr = adr_cw;
691:AS fill_buf0 = !adr_cw[0] & mack_r;
676:AL
677:IF
fill_buf1
677:NS rd_buf1 <= mdin;
Leaf_676:AL
673:AL
674:IF
fill_buf0
674:NS rd_buf0 <= mdin;
Leaf_673:AL
679:AL
680:CS
adrb_next[2:0]
682:CA
686:CA
687:CA
684:CA
685:CA
681:CA
688:CA
683:CA
682:BS tx_data_st = rd_buf0[15:08];
686:BS tx_data_st = rd_buf1[15:08];
687:BS tx_data_st = rd_buf1[23:16];
684:BS tx_data_st = rd_buf0[31:24];
685:BS tx_data_st = rd_buf1[07:00];
681:BS tx_data_st = rd_buf0[07:00];
688:BS tx_data_st = rd_buf1[31:24];
683:BS tx_data_st = rd_buf0[23:16];
Leaf_679:AL