3 bit Parity Generator

.vhd File Code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity ParityGen is
Port (A: in STD LOGIC VECTOR (2 downto 0);
          ledp : out (3 downto 0);
          ledn : out (3 downto 0));
end ParityGen;
architecture DataFlow_PG of ParityGen is
begin
     ledp <= "0001";
     ledn(0) <= not(A(0));
     ledn(1) <= not(A(1));
     ledn(2) <= not(A(2));
     ledn(3) <= not(A(0) xor A(1) xor A(2));
end DataFlow_PG;
end Behavioral;
```

.ucf File Code

```
Net "led_n<0>" loc = "p132";
Net "led_n<1>" loc = "p131";
Net "led_n<2>" loc = "p130";
Net "led_n<3>" loc = "p128";
Net "led_p<0>" loc = "p126";
Net "led_p<1>" loc = "p133";
Net "led_p<2>" loc = "p135";
Net "led_p<3>" loc = "p137";
Net "A<0>" loc = "p87";
Net "A<1>" loc = "p86";
Net "A<2>" loc = "p85";
```

Simulation and RTL Schematic