SR Flip-Flop

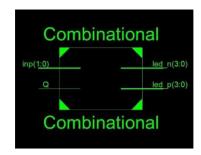
.vhd file code -

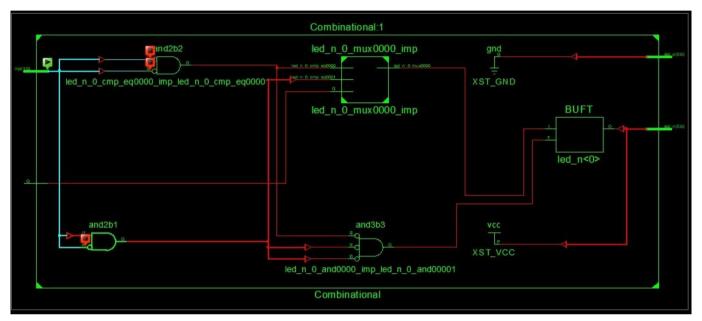
```
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
entity Combinational is
 Port ( led_p : out STD_LOGIC_VECTOR (3
    downto 0); led n : out STD LOGIC VECTOR
    (3 downto 0); inp : in STD LOGIC VECTOR
    (1 downto 0);
    Q : in STD LOGIC);
end Combinational;
architecture Behavioral of
     Combinational is
begin
     led_p(3 downto 0) <= "0001";</pre>
     led n(3 downto 1) <=</pre>
     "111"; with inp select
     led n(0) <= (not Q) when
     "00", ('1') when "01",
     ('0') when "10",
     'Z' when
others; end
Behavioral;
.ucf File Code -
Net "led n<0>" loc = "p132";
Net "led n<1>" loc = "p131";
Net "led n<2>" loc = "p130";
Net "led_n<3>" loc = "p128";
Net "led_p<0>" loc = "p126";
Net "led_p<1>" loc = "p133";
Net "led p<2>" loc = "p135";
Net "led_p<3>" loc = "p137";
```

Net "inp<0>" loc = "p101";

Net "inp<1>" loc = "p100";

Net "Q" loc = "p97";





Name	Value		ليتبيا	1,000,006 ps	1,000,007 ps	1,000,008 ps	1,000,009 ps	1,000,010 ps	1,000,011 ps	1,000,012 ps	1,000,013 ps	1,000,014 ps	1,000,015 ps
▶ 😽 led_p[3:0]	0001	2						0001					
 ■ led_p[3:0] ■ led_n[3:0] ■ led_n[3:0] 	1111							1111					
▶ 臂 inp[1:0]	01							01					
₽ q	1	Ī									ME THE WAY		



Hold - inp=11; Q=0



Invalid - Q=0; inp=00



Set - inp=10; Q=1

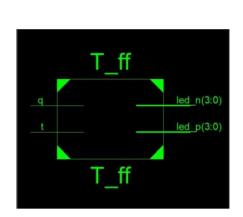


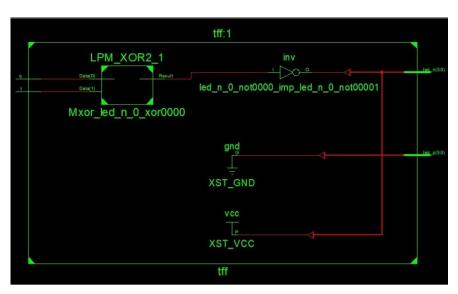
Reset - inp=01; Q=1

T Flip-Flop

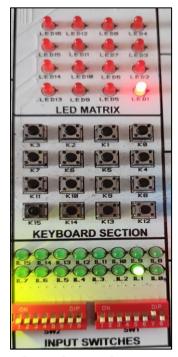
.vhd file Code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity T_ff is
  Port (t : in STD LOGIC; q : in STD LOGIC;
     led p : out STD LOGIC VECTOR (3 downto 0);
     led n : out STD LOGIC VECTOR (3 downto 0));
end T ff;
architecture Behavioral of T_ff is
begin
  led p(3 downto 0) <= "0001";</pre>
  led_n(3 downto 1) \leftarrow "111"; led_n(0) \leftarrow not(t xor q);
end Behavioral;
.ucf file code
Net "led_n<0>" loc = "p132";
Net "led_n<1>" loc = "p131";
Net "led_n<2>" loc = "p130";
Net "led_n<3>" loc = "p128";
Net "led_p<0>" loc = "p126";
Net "led_p<1>" loc = "p133";
Net "led_p<2>" loc = "p135";
Net "led_p<3>" loc = "p137";
Net "t" loc = "p101";
Net "t" loc = "p100";
```

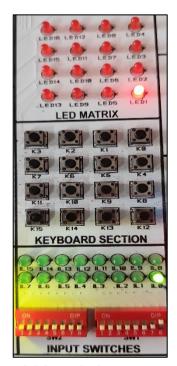




Name	Value	يسلا	1,999,992 ps	1,999,993 ps	1,999,994 ps	1,999,995 ps	1,999,996 ps	1,999,997 ps	1,999,998 ps	1,999,999 ps
t t	0									
In q → " led_p[3:0] → " led_n[3:0]	1									
	0001					0001		,		
	1110					1110		Part of the last		$\models = \mid$
		1							7	



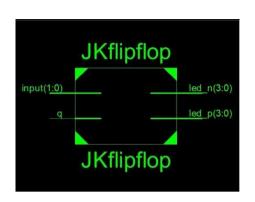
HOLD - Q=1; T=0

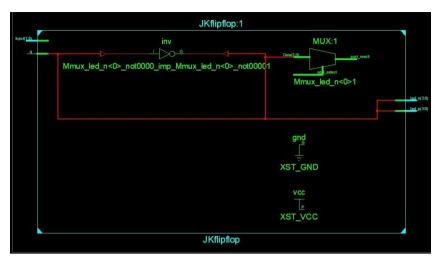


TOGGLE - Q=0; T=1

```
JK Flip-Flop
.vhd file Code
```

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity JK FF is
 Port (inp : in STD_LOGIC_VECTOR(1 downto 0);
     Q : in STD_LOGIC;
     led n : out STD LOGIC VECTOR(3 downto 0);
     led p : out STD LOGIC VECTOR(3 downto 0));
end JK FF;
architecture Behavioral of JK_FF
is
begin
led n (3 downto 1) <= "111";</pre>
led p (3 downto 0) <= "0001";</pre>
with inp select
     led n(0) \leftarrow (not Q)
     when "00", ('0') when
     "01",
     ('1') when "10",
     (Q) when
     "11", 'Z'
     when others;
end Behavioral;
.ucf file Code
Net "led n<0>" loc = "p132";
Net "led_n<1>" loc = "p131";
Net "led_n<2>" loc = "p130";
Net "led_n<3>" loc = "p128";
Net "led_p<0>" loc = "p126";
Net "led_p<1>" loc = "p133";
Net "led_p<2>" loc = "p135";
Net "led p<3>" loc = "p137";
Net "inp<0>" loc = "p101";
Net "inp<1>" loc = "p100";
Net "Q" loc = "p97";
```





Name	Value	diir	1,999,992 ps	1,999,993 ps	1,999,994 ps	1,999,995 ps	1,999,996 ps	1,999,997 ps	1,999,998 ps	1,999,999 ps
▶ 🕌 inp[1:0]	01					01				
l <mark>a</mark> q	1									
▶ 👫 led_n[3:0]	1110					1110				
▶ 👫 led_p[3:0]	0001					0001				



HOLD - inp=00; Q=1



TOGGLE - inp=11; Q=0



TOGGLE - inp=11; Q=1



RESET – inp = 01; Q = 1



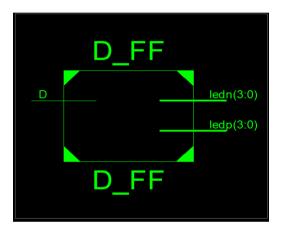
SET - inp = 10; Q = 0

D FF.vhd

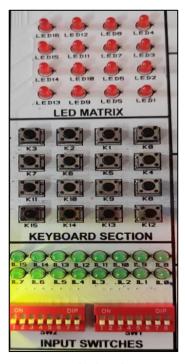
Net "D" loc = "p87";

```
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
entity D_FF is
Port (led n : out STD LOGIC VECTOR (3 downto 0);
    led p : out STD LOGIC VECTOR (3 downto 0)
    D : in STD LOGIC);
end D_FF;
architecture Behavioral of D FF is
begin
     led_n (3 downto 1) <= "111";</pre>
     led_p (3 downto 0) <= "0001";</pre>
     process(D)
       begin
         led_n(0) <=
     not(D); end
     process;
end behavioral;
D FF.ucf
Net "led_n<0>"
                loc = "p132";
Net "led n<1>"
                loc = "p131";
Net "led_n<2>"
                loc = "p130";
Net "led n<3>"
                loc = "p128";
Net
    "led_p<0>"
                loc = "p126";
Net "led p<1>"
                loc = "p133";
Net "led_p<2>"
                loc = "p135";
Net "led p<3>"
                loc = "p137";
```

Name	Value		1,999,992 ps	1,999,993 ps	1,999,994 ps	1,999,995 ps	1,999,996 ps	1,999,997 ps	1,999,998 ps	1,999,999 ps
▶ 😽 ledp[3:0]	0001					0001				
▶ 😽 ledn[3:0]	1110					1110				
¼ d	1									
Name	Value	1	3,999,992 ps	3,999,993 ps	3,999,994 ps	3,999,995 ps	3,999,996 ps	3,999,997 ps	3,999,998 ps	3,999,999 ps
▶ 🖷 ledp[3:0]	0001					0001				
Iedn[3:0]	1111					1111				
¼ d	0									
_										







D = 0; Q = 0