

Mealy Machine

.vhd File Code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity mealmachine is
    Port ( led_p : out  STD_LOGIC_VECTOR (3 downto 0);
          led_n : out  STD_LOGIC_VECTOR (3 downto 0);
          x : in  STD_LOGIC;
          DIS: out STD_LOGIC_VECTOR (1 downto 0);
          SEG: out STD_LOGIC_VECTOR (6 downto 0);
          y : in  STD_LOGIC_VECTOR (1 downto 0));
end mealmachine;

architecture Behavioral of mealmachine is
begin
    led_n (3 downto 2) <= "11";
    led_p (3 downto 0) <= "0001";
    DIS <= "01";
    process (x,y)
    begin
        led_n (1) <=  not ((not y (0)) and x);
        led_n (0) <= not ((y(0) or y(1)) and x);

        if (y = "00") then
            if (x = '0') then
                SEG <= "1000000";
            else
                SEG <= "1000000";
            end if;
        end if;
    end if;
end if;
```

```

if (y = "01") then
    if (x = '0')then
        SEG <= "1111001";
    else
        SEG <= "1000000";
    end if;
end if;
if (y = "10") then
    if (x = '0')then
        SEG <= "1111001";
    else
        SEG <= "1000000";
    end if;
end if;
if (y = "11") then
    if (x = '0')then
        SEG <= "1111001";
    else
        SEG <= "1000000";
    end if;
end if;
    end process;
end Behavioral;

```

.ucf File Code

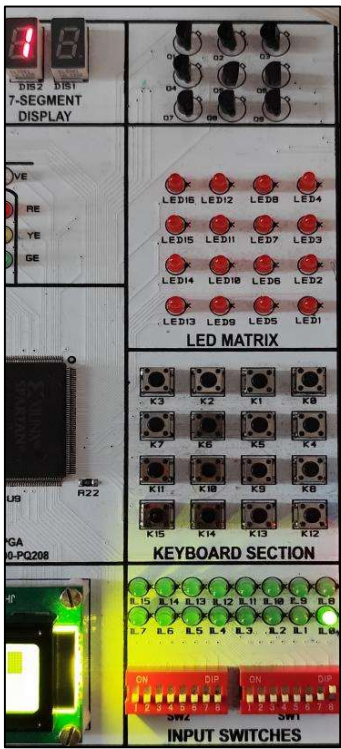
```

Net "led_n<0>" loc = "p132";
Net "led_n<1>" loc = "p131";
Net "led_n<2>" loc = "p130";
Net "led_n<3>" loc = "p128";
Net "led_p<0>" loc = "p126";
Net "led_p<1>" loc = "p133";
Net "led_p<2>" loc = "p135";

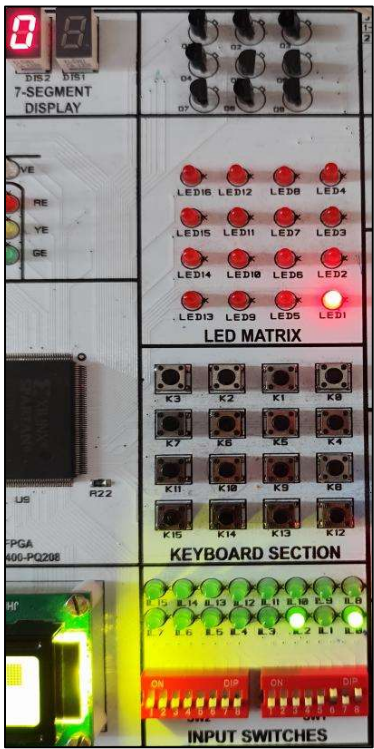
```

```
Net "led_p<3>" loc = "p137";
Net "A<0>" loc = "p87";
Net "A<1>" loc = "p86";
Net "A<2>" loc = "p85";
```

Kit Output:

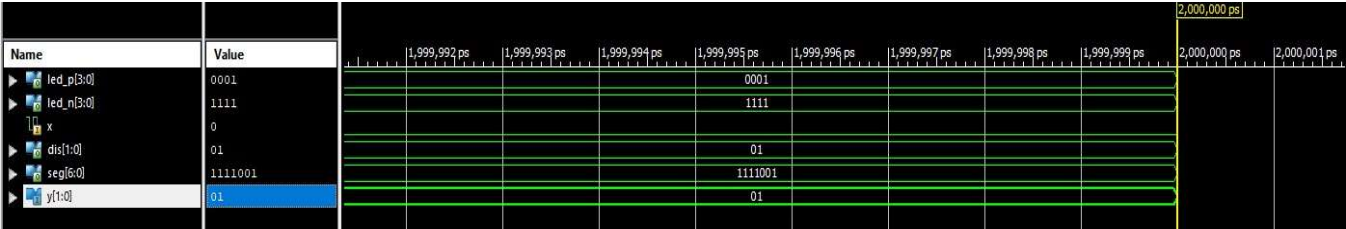


x=0; y1=0; y0=1
O/P – 1



x=1; y1=0; y0=1
O/P - 0

Simulation and RTL Schematic



mealymachine

