SR Flip-Flop

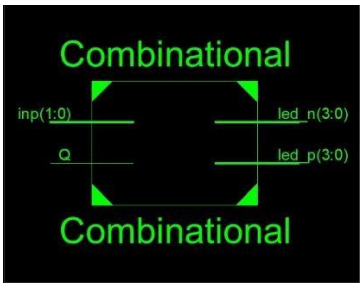
.vhd file code -

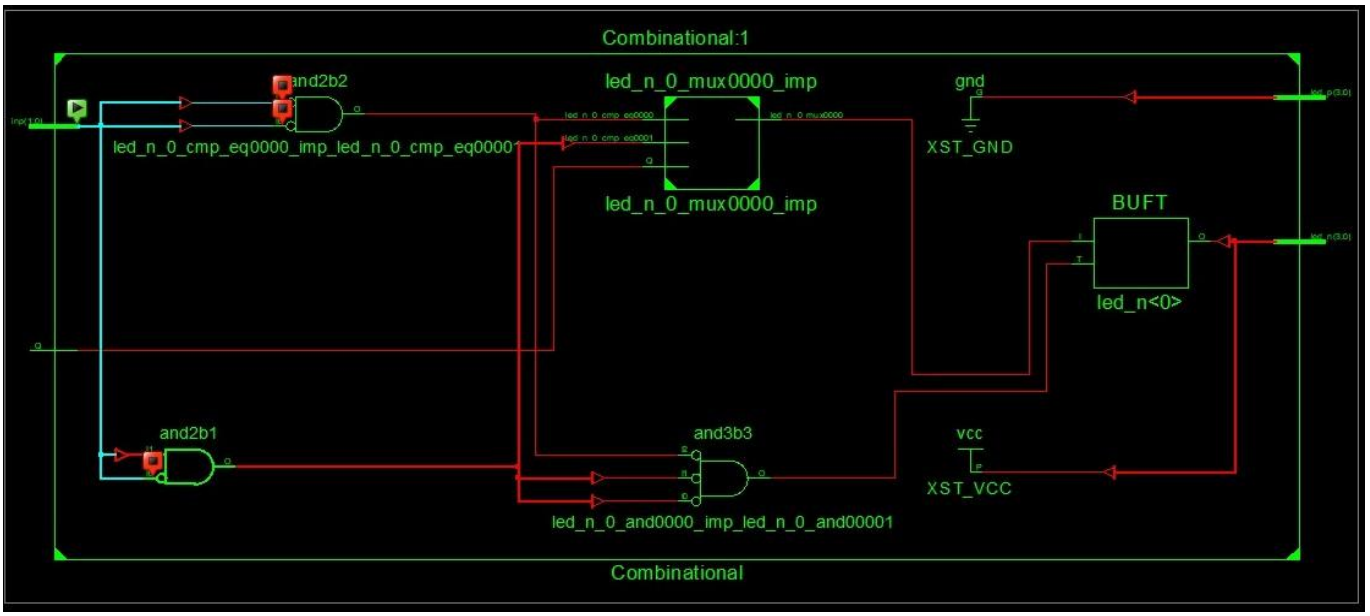
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Combinational is
  Port ( led_p : out  STD_LOGIC_VECTOR (3
     downto 0); led_n : out  STD_LOGIC_VECTOR
     (3 downto 0); inp : in STD_LOGIC_VECTOR
     (1 downto 0);
     Q : in  STD_LOGIC);
end Combinational;
architecture Behavioral of
      Combinational is
begin
      led_p(3 downto 0) <= "0001";
      led_n(3 downto 1) <=
      "111"; with inp select
      led_n(0) <= (not Q) when
      "00", ('1') when "01",
      ('0') when "10",
      'Z' when
others; end
Behavioral;
```

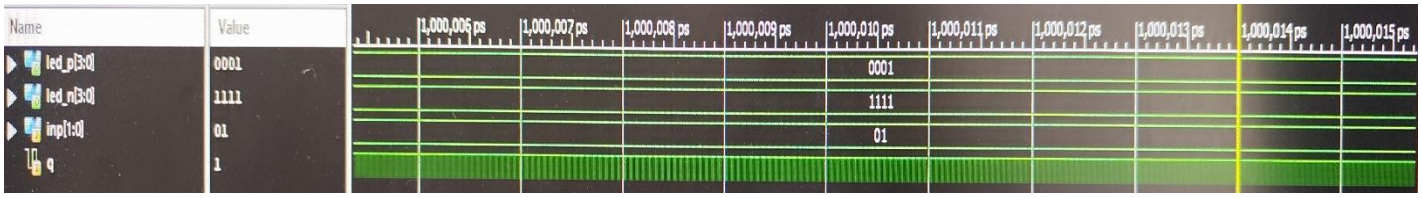
.ucf File Code –

```
Net “led_n<0>” loc = “p132”;
Net “led_n<1>” loc = “p131”;
Net “led_n<2>” loc = “p130”;
Net “led_n<3>” loc = “p128”;
Net “led_p<0>” loc = “p126”;
Net “led_p<1>” loc = “p133”;
Net “led_p<2>” loc = “p135”;
Net “led_p<3>” loc = “p137”;
Net “inp<0>” loc = “p101”;
Net “inp<1>” loc = “p100”;
Net “Q” loc = “p97”;
```

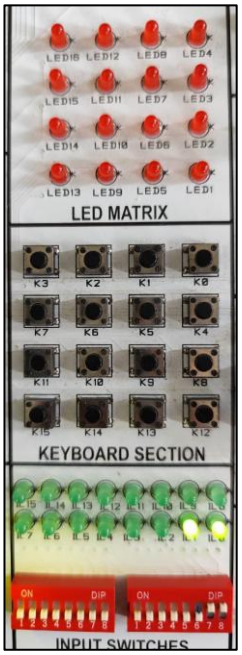
Simulation and RTL Schematic



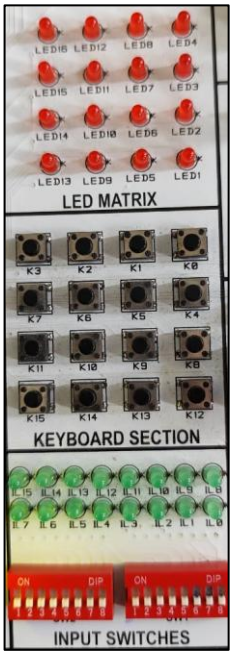




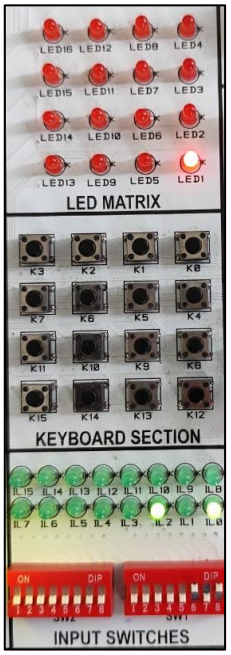
Kit Output:



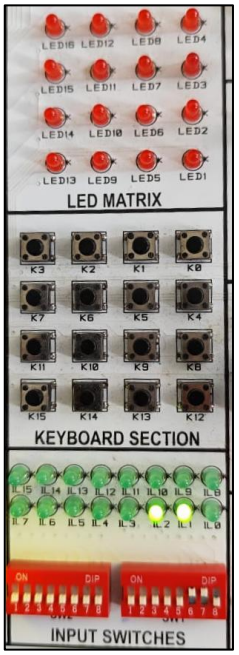
Hold – inp=11; Q=0



Invalid – Q=0; inp=00



Set – inp=10; Q=1



Reset – inp=01; Q=1

T Flip-Flop

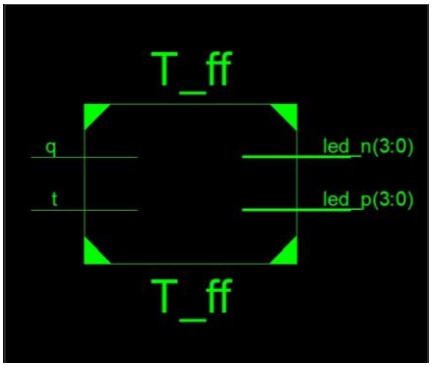
.vhd file Code

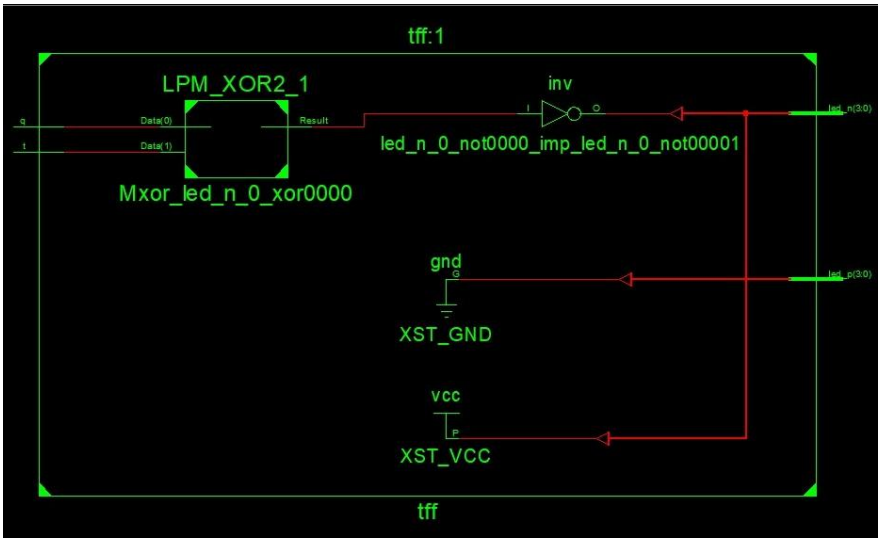
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity T_ff is
  Port (t : in STD_LOGIC; q : in STD_LOGIC;
     led_p : out STD_LOGIC_VECTOR (3 downto 0);
     led_n : out STD_LOGIC_VECTOR (3 downto 0));
end T_ff;
architecture Behavioral of T_ff is
begin
  led_p(3 downto 0) <= "0001";
  led_n(3 downto 1) <= "111"; led_n(0) <= not(t xor q);
end Behavioral;
```

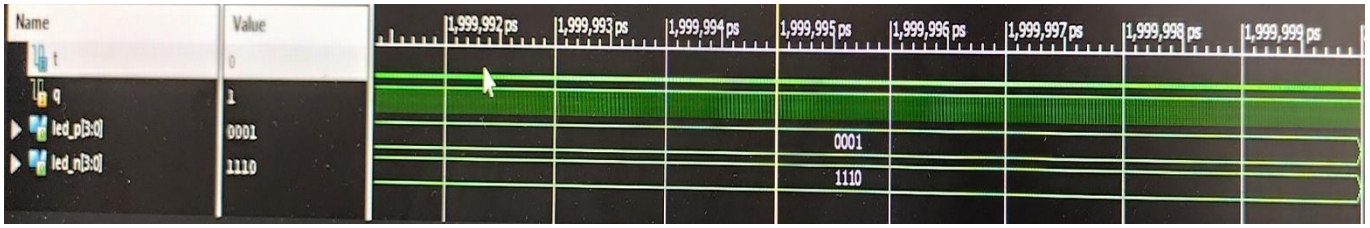
.ucf file code

```
Net “led_n<0>” loc = “p132”;
Net “led_n<1>” loc = “p131”;
Net “led_n<2>” loc = “p130”;
Net “led_n<3>” loc = “p128”;
Net “led_p<0>” loc = “p126”;
Net “led_p<1>” loc = “p133”;
Net “led_p<2>” loc = “p135”;
Net “led_p<3>” loc = “p137”;
Net “t” loc = “p101”;
Net “t” loc = “p100”;
```

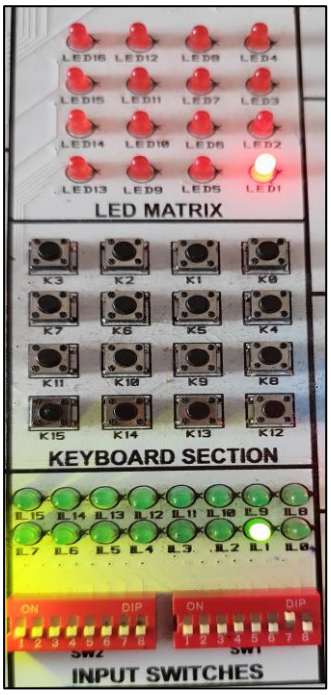
Simulation and RTL Schematic



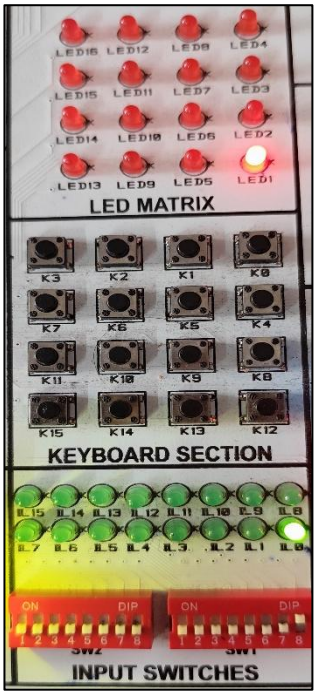




Kit Output:



HOLD - Q=1; T=0



TOGGLE - Q=0; T=1

JK Flip-Flop

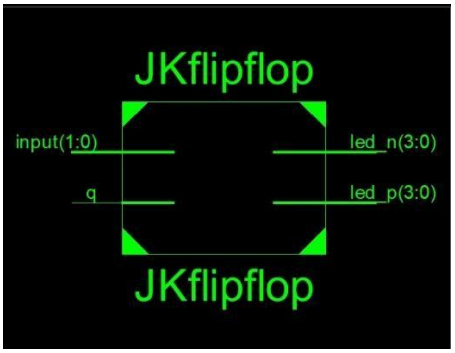
.vhd file Code

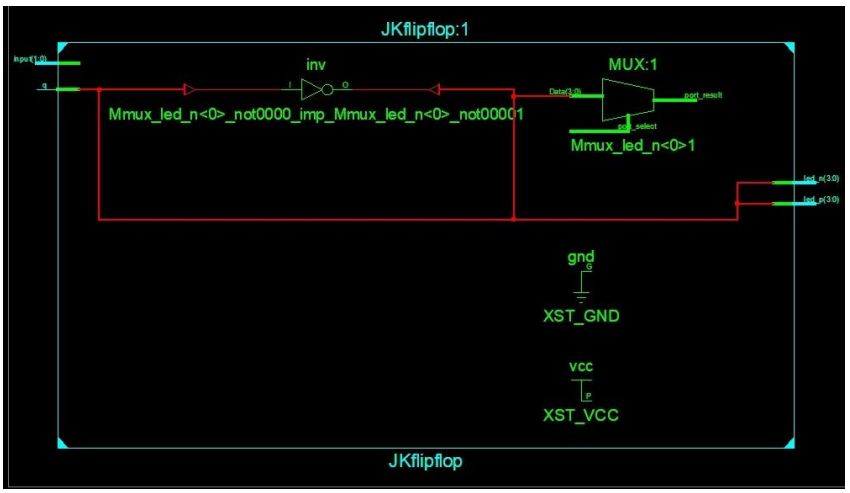
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity JK_FF is
  Port (inp : in STD_LOGIC_VECTOR(1 downto 0);
      Q : in STD_LOGIC;
      led_n : out STD_LOGIC_VECTOR(3 downto 0);
      led_p : out  STD_LOGIC_VECTOR(3 downto 0));
end JK_FF;
architecture Behavioral of JK_FF
is
begin
led_n (3 downto 1) <= “111”;
led_p (3 downto 0) <= “0001”;
with inp select
      led_n(0) <= (not Q)
      when “00”, ('0') when
      "01",
      ('1') when "10",
      (Q) when
      "11", 'Z'
      when others;
end Behavioral;
```

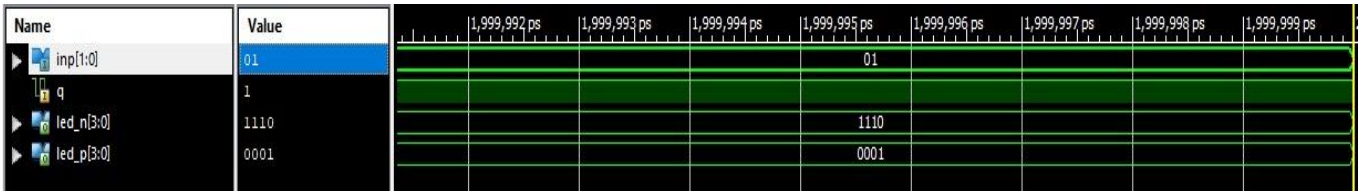
.ucf file Code

```
Net “led_n<0>” loc = “p132”;
Net “led_n<1>” loc = “p131”;
Net “led_n<2>” loc = “p130”;
Net “led_n<3>” loc = “p128”;
Net “led_p<0>” loc = “p126”;
Net “led_p<1>” loc = “p133”;
Net “led_p<2>” loc = “p135”;
Net “led_p<3>” loc = “p137”;
Net “inp<0>” loc = “p101”;
Net “inp<1>” loc = “p100”;
Net “Q” loc = “p97”;
```

Simulation and RTL Schematic





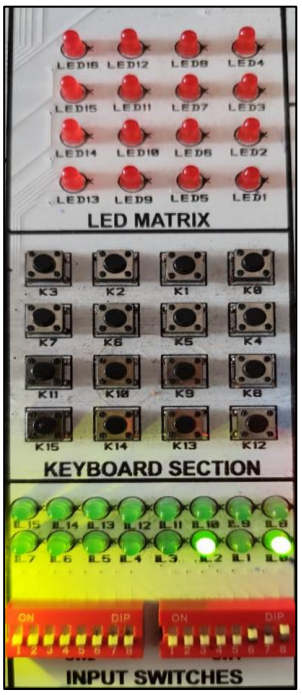


Kit Output:

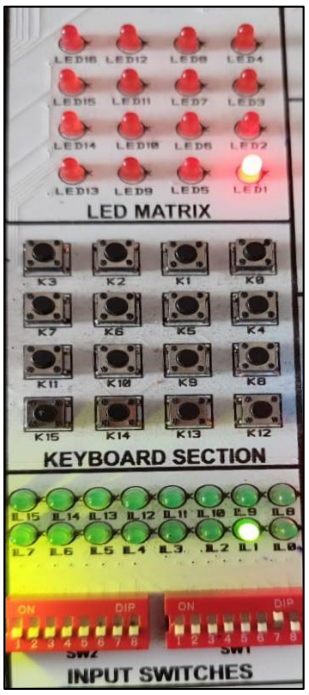
HOLD – inp=00; Q=1

TOGGLE – inp=11; Q=0

TOGGLE – inp=11; Q=1



RESET – inp = 01; Q = 1



SET – inp = 10; Q = 0

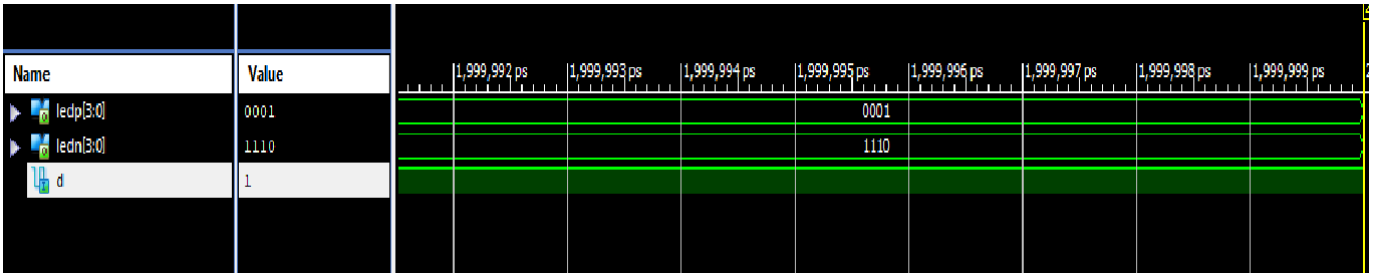
D_FF.vhd

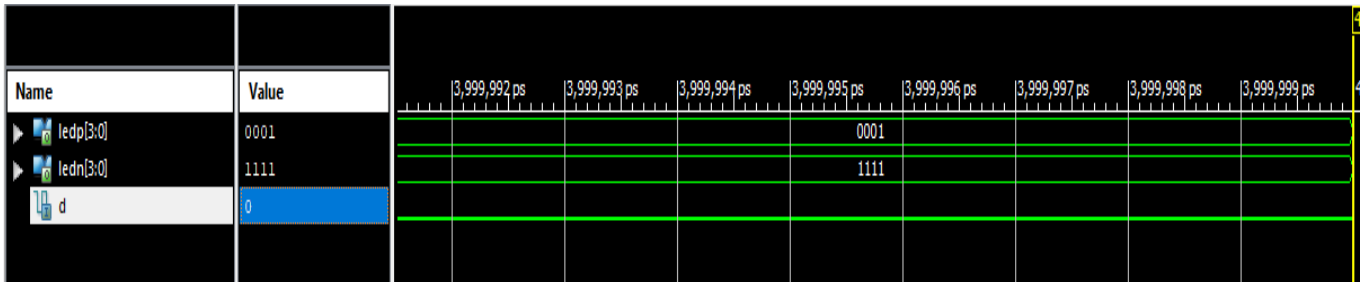
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity D_FF is
Port (led_n : out STD_LOGIC_VECTOR (3 downto 0);
    led_p : out  STD_LOGIC_VECTOR (3 downto 0)
    D : in STD_LOGIC);
end D_FF;
architecture Behavioral of D_FF is
begin
     led_n (3 downto 1) <= “111”;
     led_p (3 downto 0) <= “0001”;
     process(D)
       begin
         led_n(0) <=
     not(D); end
     process;
end behavioral;
```

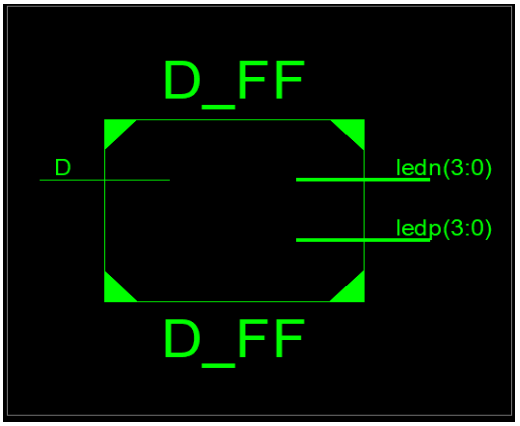
D_FF.ucf

```
Net  “led_n<0>”  loc  =  “p132”;
Net  “led_n<1>”  loc  =  “p131”;
Net  “led_n<2>”  loc  =  “p130”;
Net  “led_n<3>”  loc  =  “p128”;
Net  “led_p<0>”  loc  =  “p126”;
Net  “led_p<1>”  loc  =  “p133”;
Net  “led_p<2>”  loc  =  “p135”;
Net  “led_p<3>”  loc  =  “p137”;
Net “D” loc = “p87”;
```

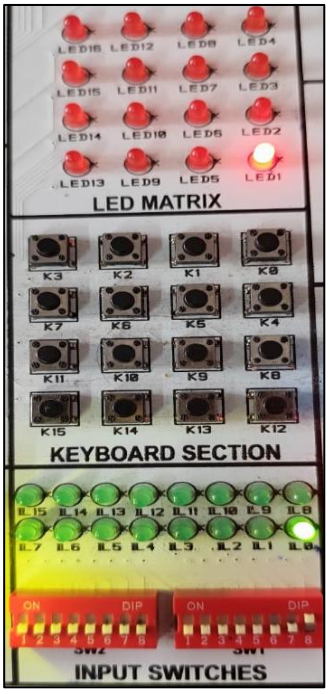
Simulation and RTL Schematic



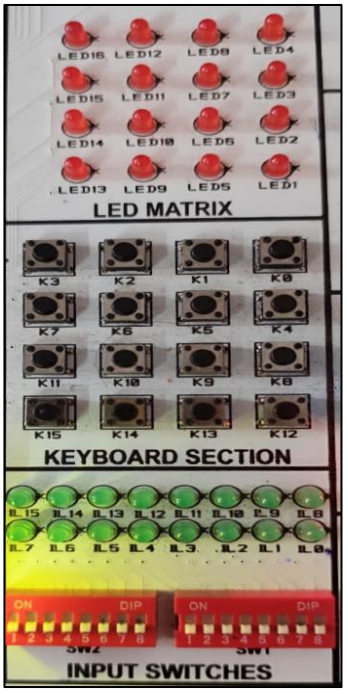




Kit Output:



D = 1; Q = 1



D = 0; Q = 0