

## Coaxial Transceiver Interface

### FEATURES

- Compatible with ISO/IEEE 802.3 10Base5 (Ethernet) and 10Base2 (Cheapernet).
- Functionally compatible with National DP8392C.
- Internal squelch circuitry for noise rejection.
- Reception/transmission mode collision detection.
- Transceiver functions integrated except for signal and power isolation.
- CD heartbeat externally selectable.
- Advanced low-power, high-performance CMOS technology.
- ESD protection greater than 2000 volts.
- 16-pin plastic DIP package, 24-pin skinny plastic DIP package, or 20 and 28-pin PLCC packages.
- Built-in LED drivers for collision, reception, jabber and transmission status display (**MTDX93/X94 only**).
- Collision detection mode for reception, transmission and hybrid (**MTDX94 only**).
- Special test mode allowing continuous transmission for waveform testing (**MTDX94 only**).

### GENERAL DESCRIPTION

The MTD392 family includes a series of products, MTD392/3/4 and MTD492/3/4. The MTD392 product family is built for easy MAU interface in a coaxial Ethernet network. The MTD392 product family integrates the coaxial cable interface functions of Medium Attachment Unit (MAU) in Ethernet or Cheapernet LAN applications. In an Ethernet 10Base5 network, the MTD392 product family is mounted on the thick Ethernet coaxial cable and connects to a station through an AUI cable. For Cheapernet applications, the MTD392 product family is connected to the Cheapernet coaxial cable through a BNC connector and is usually mounted on the LAN adapter in a station.

Following is a table describing the differences among the MTD392 product family:

Product	Features	Package Types	Recommended Applications
MTD392	Basic transceiver	16-PDIP 28-PLCC	Adapter boards
MTD393	MTD392 with built-in LEDs	20-PLCC 24-PDIP	Adapter cards with status LEDs
MTD394	MTD393 with enhanced collision detection mode, special pin for testing	24-PDIP 28-PLCC	MTD393 applications with enhanced collision detection
MTD49X	MTD39X with improved performance		Basic MTD39X applications, Hub, repeater and MAU applications



MTD392  
FAMILY

The diagram illustrates the HBE system architecture, showing the flow of data and control signals between various components. The system is divided into a **TRANSMIT STATE MACHINE** and a **RECEIVE STATE MACHINE**, which are controlled by a **WATCH DOG TIMER 26ms** and a **JABBER RESET TIMER 0.4sec**. The **WATCH DOG TIMER** is clocked by a **10MHz OSC**. The **JABBER RESET TIMER** is triggered by the **WATCH DOG TIMER** and outputs a **XMTSQ** signal to the **DC/AC SQUELCH** block.

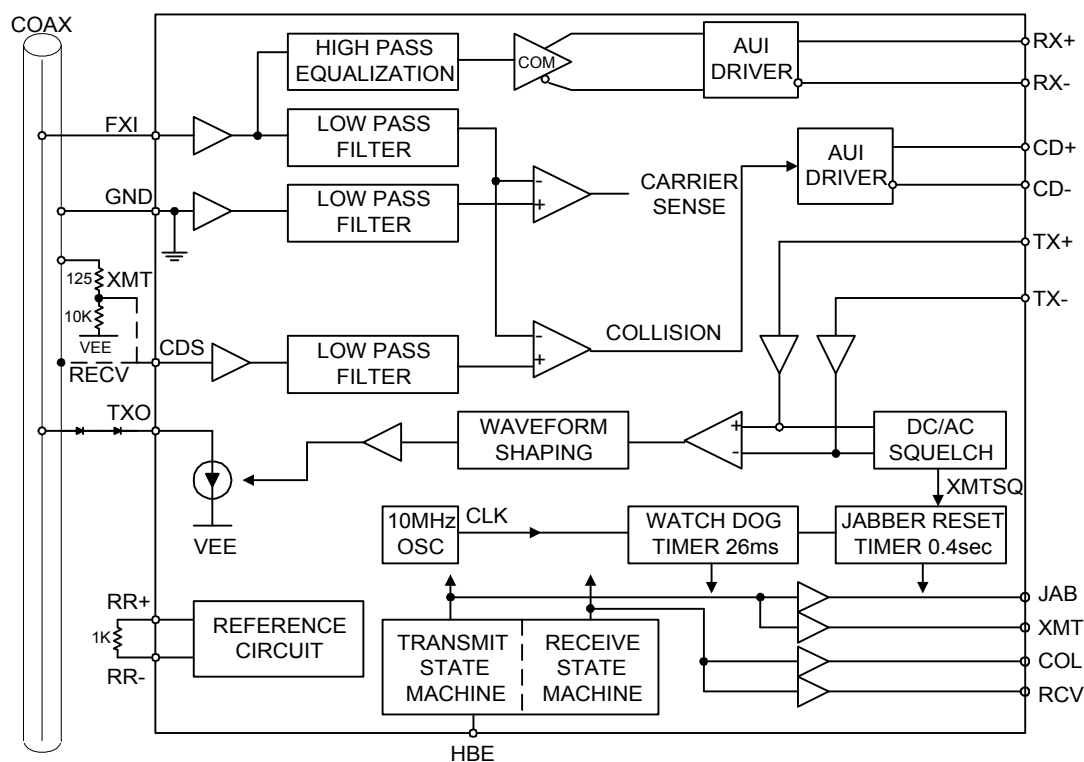
**Transmit Path:** The **TRANSMIT STATE MACHINE** outputs a signal to the **DC/AC SQUELCH** block. The **DC/AC SQUELCH** block also receives a signal from the **WATCH DOG TIMER** and outputs a signal to the **TXO** (Transmit Output) pin. The **TXO** pin is connected to a **TX** pin, which is also connected to a **TX+** and **TX-** differential pair. The **TX** pin is also connected to a **TXO** pin, which is connected to a **TX** pin, which is also connected to a **TX+** and **TX-** differential pair.

**Receive Path:** The **RECEIVE STATE MACHINE** outputs a signal to the **DC/AC SQUELCH** block. The **DC/AC SQUELCH** block also receives a signal from the **WATCH DOG TIMER** and outputs a signal to the **TXO** (Transmit Output) pin. The **TXO** pin is connected to a **TX** pin, which is also connected to a **TX+** and **TX-** differential pair. The **TX** pin is also connected to a **TXO** pin, which is connected to a **TX** pin, which is also connected to a **TX+** and **TX-** differential pair.

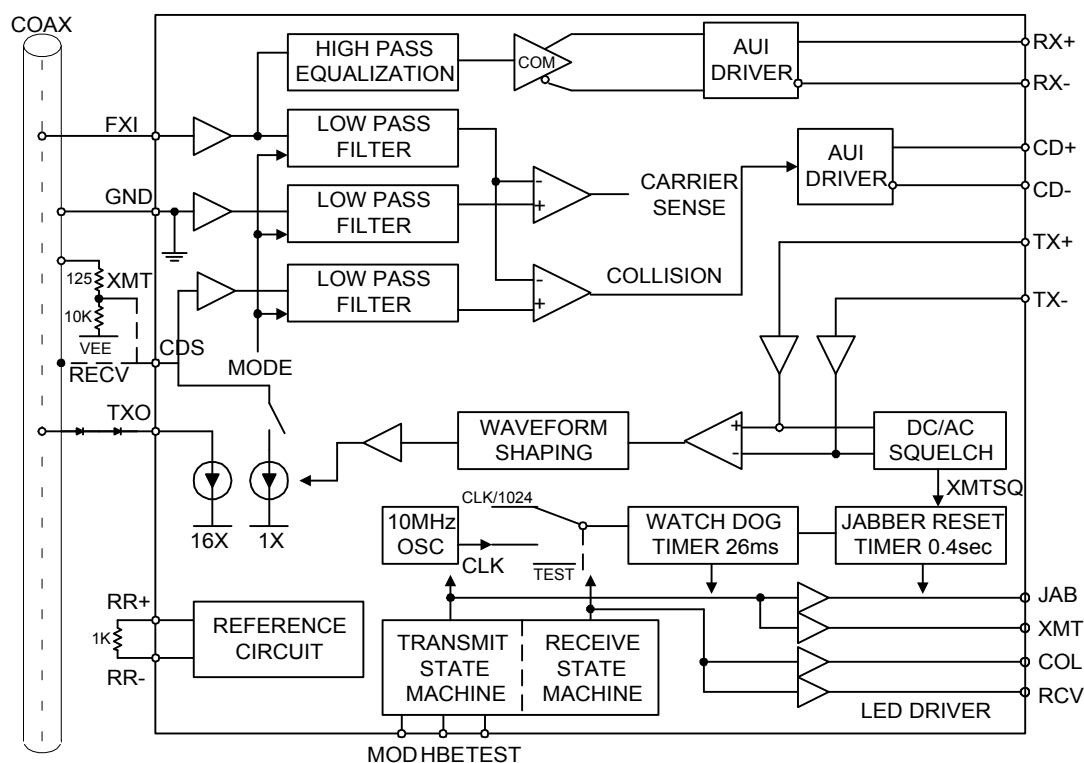
**Control and Timing:** The **WATCH DOG TIMER 26ms** and **JABBER RESET TIMER 0.4sec** are clocked by a **10MHz OSC**. The **JABBER RESET TIMER** outputs a **XMTSQ** signal to the **DC/AC SQUELCH** block. The **DC/AC SQUELCH** block also receives a signal from the **WATCH DOG TIMER** and outputs a signal to the **TXO** (Transmit Output) pin. The **TXO** pin is connected to a **TX** pin, which is also connected to a **TX+** and **TX-** differential pair. The **TX** pin is also connected to a **TXO** pin, which is connected to a **TX** pin, which is also connected to a **TX+** and **TX-** differential pair.

**Other Components:** The **REFERENCE CIRCUIT** is connected to the **RR+** and **RR-** pins. The **REFERENCE CIRCUIT** is also connected to the **RR+** and **RR-** pins. The **REFERENCE CIRCUIT** is also connected to the **RR+** and **RR-** pins. The **REFERENCE CIRCUIT** is also connected to the **RR+** and **RR-** pins.

### Block Diagram for MTDX92



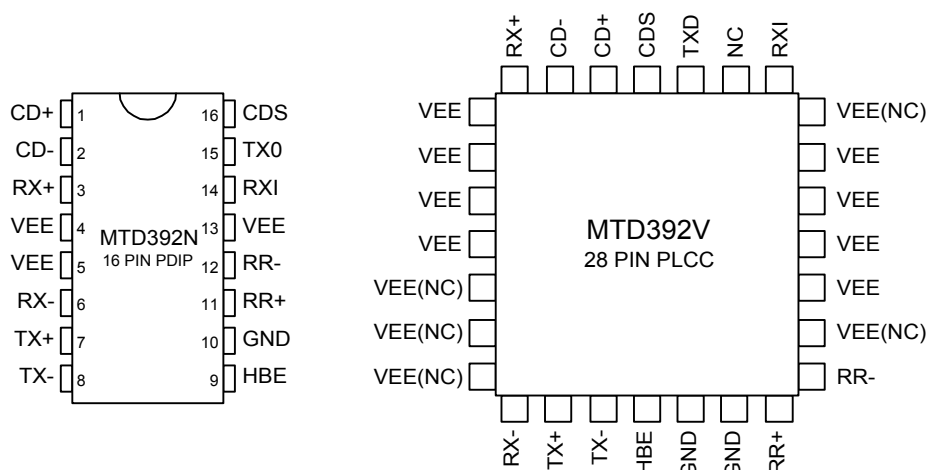
### Block Diagram for MTDX93



### Block Diagram for MTDX94

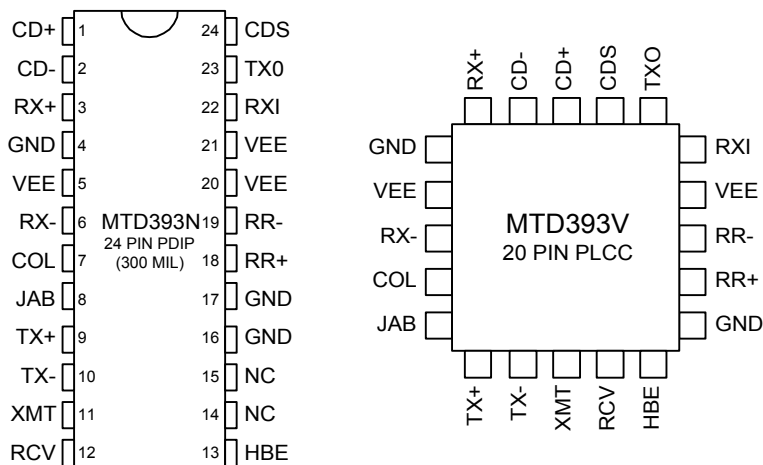
## 1.0 CONNECTION DIAGRAM

### (1) MTDX92 Pin Diagram

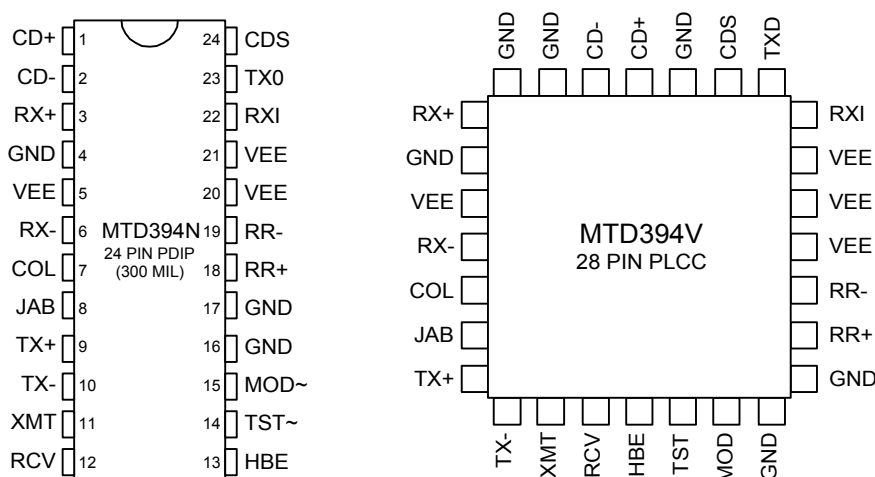




## (2) MTDX93 Pin Diagram

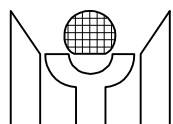


## (3) MTDX94 Pin Diagram

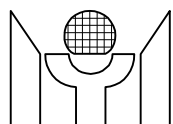


## 2.0 PIN DESCRIPTIONS

Name	I/O	MTD X92 PIN#	MTD X93 PIN#	MTD X94 PIN#	Description
TX+,TX-	I	7 8	9 10	9 10	<b>Transmission Data Input.</b> A balanced differential line receiver that receives input from the off-chip Manchester Code Converter (MCC) to the Transmitter. The common mode voltage on TX± is set internally.
HBE	I	9	13	13	<b>Heartbeat Enabler.</b> The CD heartbeat test is enabled when HBE is connected to Ground and disabled when HBE is connected to VEE.
RR+,RR-	I	11 12	18 19	18 19	<b>External Resistor.</b> A 1kΩ,1% resistor should be connected across these pins to correctly set internal operating currents. RR+ is internally shorted to GND.



RXI	I	14	22	22	<b>Network Receiving Input.</b> Should be connected to the COAX center conductor. Signals meeting receiver squelch limits are recovered and output on RX±/RXI also detects the collision voltage level.
CDS	I	16	24	24	<b>Collision Detecting Sense.</b> Connects directly to the COAX shield, providing a reference for the collision detection voltage level for receiving-mode detection. An external bias network can be used to shift the detection threshold for transmission-detection mode. For hybrid mode collision detection, a 400Ω resistor should be connected from CDS to GND.
RX+,RX-	O	3 6	3 6	3 6	<b>Receiving Data Output.</b> A balanced differential output drives data recovered from the network to the MCC. These outputs are also open sources, and pull-down resistors from 510Ω to VEE are required. To minimize power dissipation, both open source outputs are disabled during idle conditions, allowing the common mode on the pull-down resistor to be pulled to VEE.
CD+,CD-	O	1 2	1 2	1 2	<b>Collision Output.</b> A balanced differential line driver drives this output pair from the collision detection circuitry. A 10MHz signal from the internal oscillator is transferred to these outputs in the event of collision or excessive transmission (jabber), or during heartbeat condition. These outputs are open sources, and pull-down resistors from 510Ω to VEE are required. To minimize power dissipation, both open source outputs are disabled during idle condition, allowing the common mode on the pull-down resistors to be pulled to VEE.
TXO	O	15	23	23	<b>Transmitter Output.</b> Should be connected to the coaxial cable via one serial isolation diode for Cheapernet/Thinnet (10 Base2) or 2 serial isolation diodes for Thicknet (10 Base5).
GND		10	4 16 17	4 16 17	<b>Positive Supply Pin (Ground).</b> Should be connected to the COAX shield.
VEE		4 5 13	5 20 21	5 20 21	<b>Negative Power Supply.</b> -9 volts. A 0.1μF decoupling capacitor must be connected across GND and VEE as close to the device as possible.
COL, JAB, XMT, RCV,	O			7 8 11 12	<b>Transceiver Status Indicators.</b> LED displays for collision, jabber, transmission and reception. These pins are open-drain output buffers that are used to drive LED status indicators. They are designed to supply 8 mA sinking capability.
TST-	I			14	<b>Test Enabler.</b> When both TST- and MOD- pins are shorted to VEE, MTDX94 enters into test mode. In this mode, the jabber function is disabled and all state timing is accelerated by 1024 times. This pin has a 50kΩ internal pull-up resistor.
MOD-	I			15	<b>Mode Selection.</b> Along with the TST- pin, determines the collision detection method of MTDX94. If both MOD- and TST- are connected to GND, MTDX94 implements receiving-mode collision detection. The typical detection threshold in receiving-mode is -1.53V. To implement transmission-mode collision detection, the detection threshold can be lowered by placing a resistor bias network on the CDS pin. When the TST- pin is connected to GND and the MOD- pin is connected to VEE, MTDX94 uses hybrid-mode for collision detection. In this mode, the threshold is set at -0.42V during idle or



					receiving operation. During transmission, the detection threshold is increased to -0.42V plus its own transmission level on the CDS pin. When TST- is connected to VEE and MOD- is connected to GND, MTDX94 uses the transmit-hybrid mode for collision detection. This mode is identical to hybrid-mode, except that during idle or receiving operation, the detection threshold is set at -1.53V. For proper operation of hybrid and transmission-hybrid mode, a 400 $\Omega$ resistor should be connected between the CDS pin and GND. This pin has a 50 k $\Omega$ internal pull-up resistor.
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### 3.0 ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (VEE)	-12V
Input Voltage	GND+0.3 to VEE-0.3V
Storage Temperature	-65° to 150°C
Ambient Operating Temperature	0° to 70°C
ESD Protection except RXI	2000V

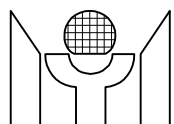
### 4.0 OPERATING CONDITIONS

DC Supply Voltage (VEE)	8.55-9.45V
Operating Temperature	0° to 70°C

### 5.0 ELECTRICAL CHARACTERISTICS (under operating conditions) (Note 1)

Parameter	Symbol	Min	Typ	Max	Unit
Recommended Supply Voltage	VEE	-8.55	-9.0	-9.45	V
Non-transmitting Supply Current (VEE to GND)	IEE	-	-25	-35	mA
Transmission		-	-70	-80	mA
Receiving Input Bias Current (RXI)	I <sub>rx</sub>	-2	-	+25	$\mu$ A
Transmitting Output DC Current (TXO)	I <sub>tdc</sub>	37	41	45	mA
Transmitting Output AC Current (TXO)	I <sub>tac</sub>	$\pm$ 28	-	I <sub>tdc</sub>	mA
Collision Threshold (Receiving Mode)	V <sub>cd</sub>	-1.45	-1.53	-1.62	V
Collision Threshold (Hybrid Mode) (MTDX94 only)	V <sub>hcd</sub>	-0.38	-0.45	-0.52	V
Carrier Sense Threshold (RXI)	V <sub>cs</sub>	-0.38	-0.45	-0.52	V
Differential Output Voltage (RX $\pm$ , CD $\pm$ )	V <sub>od</sub>	$\pm$ 500	-	$\pm$ 1500	mV
DC Common Mode Output Voltage (RX $\pm$ , CD $\pm$ ) (Note2)	V <sub>oc</sub>	-1.0	-2.0	-3.0	V
Idle State Differential Offset Voltage (RX $\pm$ , CD $\pm$ )	V <sub>ob</sub>	-	0	$\pm$ 40	mV
Transmission Squelch Threshold (TX $\pm$ ) (Note 3)	V <sub>ts</sub>	-175	-225	-300	mV
Input Capacitance (RXI)	C <sub>x</sub>	-	1.5	-	pF
Shunt Resistance-Non-transmitting	R <sub>rx</sub>	100	-	-	k $\Omega$
Shunt Resistance-Transmitting	R <sub>tx</sub>	10	-	-	k $\Omega$

- Notes: 1. Testing is done under the testing load defined in Figure 6.  
2. During idle condition, V<sub>oc</sub> is pulled down to VEE to minimize the power dissipation across the load resistors connected to RX $\pm$  and CD $\pm$  pins.  
3. For a minimum pulse width of  $\geq$ 40 ns.



## 6.0 SWITCHING CHARACTERISTICS (under operating conditions) (Note 1)

Parameter	Symbol	Min	Typ	Max	Unit
Receiving Start-up Delay (RXI to RX $\pm$ )	T <sub>ron</sub>	-	2.5	5	bits
Receiving Propagation Delay (RXI to RX $\pm$ )	T <sub>rd</sub>	-	25	50	ns
Differential Output Rise Time (RX $\pm$ , CD $\pm$ )	T <sub>rr</sub>	-	4	7	ns
Differential Output Fall Time (RX $\pm$ , CD $\pm$ )	T <sub>rf</sub>	-	4	7	ns
Reception and Cable Total Jitter	T <sub>rj</sub>	-	$\pm 2$	-	ns
Transmission Start-up Delay	T <sub>tst</sub>	-	1	2	bits
Transmission Propagation Delay	T <sub>td</sub>	-	25	50	ns
Transmission Rise Time (10%-90%) (TXO)	T <sub>tr</sub>	20	25	30	ns
Transmission Fall Time (10%-90%) (TXO)	T <sub>tf</sub>	20	25	30	ns
T <sub>tr</sub> and T <sub>rf</sub> Mismatch	T <sub>tm</sub>	-	$\pm 0.5$	$\pm 3.0$	ns
Transmission Skew(TXO)	T <sub>ts</sub>	-	$\pm 0.5$	$\pm 2$	ns
Transmission Turn-on Pulse Width at V <sub>ts</sub> (TX+) (Note 4)	T <sub>ton</sub>	10	20	40	ns
Transmission Turn-off Delay	T <sub>toff</sub>	130	200	300	ns
Collision Turn-on Delay	T <sub>con</sub>	-	7	13	bits
Collision Turn-off Delay	T <sub>coff</sub>	-	-	20	bits
Collision Frequency (CD $\pm$ )	F <sub>cp</sub>	8.5	10	12.5	MHz
Collision Pulse Width (CD $\pm$ )	T <sub>cp</sub>	40	50	60	ns
CD Heartbeat Delay (TX $\pm$ to CD $\pm$ )	T <sub>hon</sub>	0.6	1.1	1.6	$\mu$ s
CD Heartbeat Duration(CD $\pm$ )	T <sub>hw</sub>	0.5	1.0	1.5	$\mu$ s
Jabber Activation Delay(TX $\pm$ to CD $\pm$ )	T <sub>ja</sub>	20	26	32	ms
Jabber Reset Timeout (TX $\pm$ to TXO and CD $\pm$ )	T <sub>jr</sub>	300	420	550	ms

Notes: 4. For a minimum pulse amplitude of  $\geq -300$  mV.

## 7.0 TIMING DIAGRAM FOR MTD392 FAMILY

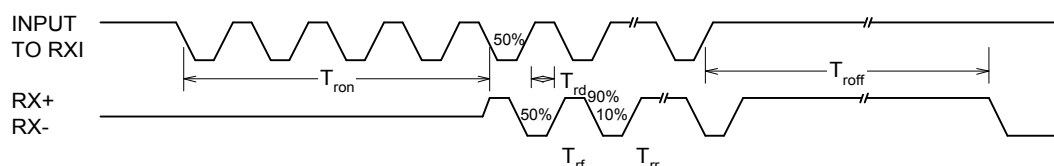


Figure 1. Reception Timing

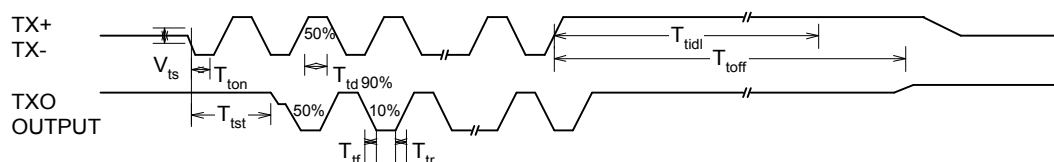


Figure 2. Transmission Timing

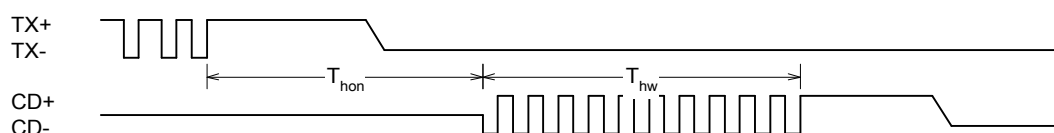


Figure 3. Heartbeat Timing

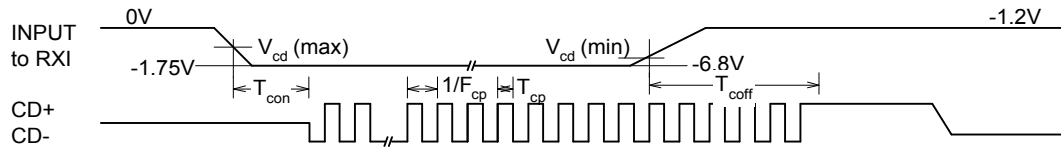
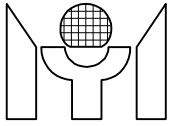


Figure 4. Collision Timing

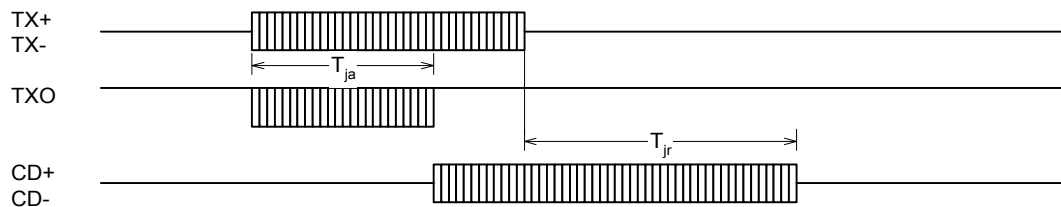


Figure 5. Jabber Timing

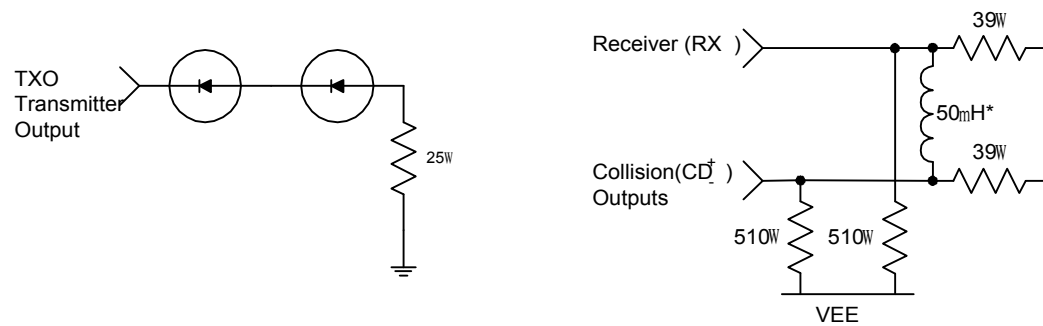
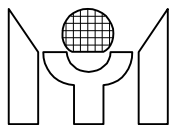


Figure 6. Test Loads

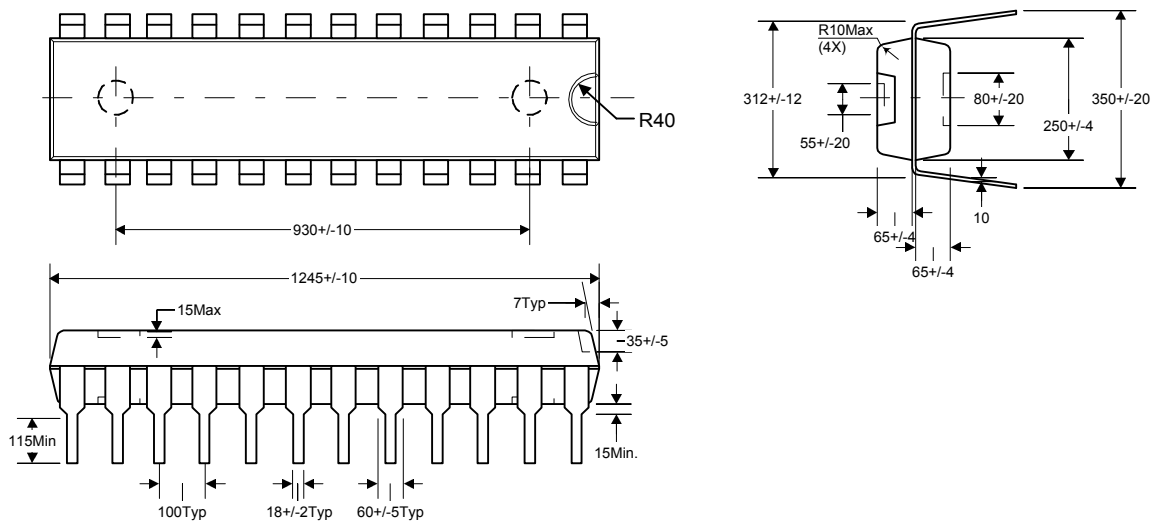




## 8.0 PACKAGE DIMENSION FOR 392 FAMILY

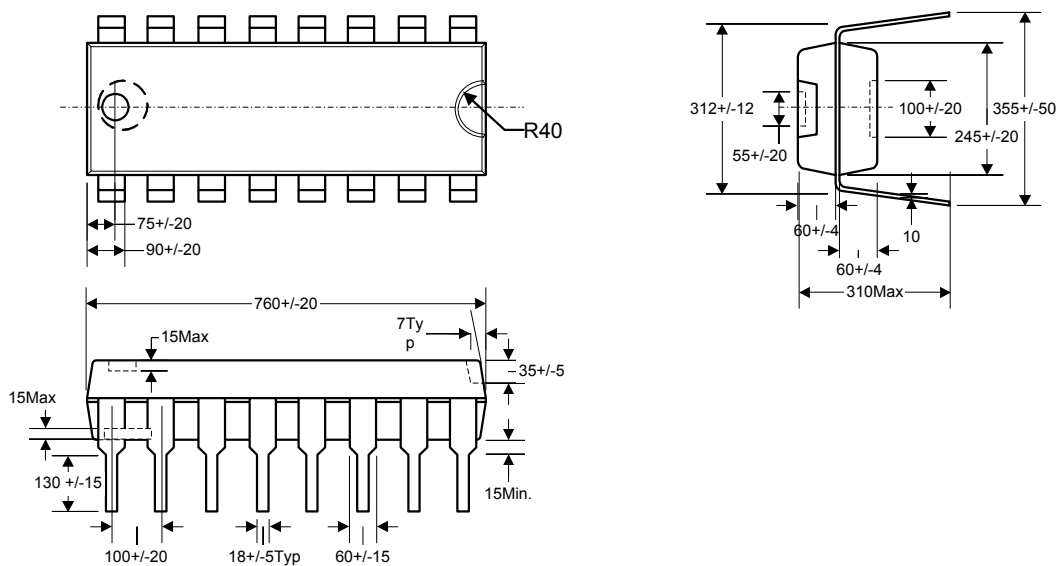
### A. 24-PIN PDIP

UNIT: MIL



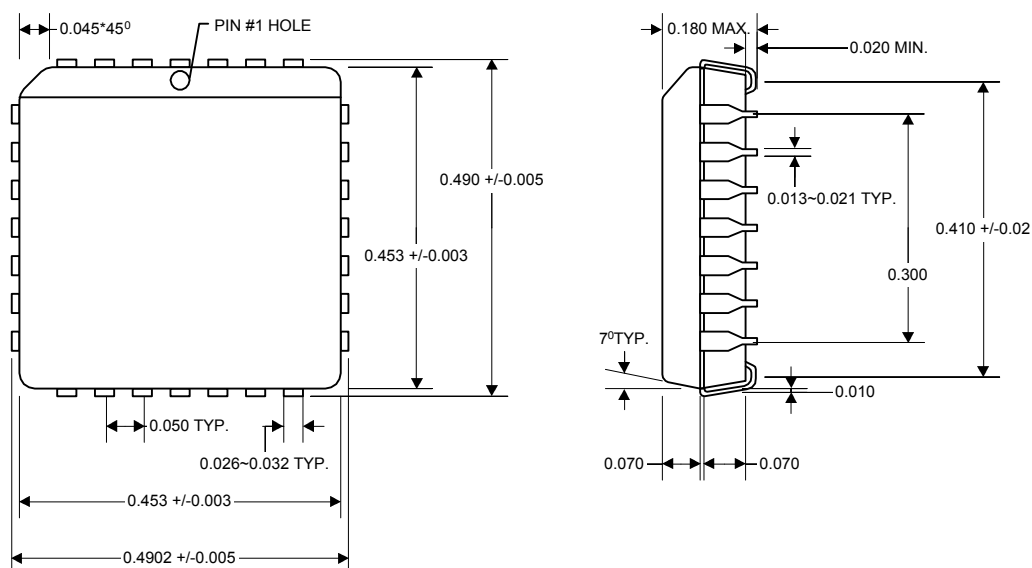
### B. 16-PIN PDIP

UNIT: MIL





## C. 28-PIN PLCC UNIT: INCH



## D. 20-PIN PLCC UNIT: INCH

