J2 MEM_EXT

U2

C7
0.1uF

SST39SF040

C10
22uF

SW1 CONFIG
Switches PnP
RN1

C8
0.1uF

U3 93LC46C

R6
27k

C6
0.1uF

SW2 IRQ
10k 10k
RN2

SW3 IO_ADDR
10k RN4 10k RN3 10k

SW4 ROM_ADDR

JLCJLCJLCJLC

U1   RTL8019AS

ISA 8-bit Ethernet Controller
Version 1.0
Copyright (C) 2021 Sergey Kiselev

C5   C2   R1   C4   R2   R3
0.1uF   10pF   200 0.01uF 470   470

            R7
            1M   Y1 20MHz

            C1
            10pF

C3
0.01uF

J1   RJMG1BD3B8K1ANR

Design files and documentation:
github.com/skiselev/isa8_eth
Licensed under CERN-OHL-S:
https://cern-ohl.web.cern.ch

open source hardware

Designed in Oregon

KiCad
DESIGNED WITH

www.malinov.com

C9
22uF

SW1.1: OFF – Jumperless; ON – Switches
SW1.2: OFF – No PnP; ON – PnP Mode

Card edge pins

5V	5V
NC	A21
NC	A20
NC	A19
MEMW	A18
A17	A16
A14	A15
A13	A12
A8	A7
A9	A6
A11	A5
MEMR	A4
A10	A3
CS	A2
D7	A1
D6	A0
D5	D0
D4	D1
D3	D2
GND	GND

IRQ

IRQ	SW2.1	SW2.2
IRQ2	OFF	OFF
IRQ3	ON	OFF
IRQ4	OFF	ON
IRQ5	ON	ON

I/O Address

I/O Address	SW3.1	SW3.2	SW3.3	SW3.4
0x200	OFF	OFF	OFF	ON
0x220	ON	OFF	OFF	ON
0x240	OFF	ON	OFF	ON
0x260	ON	ON	OFF	ON
0x280	OFF	OFF	ON	ON
0x2A0	ON	OFF	ON	ON
0x2C0	OFF	ON	ON	ON
0x2E0	ON	ON	ON	ON

I/O Address

I/O Address	SW3.1	SW3.2	SW3.3	SW3.4
0x300	OFF	OFF	OFF	OFF
0x320	ON	OFF	OFF	OFF
0x340	OFF	ON	OFF	OFF
0x360	ON	ON	OFF	OFF
0x380	OFF	OFF	ON	OFF
0x3A0	ON	OFF	ON	OFF
0x3C0	OFF	ON	ON	OFF
0x3E0	ON	ON	ON	OFF

ROM Address

ROM Address	ROM Size	SW4.1	SW4.2	SW4.3	SW4.4	SW4.5
Boot ROM Disabled		*	*	*	OFF	OFF
0xC0000	16 KiB	OFF	OFF	OFF	OFF	ON
0xC4000	16 KiB	ON	OFF	OFF	OFF	ON
0xC8000	16 KiB	OFF	ON	OFF	OFF	ON
0xCC000	16 KiB	ON	ON	OFF	OFF	ON
0xD0000	16 KiB	OFF	OFF	ON	OFF	ON
0xD4000	16 KiB	ON	OFF	ON	OFF	ON
0xD8000	16 KiB	OFF	ON	ON	OFF	ON
0xDC000	16 KiB	ON	ON	ON	OFF	ON
0xC0000	32 KiB	OFF	OFF	OFF	ON	OFF
0xC8000	32 KiB	ON	OFF	OFF	ON	OFF
0xD0000	32 KiB	OFF	ON	OFF	ON	OFF
0xD8000	32 KiB	ON	ON	OFF	ON	OFF
0xC0000	64 KiB	OFF	OFF	ON	ON	OFF
0xD0000	64 KiB	ON	OFF	ON	ON	OFF

Note: 16 KiB Page Mode

64 KiB ROM Page Mode