Lab 2

Microwave Circuit Principles and Design

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MICROWAVE AMPLIFER DESIGN

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&

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MICROWAVE TRANSISTOR AMPLIFIERS

For this laboratory it is not assumed that you know a great deal about the transistor, in fact the device will be represented solely by an S-parameter file containing the small signal parameters for a particular transistor bias point, i.e. we will simply assume that the transistor is a black box with the given S-parameters. In reality of course life is not so simple.

In this excise we assume that the transistor has already been properly biased and the amplifier will be executed for a centre frequency of 4 GHz. Both narrow and broadband amplifiers will be designed. Gain and bandwidth are another two parameters will be considered.

The purpose of this laboratory is to design matching stages of amplifiers at the centre frequency of 4 GHz for both narrow and broadband applications. Firstly you need to examine the S-parameters of the transistor. Open the ADS and create project directory. Download the S-parameters (FLC317MG-4.s2p) from Bb9. Save this file to the Data directory under the Project directory.

Since here we will only be considering the small signal performance of the design it is worth noting that this implies that only a linear simulation will be used. For high power amplifier design non-linear models for the transistors will be needed to enable designers to examine the large signal performances.

In ADS, create the schematic for the transistor test as shown in Figure 1. To put the data item in your schematic window, you need to call up a 2-port data item from the **Data Item** palette. Ground the reference port and input should be at Port 1 and output at Port 2. Then double click on the **Data Item** to open it and then **Browse** to the correct file in the Data directory under the Project directory. Then place terminating ports on the input and output as shown in Figure 1. Now save the schematic, for example **Trans_1** and plot the S-parameters from 2 - 6 GHz in 0.5 GHz steps. You can also choose tabular format to show the S-parameters, which are displayed as magnitude and angle unless you specify otherwise.

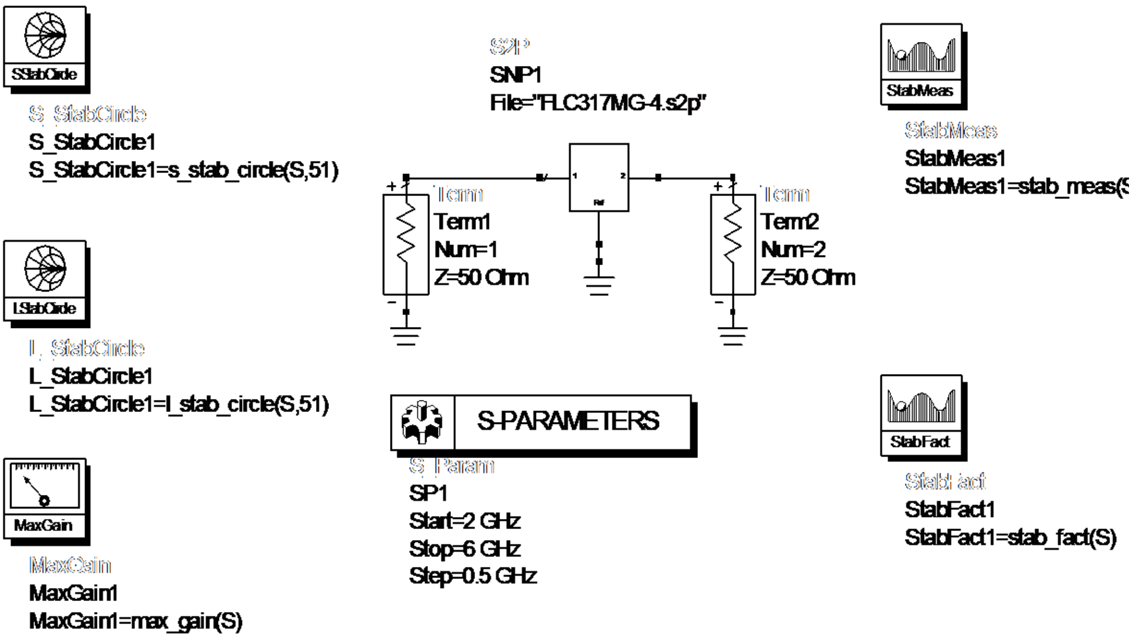

Figure 1 Schematic for the transistor S-parameters.

Usually the choice of transistor is based fundamentally upon the specification that you are required to meet in terms of stability, gain, frequency and power handling. For this laboratory we will assume that you are using the Fujitsu C-Band Power GaAs FET, FLC317MG-4. The S-parameters were measured under DC bias at V_{ds} = 10V and I_d = 720 mA. Notice that the transistor's $P_{out,1dB}$ is ~35dBm or 3W.

STABILITY

The single most important characteristic an amplifier must possess is that it is stable otherwise in designing an amplifier you may inadvertently build an oscillator. To find out if the device is stable you can simply examine the Rollett stability factor ***k*** and the stability measure ***b***. These are particularly useful to gauge stability across a broad bandwidth. It is worth pointing out that just because a transistor is potentially unstable does not mean that it is unusable at that frequency. Simply the bias and matching networks must avoid regions of instability.

The stability factor and stability measure are found in the **Simulation-S_Param** palette as **StabFct** and **StabMs** respectively. The stability factor and measure are best displayed on a linear grid.

Question: At what frequency is this device potentially unstable? Refer to the lecture notes or use **Help** here to check on the values of stability measure and stability factor that guarantee stability, i.e. unconditional stability. You can also see what the stability circles look like by plotting them – these are **S_StabCircle** and **L_StabCircle** which are the source and load stabilities circles. One circle will be plotted for each frequency point. The reality for your design would be that it should be unconditionally stable across all frequency ranges and steps would have to be taken to ensure unstable regions are avoided. Stability can be improved using various techniques, such as through resistive loading but this can have a deleterious effect on achievable gain.

From the S-parameter plots you should see that around 4 GHz the magnitude of S_{11} and S_{22} are less than one and S_{21} is much larger than S_{12} (Why?).

Maximum Transducer/available Gain

In order to see what the maximum transducer/available gain from the transistor is choose the **MaxGain** icon in the **Simulation-S_Param** palette. What is the maximum transducer/available gain this transistor can offer at 4 GHz?

1. NARROWBAND Maximum Transducer/available Gain Amplifier Design

To design maximum amplifier with maximum transducer/available gain, you need to find out the source and load impedance so that both input and output of the transistor can be conjugately matched. To do so, you need to use **SmZl** and **SmZ2** icons in the **Simulation-S_Param** palette. To find the meaning of **SmZl** and **SmZ2** click on the **help** button when these items come up.

These two impedances give the simultaneous input and output matches required to achieve the maximum transducer/available gain **MaxGain.** You can if you'd prefer calculate these in admittance or as reflection coefficient. If the device was unstable then **SmZ1** and **SmZ2** would return zero values. Alternatively one could plot **SmGamma1** and **SmGamma2** (icon is found in the **Simulation-S_Param** palette) in which return the desired reflection coefficients for conjugate matching and can readily be displayed on the Smith Chart.

Simulate and write down two impedances **SmZ1** and **SmZ2** and maximum transducer/available gain at 4 GHz in Table 1. The **SmZ1** and **SmZ2** essentially tell you the conjugate matching impedances needed for the input and output when the device is unconditionally stable. You will need to generate these impedances using (a) ideal transmission line matching networks and (b) microstrip line matching networks, from the 50 Ohm termination. It is best to plot **SmZ1** and **SmZ2** in a table and convert them to real and imaginary values rather than magnitude and angle. To convert the values click on **SmZ1** and **SmZ2** in the table. Then click **Trace Options…** and select **Real/Imaginary** from the menu. These values are in Ohms and are not normalised.

Table 1: Max G_T /G_a and simultaneous Input and Output Impedances at 4 GHz for **FLC317-MG** at Vds = 10V and Id = 720mA

Input Impedance **SmZ1** (Simultaneous Match)	Output Impedance **SmZ2** (Simultaneous Match)	Max G_T /G_a

1.1 Ideal Matching Network Amplifier Design:

You need to generate both input and output matching networks from ideal transmission lines with the usual microstrip limited impedances (10 – 120 Ω). To determine the matching networks required plot the impedances in Table 1 on a Smith Chart. You could do this using ADS. You can find **Smith Chart** in the **Tools.** Use the **Smith Chart** facility and the networks given in Figure 2 to design your matching networks. Check on a Smith Chart what each of these networks does. You need to use each of these networks for both input and output matching, i.e., you need to design three amplifiers that will provide maximum transducer power gain using each of these networks.

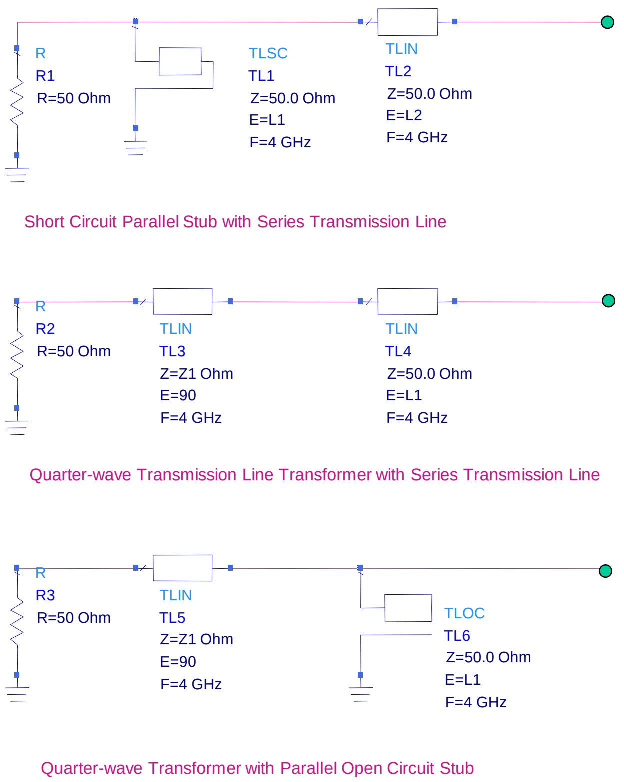

Figure 2 Matching Network Configurations for Narrowband Amplifiers (ideal transmission line networks).

It is worth to point out that you are not simply limited to transmission lines to provide the matching network, capacitors/inductors are equally useful as lumped components so long as you are below the self-resonant frequency although you are only required to use transmission lines to design matching networks in this lab.

Once you have decided on the network you wish to use for input and output check these in new schematics called **input_match** and **output_match** each using a simple 50 Ohm resistor as a representative load and then your network to generate the desired input and output impedance that is to be connected to the transistor in a new schematic called say **fet_match**.

Next re-simulate and optimise for maximum gain at 4 GHz. One option you can use to speed up the process is to do some optimization by hand using the **Tune** facility. To do this either select the **Tune Parameters** icon in the Schematic toolbar or select **Tuning** from the **Simulate** menu. When the tuning window appears select the transmission line for tuning by clicking on it in the schematic window. This item should now appear in the tune window where it may be varied by selecting a tuning step and applying it. For each tune iteration the table of results should be updated. As you improve the gain you should notice that the input and output reflection coefficients are improved. In essence more of the energy is getting into and out of the transistor.

1.2 Microstrip Line Matching Network Amplifier Design:

Once you are happy with the ideal matching network in terms of the impedances and line lengths, you can now convert ONE of the ideal matching networks to microstrip line network. You should now go into **Linecalc** in the **Schematic** and calculate the equivalent line widths and lengths for a RT/Duroid substrate. That is:

Er = 2.20, Cond =5.8×10^{7} Siemens/m, *H* = 20 mil or 0.508 mm, *T* = 0.1 mil or 2.5×10^{-3} mm, Rough = 0.001 and *TanD* = 0.0009.

Again optimise or tune to give a maximum in the gain response at 4 GHz. You should easily be able to achieve a gain that is very close to the ideal maximum gain. Finally plot all the S parameters for your report on a grid over a frequency range from 2 - 6 GHz with a step of 100 MHz. Comment on the bandwidth of your amplifier.

You need to design not only the schematic circuit, but also the layout of the amplifier. You will need to include microstrip tees and steps where appropriate, especially when you convert the schematic circuit into layout. Make sure you also include some 50 Ohm feed lines up to your matching circuits. Go inot **Layout** in the **Schematic** to convert the schematic circuit to PCB layout.

2. Broadband Microstrip Line Matching Network Amplifier Design

This is a slight challenge case - if the amplifier specification was to build a broadband amplifier of 10dB flat gain +/- 0.2 dB from say 3.5 – 4.5 GHz how can this be done? Well inspection of the maximum gain characteristic shows that this is feasible in that the gain is available but the question is how can we see the matching requirement on input and output reflection coefficients? To see the locus of reflection coefficients on the Smith Chart that will yield the desired gain we use the constant gain circles available in ADS under the **Simulation-S_Param** palette. So choosing the two blocks **GaCircle** and **GpCircle** (the transistor is not unilateral) you will be able to plot gain circles directly onto the Smith Chart. Use **Help** to find the means of **GaCircle** and **GpCircle**. In order not to be swamped with plotted data I suggest for plotting the gain circles that you change the frequency sweep to begin at 3.5 GHz and end at 4.5 GHz with a 0.5 GHz step. Then plot **GaCircle1** and **GpCircle1** onto separate Smith Charts.

The available gain circle draws the locus of the gain for a given source mismatch whilst assuming the output is conjugately matched. Any **Γ_S** on the GaCircle will give the constant gain as defiend. For instance, Any **Γ_S** on **GaCircle1=ga_circle(S,10,51)** circles will give the available gain of 10 dB. Similarly the power gain circle assumes that the input is conjugately matched and draws circles on the Smith Chart representing a constant-power-gain circle resulting from a load mismatch. For instance, Any **Γ_L** on **GpCircle1=gp_circle(S,10,51)** circles will give the power gain of 10 dB. Since you have the luxury of stability you can choose which way you approach the problem, either match to the available gain circle at 10dB on the input (In this case, the output is already conjugately matched in 1. Only new **Γ_S** is needed.). Or match to the 10dB power gain circle at the output (In this case, the input is already conjugately matched in 1. Only new **Γ_L** is needed.). You might, however, still need to do a bit tuning on **Γ_S** or **Γ_L** to meet the broadband requirement. If the input or output match network alone can't give the bandwidth you need, you might have to tune both **Γ_S** or **Γ_L**.

To display the available power gain circle use the command in the schematic **GaCircle1=ga_circle(S,10,51)** This will display the 10dB available gain circles. Indicate what **Γ_S** you have chosen before the final tuning.

To display the power gain circle use the command in the schematic **GpCircle1=gp_circle(S,10,51)** This will display the 10dB power gain circles. Indicate what **Γ_L** you have chosen before the final tuning.

Once you've completed this exercise you can now tune up the components you have derived to give a flat gain characteristic across the band from 3.5 – 4.5 GHz. Fine tuning may be more useful and easier here than optimization. If you do optimize you shouldn't allow the values to vary widely (no more than 10%). With a bit of practice you should be able to achieve a gain response at least as good as shown in Figure 3. The data circles indicate the maximum gain achievable and the solid other line is the overall gain S_{21}. In reality this design should firstly be checked across the wide bandwidth of where there is gain for potential instabilities then once corrected it would be converted into microstrip with some thought then given to how the device is to be biased without destroying the gain response and then once the design was complete it could be fabricated and tested.

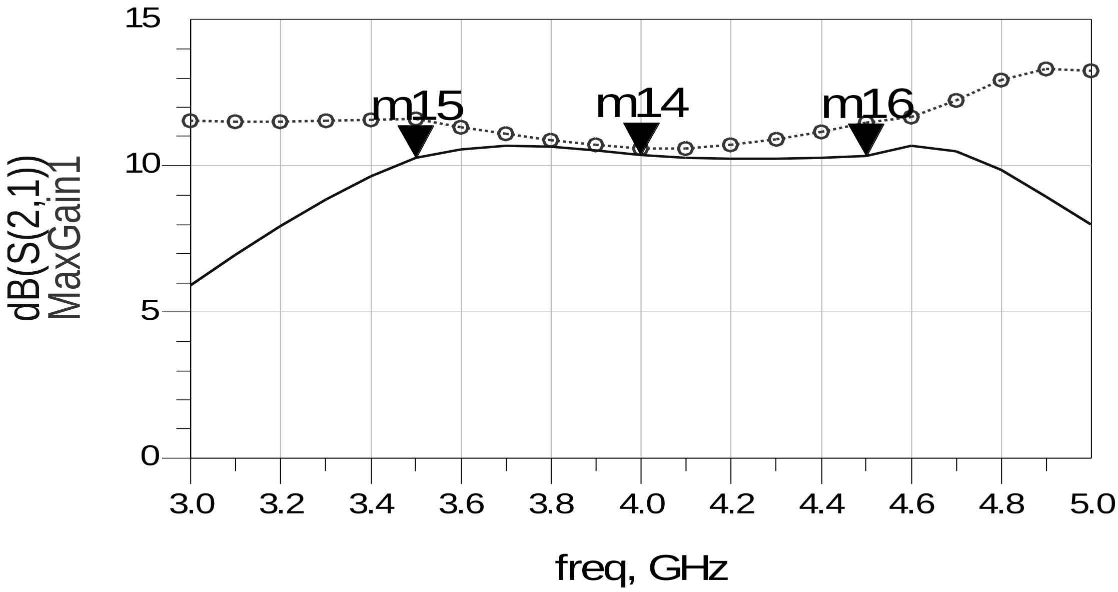

Figure 3: Broadband Gain Response of Power Amplifier Using **FLC317-MG** FET

References

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