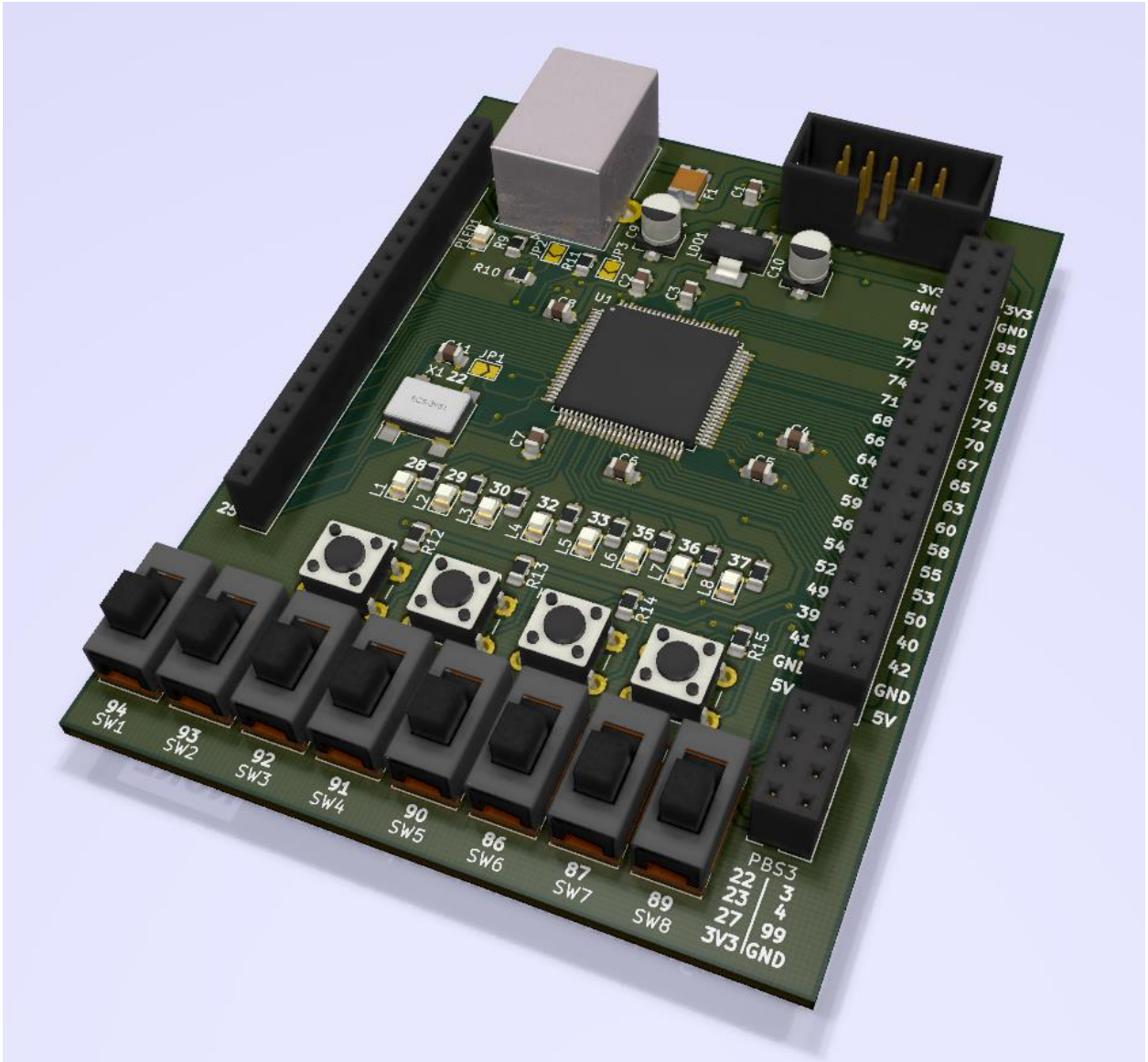
Xilinx XC9572XL
AntBoard
User Guide



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Chapter 1

Switches, Buttons and LEDs

Slide Switches

Locations and Labels

Xilinx XC9572XL AntBoard has eight slide switches, as shown in Figure 1-1. The slide switches are located on the bottom of the board and are labeled from SW1 to SW8. Switch SW1 is the left-most switch, and SW2 is the right-most one.

Figure 1-1: Eight Slide Switches

Operation

When in the UP or ON position, a switch connects the I/O pin to 3.3V, a logic High. When DOWN or in the OFF position, the switch connects the I/O pin to ground, a logic Low. The switches typically exhibit about 25ms of mechanical bounce and there is no active debouncing circuitry, although such circuitry could easily be added to the design project programmed on the board.

UCF Location Constraints

Figure 1-2 provides the UCF constraints for the slide switches, including the I/O pin assignment for switches SW1-SW3.

```
NET "SW(1)" LOC = "P94";
NET "SW(2)" LOC = "P93";
NET "SW(3)" LOC = "P92";
```

Figure 1-2: UCF Constraints for Slide Switches

Push Buttons

Locations and Labels

Xilinx XC9572XL AntBoard has four momentary-contact push-button switches, as shown in Figure 1-3. The push buttons are located on the bottom of the board, above the slide switches, and are labeled from KEY1 to KEY4. The FPGA pins that connect to the push buttons appear above each button.

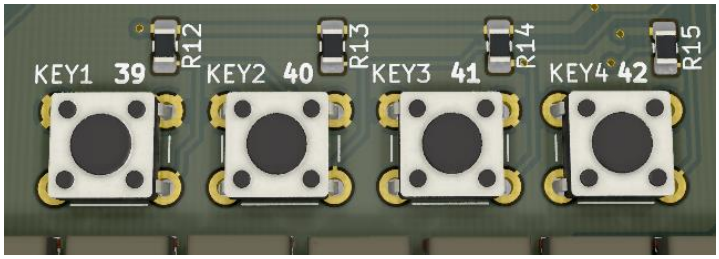


Figure 1-3: Four Push-Button Switches

Operation

Pressing a push button connects the associated FPGA pin to Ground, as shown in Figure 1-4. All the buttons are default connected to 3.3v using external pull-up resistors. There is no active debouncing circuitry on the push button.

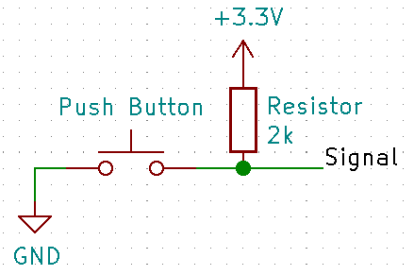


Figure 1-4: Push-Button Switch and an external pull-up resistor

UCF Location Constraints

Figure 1-5 provides the UCF constraints for the push-button switches, including the I/O pin assignment for buttons KEY1-KEY4.

```
NET "KEY1" LOC = "P39";
NET "KEY2" LOC = "P40";
NET "KEY3" LOC = "P41";
NET "KEY4" LOC = "P42";
```

Figure 1-5: UCF Constraints for Push-Button Switches

Discrete LEDs

Locations and Labels

Xilinx XC9572XL AntBoard has eight individual surface-mount LEDs located above the push-button switches as shown in Figure 1-6. The LEDs are labeled L1 through L8. L1 is the left-most LED, L8 the right-most LED.

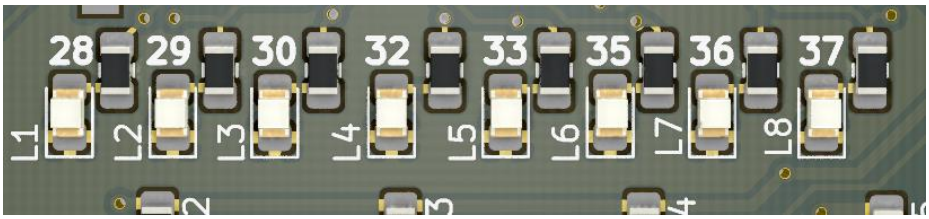


Figure 1-6: Eight Discrete LEDs

Operation

Each LED has one side connected to ground and the other side connected to a pin on the XC9572 device via a 1,5kΩ current limiting resistor. To light an individual LED, drive the associated FPGA control signal High.

UCF Location Constraints

Figure 1-7 provides the UCF constraints for the discrete LEDs, including the I/O pin assignment for LEDs L1-L4.

```
NET "L(1)" LOC = "P28";
NET "L(2)" LOC = "P29";
NET "L(3)" LOC = "P30";
NET "L(4)" LOC = "P32";
```

Figure 1-7: UCF Constraints for Eight Discrete LEDs

Chapter 2

Clock Sources

On-Board Oscillator

Xilinx XC9572XL AntBoard includes one on-board 25 MHz clock oscillator. The oscillator is located above a left-most LED, as shown in Figure 2-1. Its pin is duplicated on PBS3 and is controlled by jumper JP1. Consequently, the oscillator can be easily disconnected by removing the jumper.

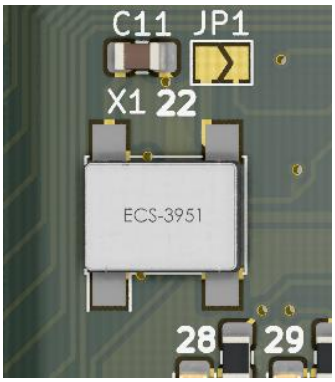


Figure 2-1: On-board 25 MHz Clock Oscillator

Clock Connections

Xilinx XC9572XL AntBoard has PBS3 connector that is located in the lower right corner of the board, as shown in Figure 2-2. Each of the clock inputs connect directly to a global buffer input pins. Global buffers are most commonly used to provide the least amount of skew possible between a large number of macrocells in a CPLD. You can also use them to provide quick access to control signals in high speed applications. Each global buffer in a CPLD may be routed to as many macrocells as desired without using additional routing or logic resources. (GCK – global clock, GTS – global tri-state, GSR – global set/reset).

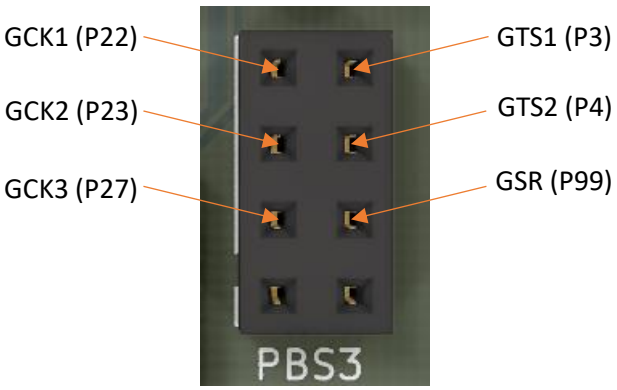


Figure 2-2: Pin Header routed to global buffers

UCF Constraints

You can manually assign selected signals to global nets with the **BUFG** attribute. **BUFG** can also be placed on internal nets, causing the fitter to automatically route the net to corresponding control points using the global nets. For tri-state control signals (BUFG=OE), internal nodes are routed through a global I/O pad. For example, use BUFG=CLK to route through a GCK buffer, use BUFG=OE to route through a GTS buffer and use BUFG=SR to route through a GSR buffer. Figure 2-3 provides an example for routing the on-board 25 MHz oscillator to a global clock net.

```
INST "CLK" LOC = "P22";
NET "Clk" BUFG = "CLK";
```

Figure 2-3: UCF Constrains to Connect Signal to a Global Clock Net

Chapter 3

Expansion Connectors

I/O Pin Headers

The 20-pin accessory headers provide easy I/O expansion interface for using various peripheral devices and modules.

Header PBS1

The PBS1 header, shown in Figure 3-1, is the 20-pin connector along the left edge of the board. It uses a female 90° socket. The header has 2 power pins and 18 connected CPLD I/O.

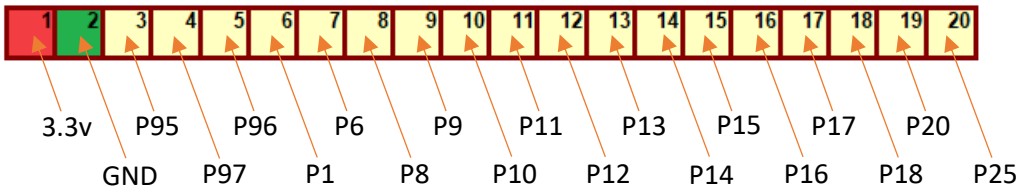


Figure 3-1: Header PBS1 Pinout

Header PBS2

The PBS1 header, shown in Figure 3-2, is the 40-pin connector along the right edge of the board. It uses a female 90° socket. The header has 8 power pins: 2 – 3.3v, 2 – 5v and 4 – GND. 32 pins connect CPLD I/O. Pins from P39 to P42 are duplicated on the buttons. That means they are pulled-up by default.

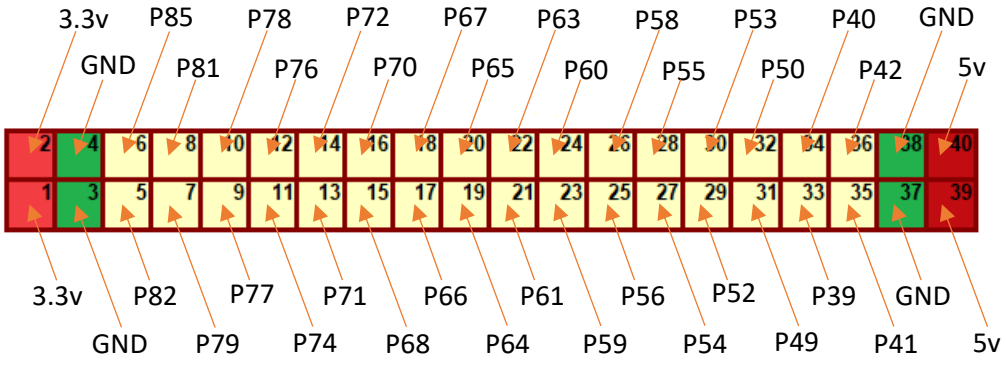


Figure 3-2: Header PBS2 Pinout

USB Connection

Xilinx XC9572XL AntBoard can be connect as an USB device. To start working with USB you need to put jumpers JP2 and JP3, shown Figure 3-3. They go from P25 and P20 CPLD I/O and connect to USB DP/DN accordingly. Their line have all the necessary pull-up and pull-down resistors.

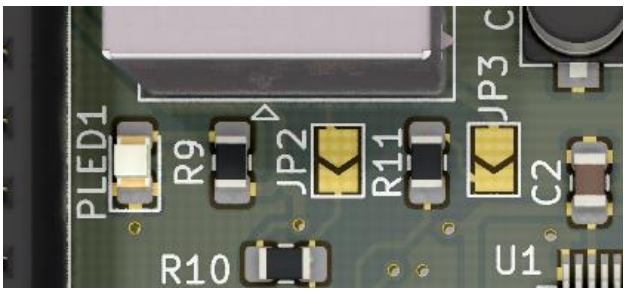
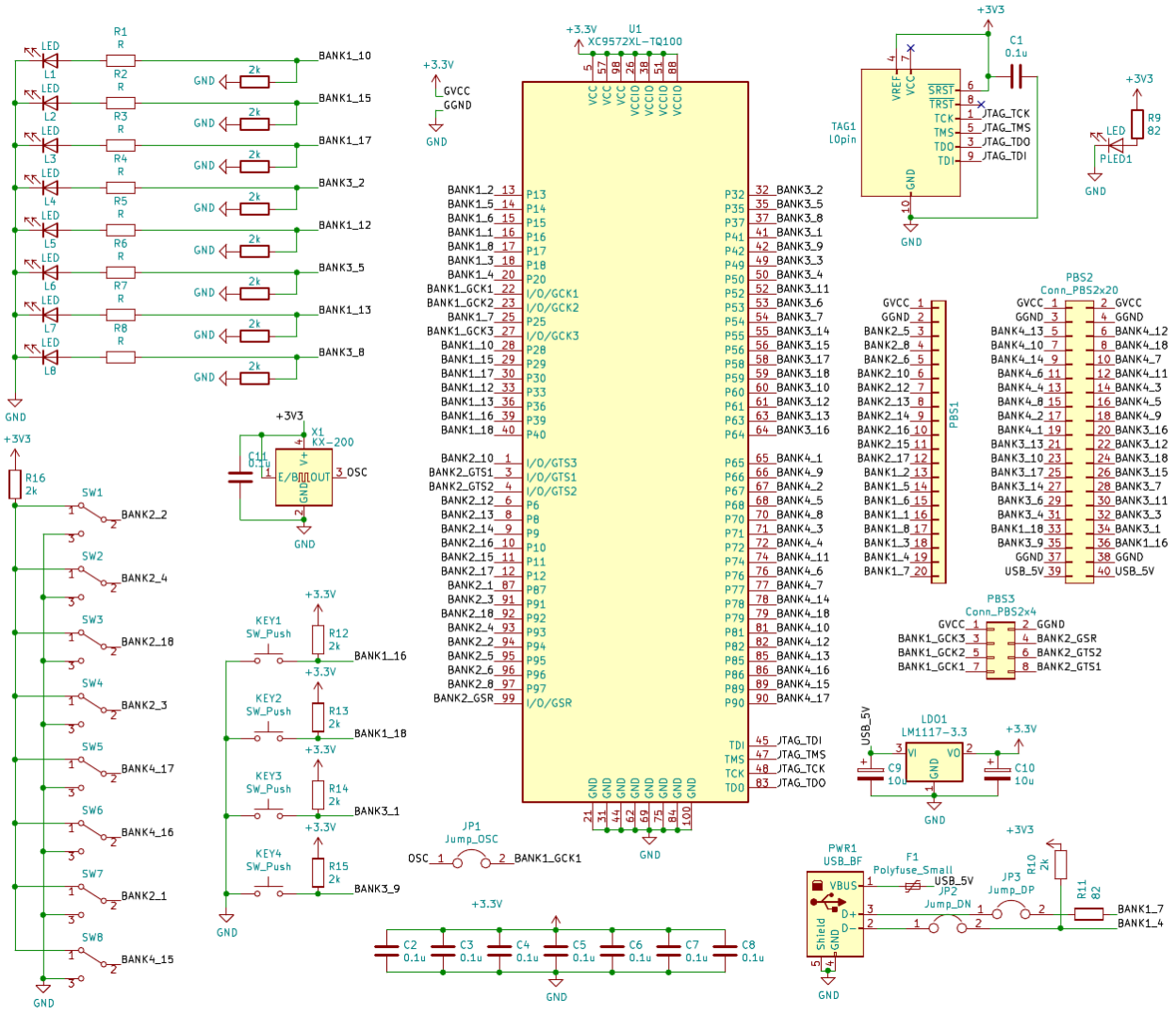


Figure 3-3: Jumpers JP2 and JP3 below USB Port

Schematic


U1
XC9572XL-TQ100
+3.3V
GND
GVCC
GGND
BANK1_10
BANK1_15
BANK1_17
BANK3_2
BANK1_12
BANK3_5
BANK1_13
BANK3_8
BANK2_2
BANK2_4
BANK2_18
BANK2_3
BANK4_17
BANK4_16
BANK2_1
BANK4_15
BANK1_16
BANK1_18
BANK3_1
BANK3_9
BANK1_GCK1
OSC
TAG1
LOpin
JTAG_TCK
JTAG_TMS
JTAG_TDO
JTAG_TDI
PBS1
PBS2
Conn_PBS2x20
PBS3
Conn_PBS2x4
LDO1
LM1117-3.3
PWR1
USB_BF
F1
Polyfuse_Small
USB_5V
JP1
Jump_OSC
JP2
Jump_DN
JP3
Jump_DP
PLED1

Appendix B

Example User Constraints File (UCF)

```
##################################################
### XILINX XC9572XL ANTBOARD CONSTRAINTS FILE ###
##################################################

# ==== Push-Button Switches ====
NET "KEY(1)" LOC = "P39";
NET "KEY(2)" LOC = "P40";
NET "KEY(3)" LOC = "P40";
NET "KEY(4)" LOC = "P42";

# ==== Slide Switches ====
NET "SW(1)" LOC = "P94";
NET "SW(1)" LOC = "P93";
NET "SW(1)" LOC = "P92";
NET "SW(1)" LOC = "P91";
NET "SW(1)" LOC = "P90";
NET "SW(1)" LOC = "P86";
NET "SW(1)" LOC = "P87";
NET "SW(1)" LOC = "P89";

# ==== Discrete LEDs ====
NET "L(1)" LOC = "P28";
NET "L(2)" LOC = "P29";
NET "L(3)" LOC = "P30";
NET "L(4)" LOC = "P32";
NET "L(5)" LOC = "P33";
NET "L(6)" LOC = "P35";
NET "L(7)" LOC = "P36";
NET "L(8)" LOC = "P37";
```

```
# ==== Global Nets ====
#INST "CLK" LOC = "P23";
#INST "CLK" LOC = "P27";
INST "CLK" LOC = "P22";
NET "Clk" BUFG = "CLK";

#INST "OE" LOC = "P3";
INST "OE" LOC = "P4";
NET "TriState" BUFG = "OE";

INST "SR" LOC = "P99";
NET "SetReset" BUFG = "SR";
```