**Self-directed channel memristor for high temperature operation**

**Introduction**

Memristors have been studied intensely for the past several years due to their potential use in applications such as non-volatile memory, neuromorphic and bio-inspired computing and threshold logic.

The type of memristor described in this work is an ion-conducting device (also referred to as an electrochemical metallization, ECM, device) which relies on Ag+ movement into channels within the device active layer to change the device resistance. This memristor, referred to as a self-directed channel (SDC) device, uses a metal-catalyzed reaction within the device active layer to generate permanent conductive channels that contain Ag agglomeration sites. The amount of Ag within the channel determines the resistance of the device.

In this work, electrical properties of the layered memristor device are presented. These include the response of the device to a quasi-static DC IV sweep as a function of temperature and compliance current, frequency response to a sinusoidal input signal, write endurance, and pulsed response.

**Device operation**

SDC devices are initially in a high resistance state (MΩ–GΩ range) following fabrication. The first time a device is operated after fabrication the device self-directed channel is formed during application of a positive potential to the top electrode. The potential required for this operation is the same as required during normal device operation. This first operation generates Sn ions from the SnSe layer and forces them into the active Ge2Se3 layer. Theoretical calculations predict that these Sn ions facilitate the incorporation of Ag into the active layer at the Ge-Ge bonding sites. This occurs through an energetically favorable process in which the electrons entering the active layer from the negative bottom electrode, concurrently with the formation of Sn ions from the SnSe layer, enable formation of a pair of self-trapped electrons in the Ge2Se3 active layer strongly localized around the Ge-Ge dimers present in this Ge-rich glass.

The result of this is that Sn ions facilitate an energetically favorable reaction of Ag substitution for Ge on the Ge-Ge bond. During this reaction, the glass network is distorted, creating an ‘opening’ near the Ge-Ge sites. The open regions provide good access for Ag+ to the Ag-Ge site and become natural ‘conductive channels’ within the active layer for the movement of Ag+ during device operation. This self-directed channel is a result of the natural glass structure and follows the location of the initial Ge-Ge dimers within the glass. Since Ag has a tendency to agglomerate with other Ag atoms, these sites may encourage Ag agglomeration within the glass. Thus, device resistance changes by adding or removing Ag from the agglomeration sites within this in-situ generated pathway. It is expected then that conduction could occur between clusters of Ag agglomeration sites. The concentration of Ag at a given agglomeration site, and the distance between agglomeration sites dictates the device resistance. The resistance is tunable in the lower and higher directions by movement of Ag onto or away from these agglomeration sites through application of either a positive or negative potential, respectively, across the device.

**Device structure and fabrication**

Ion-conducting devices were fabricated with a via structure and top and bottom electrodes, each of which extends to a metal pad for wirebonding or electrical probing access (Fig.1). Devices were fabricated on 100 mm p-type Si wafers with 250 Å Cr (CVD)/500 Å W (CVD) layers already deposited on the wafers (purchased from Encompass Distribution Services, Tracy, CA, USA).

This constitutes the bottom electrode. After patterning the bottom electrode, 800 Å nitride is sputtered on the wafer. A via etched through the nitride layer defines the device contact size. Via sizes ranged from 0.25 to 4 µm in diameter. Device operation was independent of via size within this range.

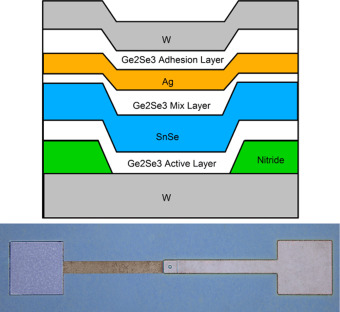
  
**Electrical measurements**

Figure 1

Electrical measurements consisted of: DC measurements as a function of compliance current and temperature; continuous-wave (CW) response for memristor classification and for cycling measurements; and pulse response to single and consecutive programming pulses.

**Results**

The DC programmed resistance as a function of compliance current and operating temperature, up to 150 °C, shows no significant variation in programmed resistance as a function of temperature. Furthermore, device cycling at room temperature and 140 °C both show functional devices out to at least 1 billion cycles.

These devices are classified as generic memristors based on their response to a sinusoidal input signal over a frequency range of 0.5–100 kHz.

The devices can be programmed over a continuous range of resistance states using two techniques: DC compliance current limiting and pulsed operation. Consecutive pulsing can selectively place a device into a desired resistance range, either through consecutive erase or write pulses. This range can be selected by varying the number of pulses applied, the pulse width, and/or the pulse amplitude.

**Acknowledgments**

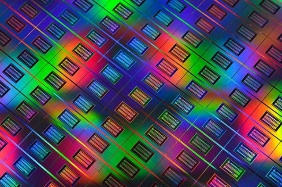
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memristor = memory resistor мемристор, запоминающий резистор (созданный компанией HP четвёртый фундаментальный элемент электронных схем - в дополнение к резистору, конденсатору и индуктивности; состоит из тонкого слоя диоксида титана, расположенного между двумя платиновыми электродами)

threshold logic 1) пороговая логика, логика на пороговых элементах

**HP bets it all on The Machine, a new computer architecture based on memristors and silicon photonics** June 11, 2014

https://www.extremetech.com/extreme/184165-hp-bets-it-all-on-the-machine-a-new-computer-architecture-based-on-memristors-and-silicon-photonics

memristor-die-wafer-shot-640x426

HP, one of the original 800lb Silicon Valley gorillas that has seen much happier days, is staking everything on a brand new computer architecture that it calls… *The Machine*. Judging by an early report from Bloomberg Businessweek, up to 75% of HP’s once fairly illustrious R&D division — HP Labs — are working on The Machine. As you would expect, details of what will actually make The Machine a unique proposition are hard to come by, but it sounds like HP’s groundbreaking work on memristors (pictured top) and silicon photonics will play a key role.

In the words of HP Labs, The Machine will be a complete replacement for current computer system architectures. There will be a new operating system, a new type of memory (memristors), and super-fast buses/peripheral interconnects (photonics).

First things first, we’re probably not talking about a *consumer* computing architecture here, though it’s possible that technologies commercialized by The Machine will percolate down to desktops and laptops. Basically, HP used to be a huge player in the workstation and server markets, with its own operating system and hardware architecture, much like Sun. Over the last 10 years though, Intel’s x86 architecture has rapidly taken over, to the point where HP (and Dell and IBM) are essentially just OEM resellers of commodity x86 servers. This has driven down enterprise profit margins — and when combined with its huge stake in the diminishing PC market, you can see why HP is rather nervous about the future. The Machine, and [IBM’s OpenPower initiative](http://www.extremetech.com/computing/181102-ibm-power8-openpower-x86-server-monopoly), are both attempts to get out from underneath Intel’s x86 monopoly.

HP started work on The Machine two years ago, when Martin Fink became CTO and head of HP Labs. He took a look at the components that HP Labs was working on — memristors, silicon photonics — and six months later he decided that it was time to pitch The Machine to HP CEO Meg Whitman. At the presentation, Fink said he expected 75% of HP Labs personnel to be dedicated to work on The Machine. Seemingly, Whitman agreed to the plan, because here we are in 2014 and HP is apparently staking its future on it.

While exact details are hard to come by, it seems The Machine is predicated on the idea that current RAM, storage, and interconnect technology can’t keep up with modern Big Data processing requirements. HP is working on two technologies that could solve both problems: Memristors could replace RAM and long-term flash storage, and silicon photonics could provide faster on- and off-motherboard buses. Memristors essentially combine [the benefits of DRAM and flash storage](http://www.extremetech.com/computing/83586-memristors-a-flash-competitor-that-works-like-brain-synapses) in a single, hyper-fast, super-dense package. Silicon photonics is all about reducing optical transmission and reception to a scale [that can be integrated into silicon chips](http://www.extremetech.com/computing/142881-ibm-creates-first-cheap-commercially-viable-silicon-nanophotonic-chip) (moving from electrical to optical would allow for much higher data rates and lower power consumption). Both technologies can be built using conventional fabrication techniques.

It sounds like The Machine would do away with RAM and external storage, instead packing tons of high-density memristor chips onto the motherboard, close to the CPU. (No word on what architecture the CPU might use, incidentally.) Everything would be connected together at high speed using silicon photonics — and you will no doubt be able to connect multiple Machines together via an optical interconnect, too.

The result would undoubtedly be a very fast device that opens up new ways of processing data. But, in all honesty, it isn’t hard to *conceive* of a fantabulous computer architecture that has monstrous processing power — but it is hard to actually build such a system in reality. The key element here will be software — both the operating system, which will have to be designed from the ground up for these new computing and storage paradigms, and the app ecosystem. The entire PC and server industry is already entrenched with x86, Windows, and Linux. It would require a monumental effort on HP’s behalf to create and support a brand new architecture that has almost no similarity to the platforms that developers have been targeting for the last 50 years.