**Lab2:**Q1.1:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Cache | Cache Line Size | Total Size | Number of Ways (Associativity) | Number of Sets | Raw Latency |
| L1 | 64 bytes | 64 KB | 8 | 128 | Didn't find |
| L2 | 64 bytes | 256 KB | 4 | 1024 | On the |
| L3 | 64 bytes | 12288KB | 12 | 16384 | Given website |

Q1.2 : L1 average latency id 22 cycles

Q1.3 : DRAM average latency id 179 cycles

Q1.4: To fill L1 we needed L1size/cacheLineSize = 512 cache lines. For filling L2 we needed L2size/cacheLineSize = 4096 cache lines.

Q1.5: L2 : 32 cycles and L3 43 cycles