**Lab2:**Q1.1:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Cache | Cache Line Size | Total Size | Number of Ways (Associativity) | Number of Sets | Raw Latency |
| L1 | 64 bytes | 64 KB | 8 | 128 | Didn't find |
| L2 | 64 bytes | 256 KB | 4 | 1024 | On the |
| L3 | 64 bytes | 12288KB | 12 | 16384 | Given website |

Q1.2 : L1 average latency id 22 cycles

Q1.3 : DRAM average latency id 179 cycles

Q1.4: To fill L1 we needed L1size/cacheLineSize = 512 cache lines. For filling L2 we needed L2size/cacheLineSize = 4096 cache lines.

Q1.5: L2 : 22 cycles and L3 34 cycles

A graph of different colored lines

AI-generated content may be incorrect.Q1.6:

Q1.7: The threshold between L2 and L3 will be 30 cycles and between L3 and DRAM will be 100 cycles.  
  
Q2.1:  
Sender and receiver communicate over an L2 cache covert channel: the sender creates contention on one cache *set* so the receiver can detect which set is being targeted.  
The sender converts user input to an integer message and then repeatedly reads a pattern of addresses that chosen.

The receiver scans the L2 cache, measuring the access time to each cache line to find the one that targeted by the sender.