Ref Doc		Description	UAL Code				Bits														Flags			
			Instruction	Operandes			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	C	V	N	Z
		Shift , add, sub, mov							opcode																	
p.30	1	Logical Shift Left	LSLS	Rd	Rm	imm5	0	0	0	0	0	imm5					Rm		Rd		x		x	x
	2	Logical Shift Right	LSRS	Rd	Rm	imm5	0	0	0	0	1	imm5					Rm		Rd		x		x	x
	3	Arithmetic Shift Right	ASRS	Rd	Rm	imm5	0	0	0	1	0	imm5					Rm		Rd		x		x	x
	4	Add register	ADDS	Rd	Rn	Rm	0	0	0	1	1	0	0	Rm			Rn		Rd		x	x	x	x
	5	Substract register	SUBS	Rd	Rn	Rm	0	0	0	1	1	0	1	Rm			Rn		Rd		x	x	x	x
	6	Add 3-bit immediate	ADD3	Rd	Rn	imm3	0	0	0	1	1	1	0	imm3			Rn		Rd		x	x	x	x
11.1.1	7	Substract 3-bit immediate	SUB3	Rd	Rn	imm3	0	0	0	1	1	1	1	imm3			Rn		Rd		x	x	x	x
	8	Move	MOVS	Rd	imm8		0	0	1	0	0	Rd							imm8				x	x
	9	Compare	CMPS	Rd	imm8		0	0	1	0	1	Rd							imm8		x	x	x	x
	10	Add 8-bit immediate	ADDS8	Rdn	imm8		0	0	1	1	0	Rdn							imm8		x	x	x	x
	11	Substract 8-bit immediate	SUBS8	Rdn	imm8		0	0	1	1	1	Rdn							imm8		x	x	x	x
		Data Processing											opcode											
p.35	1	Bitwise AND	ANDS	Rdn	Rm		0	1	0	0	0	0	0	0	0	0	Rm		Rdn		0		x	x
	2	Exclusive OR	EORS	Rdn	Rm		0	1	0	0	0	0	0	0	0	1	Rm		Rdn		1		x	x
	3	Logical Shift Left	LSLS	Rdn	Rm		0	1	0	0	0	0	0	0	1	0	Rm		Rdn		x		x	x
	4	Logical Shift Right	LSRS	Rdn	Rm		0	1	0	0	0	0	0	0	1	1	Rm		Rdn		x		x	x
	5	Arithmetic Shift Right	ASRS	Rdn	Rm		0	1	0	0	0	0	0	1	0	0	Rm		Rdn		x		x	x
	6	Add with Carry	ADCS	Rdn	Rm		0	1	0	0	0	0	0	1	0	1	Rm		Rdn		x	x	x	x
	7	Substract with Carry	SBCS	Rdn	Rm		0	1	0	0	0	0	0	1	1	0	Rm		Rdn		x	x	x	x
	8	Rotate Right	RORS	Rdn	Rm		0	1	0	0	0	0	0	1	1	1	Rm		Rdn		x		x	x
	9	Set Flags on bitwise AND	TSTS	Rdn	Rm		0	1	0	0	0	0	1	0	0	0	Rm		Rn		0		x	x
11.1.2	10	Reverse Substract from 0	RSBS	Rd	Rn		0	1	0	0	0	0	1	0	0	1	Rn		Rd		0	x	x	x
	11	Compare Registers	CMPS	Rn	Rm		0	1	0	0	0	0	1	0	1	0	Rm		Rn		x	x	x	x
	12	Compare Negative	CMNS	Rn	Rm		0	1	0	0	0	0	1	0	1	1	Rm		Rn		x	x	x	x
	13	Logical OR	ORRS	Rdn	Rm		0	1	0	0	0	0	1	1	0	0	Rm		Rdn		0		x	x
	14	Multiply Two Registers	MULS	Rdm	Rn	Rdm	0	1	0	0	0	0	1	1	0	1	Rn		Rdm				x	x
	15	Bit Clear	BICS	Rdn	Rm		0	1	0	0	0	0	1	1	1	0	Rm		Rdn		0		x	x
	16	Bitwise NOT	MVNS	Rd	Rm		0	1	0	0	0	0	1	1	1	1	Rm		Rd		1		x	x
		Load/Store									opcode													
11.1.3	1	Store Register	STR	Rt	imm8	SP	1	0	0	1	0	Rt							imm8					
p.41	2	Load Register	LDR	Rt	imm8	SP	1	0	0	1	1	Rt							imm8					
		Miscellaneous 16-bit instructions									opcode													
11.1.4	1	Add Immediate to SP	ADD	SP	imm7	SP	1	0	1	1	0	0	0	0	0	imm7								
p.42	2	Substract Immediate from SP	SUB	SP	imm7	SP	1	0	1	1	0	0	0	0	1	imm7								
		Branche conditionnelle									condition													
11.1.5		Egalité	EQ				1	1	0	1	0	0	0	0	imm8									1
p.42		Différence	NE				1	1	0	1	0	0	0	1	imm8									0
		Retenue	CS ou HS				1	1	0	1	0	0	1	0	imm8						1			
		Pas de retenue	CC ou LO				1	1	0	1	0	0	1	1	imm8						0			
		Négatif	MI				1	1	0	1	0	1	0	0	imm8								1	
		positif ou nul	PL				1	1	0	1	0	1	0	1	imm8								0	
		Dépassement de capacité	VS				1	1	0	1	0	1	1	0	imm8							1		
		Pas dépassement capacité	VC				1	1	0	1	0	1	1	1	imm8							0		
		Supérieur (non signé)	HI				1	1	0	1	1	0	0	0	imm8						1			0
		Inf. ou égal (non signé)	LS				1	1	0	1	1	0	0	1	imm8						C==1 ou Z==1			
		Supérieur ou égal (signé)	GE				1	1	0	1	1	0	1	0	imm8							N == V		
		Inférieur (signé)	LT				1	1	0	1	1	0	1	1	imm8							N != V		
		Supérieur (signé)	GT				1	1	0	1	1	1	0	0	imm8							N==V		0
		Inf. ou égal (signé)	LE				1	1	0	1	1	1	0	1	imm8						Z == 0 et N == V			
		toujours vrai	AL				1	1	0	1	1	1	1	0	imm8									
		Branche non conditionnelle	B				1	1	1	0	0	imm11												