SPCC

ALP structure

Lable Opcode Operand

5) Assembler & Macro Processor

* Types of ALP :- Absolute / Non Relocatable
:- Relocatable

Absolute / Non Relocatable

→ The address at which program needs to be loaded in the memory for execution is fixed.

→ Allocation is done by programmer & loading is done by Loader.

Eg :- PG1 START 4000H

Relocatable

→ These programs can be loaded anywhere in the memory.

→ Allocation and loading would be done by loader

Eg :- PG1 START 0

* Statements in ALP

1) Imperative Statements

→ These are the statements executed and understood by the machines.

→ Eg :- Instructions

#→ 5 ~~Imperative~~ Statements :- START, END, EQU, USING & DROP.
Assembler Directive

2) Declarative Statements

→ These statements are used for declaration purpose.

→ Declare / Define Constant (DC)

Eg:- D1 DC F '4'

→ D1 is declared as constant having value 4 with memory size of 1 Full Word.

→ Define / Declare Storage (DS)

Eg:- ~~D1 DS~~ T1 DS '1' F

→ T1 is declared as a temporary storage with memory 1 Full Word

3) Assembler Directive Statement

→ These are the statements that direct the assembler to take necessary actions.

Eg:- START Statement PG1 START 4000H → Absolute

END Statement PG1 START → Relocatable

#

		Bytes	bits
Bytes	B	1	8
Half Word	H	2	16
Full Word	F	4	32
Double Word	D	8	64

Symbols are in Label Field
1, FIVE → RX → ~~L0~~ LC ↑ by 4
EA → Disp (Index, Base)

Ex 1)

		LC (Pass 1)	LC (Pass 2)
PG1	START 0	0	0
	USING *, 15	0	0
	L 1, FIVE	0 L1, ___	0 L1, 16(0,15
	A 1, FOUR	4 A1, ___	4 A, 12(0, 1
	ST 1, TEMP	8 ST 1, ___	8 ST, 20(0, 1
FOUR	DC F '4'	12 F '4', ___	12 0100
FIVE	DC F '5'	+4(F) 16 F '5'	16 0101
TEMP	DS ~~1F~~	20 DS 1F	
	END	24	

→

MOT (Machine Opcode Table)

Machine Opcode	Binary Opcode	Instruction Length	Instruction Format
L	✓	✓	RX
A	✓	✓	RX
ST	✓	✓	RX

POT (Pseudo Opcode Table) [Fixed Length Table]

Pseudo Opcode	Address
START	
USING	
~~DC~~	
DS	
END	

ST (Symbol Table)

Symbol	Value	Length	R/A
PG1	0	01	R
FOUR	12	04 (Full)	R
FIVE	16	04	R
TEMP	20	04	R

LT (Literal Table)

Literal	Value	Length	R/A

BT (Base Table)

Availability of Indicator	Content of BR
0 N 1 N 2 N 3 N . . . . 14 N 15 YES	00

Q2)

		LC (Pass 1)	LC (Pass 2)
PG2	START	0	0
	USING *, BASE	0	0
	L 2, D1	0 L2, ___	0 L2, 16(0,12)
	A 2, D2	4 A2, ___	4 A2, 20(0,12)
	A 2, D3	8 A2, ___	8 A2, 24(0,12)
	ST 2, T1	12 ST 2, ___	12 ST 2, 28(0,12)
D1	DC F'7'	16 ~~DF7~~	16 0111
D2	DC F'4'	20 F4 ___	20 0100
D3	DC F'8'	24 F8	24 1000
BASE	EQU 12	28	
T1	DS '1' F	28 DS 1F	
	END	32	

Symbol Table:

Symbol	Value	Length	R/A
PG2	0	01	R
D1	16	04	R
D2	20	04	R
D3	24	04	R
BASE	12	01	A

T1	28	4	R

POT (Pseudo Opcode Table) :-

Pseudo Opcode	Address
START	
USING	
DC	
DS	
EQU	
END	

MOT (Machine Opcode Table) :-

Machine Opcode	Binary Opcode	Instr. Length	Instr. Format
L	✓	✓	RX
A	✓	✓	RX
A	✓	✓	RX
ST	✓	✓	RX

Base Table (BT)

Availability Indicator		Content of Base Register
0	NO	
1	NO	
2	:	
:	:	
12	YES	00
13	NO	
14	NO	
15	NO	

Literal at Value End of Program

			LC (PASS 1)		LC (PASS 2)	
(Q3)	PG3	START	0		0	
		USING *, BASE	0		0	
		L 2, D1	0	L2, ___	0	L2, 16(0,12)
		A 2, D2	4	A2, ___	4	A2, 20(0,12)
		A 2 = F'4'	8	A2	8	A2, 28(0,12)
		ST 2, T1	12	ST 2, ___	12	ST2, 24(0,12)
	D1	DC F '5'	16	F5	16	101
	D2	DC F '7'	20	F7	20	111
	BASE	EQU 12	24			
	T1	DS 1'F'	24	DS 1F		
		END	28			

→ ST

Symbol	Value	Length	R/A
PG3	0	01	R
D1	16	04	R
D2	20	04	R
BASE	24	01	A
T1	24	04	R

→ MOT

MO	BO	Inst. Length	Inst. Format
L	✓	✓	RX
A	✓	✓	RX
ST	✓	✓	RX

→ POT

PO	Address
~~PG~~ START	
USING	
DC	
DS	
EQU	
END	

→ LT

Literal	Value	Length	R/A
=F'4'	28	04	R