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```
[2025-06-19 17:39:11 UTC] vcs -full64 -licqueue '-timescale=1ns/1ns' '+vcs+flush+all' '+warn=al
                        Chronologic VCS (TM)
       Version U-2023.03-SP2_Full64 -- Thu Jun 19 13:39:12 2025

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Parsing design file 'design.sv'
Parsing design file 'testbench.sv'
Top Level Modules:
       async_fifo_tb
TimeScale is 1 ns / 1 ps
Starting vcs inline pass...

1 module and 0 UDP read.
recompiling module async_fifo_tb
rm -f _cuarc*.so _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [ -x ../simv ]; then chmod a-x ../simv; fi
g++  -o ../simv      -rdynamic  -Wl,-rpath='$ORIGIN'/simv.daidir -Wl,-rpath=./simv.daidir -Wl,-r
../simv up to date
CPU time: .487 seconds to compile + .502 seconds to elab + .388 seconds to link
Chronologic VCS simulator copyright 1991-2023
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Compiler version U-2023.03-SP2_Full64; Runtime version U-2023.03-SP2_Full64;  Jun 19 13:39 2025
Starting Async FIFO Testbench...

--- Writing to FIFO ---
Write: 24
Write: 81
Write: 9
Write: 63
Write: d
Write: 8d
Write: 65
Write: 12
Write: 1
Write: d
Write: 76
Write: 3d
Write: ed
Write: 8c
```

```
Write: f9
FIFO Full! Write blocked.
FIFO Full! Write blocked.
FIFO Full! Write blocked.
FIFO Full! Write blocked.
FIFO Full! Write blocked.

--- Reading from FIFO ---
Read: 0
Read: 24
Read: 81
Read: 9
Read: 63
Read: d
Read: 8d
Read: 65
Read: 12
Read: 1
Read: d
Read: 76
Read: 3d
Read: ed
Read: 8c
FIFO Empty! Read blocked.
FIFO Empty! Read blocked.
FIFO Empty! Read blocked.
FIFO Empty! Read blocked.
FIFO Empty! Read blocked.

--- Simultaneous Write and Read ---
Write: c6
Write: c5
Write: aa
Read: f9
Write: e5
Read: c6
Write: 77
Read: c6
Write: 12
Read: c5
Write: 8f
Read: aa
Write: f2
Read: aa
Write: ce
Read: e5
Write: e8
Read: e5

Testbench Finished.
$finish called from file "testbench.sv", line 114.
$finish at simulation time               595000
           V C S   S i m u l a t i o n   R e p o r t
Time: 595000 ps
CPU Time:      0.400 seconds;       Data structure size:   0.0Mb
```