EE 4540L/6540L/CEG4322L/CEG6322L

FALL 2023

TA: Kanchan Vissamsetty

Lab section: Lab6

UID: U01102112

Name: Vamshikrishna Bavirishetty

"I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code"

Signature: Vamshi **Date:11/10/2023**

Report due date: 11/13/2023

AIM/OBJECTIVE: The main aim of this lab is to design a 4-bit down counter in binary and decimal mode.

Procedure: I had used the D Flip Flop that was designed in the last lab.

And then I connected the circuit according to the manual.

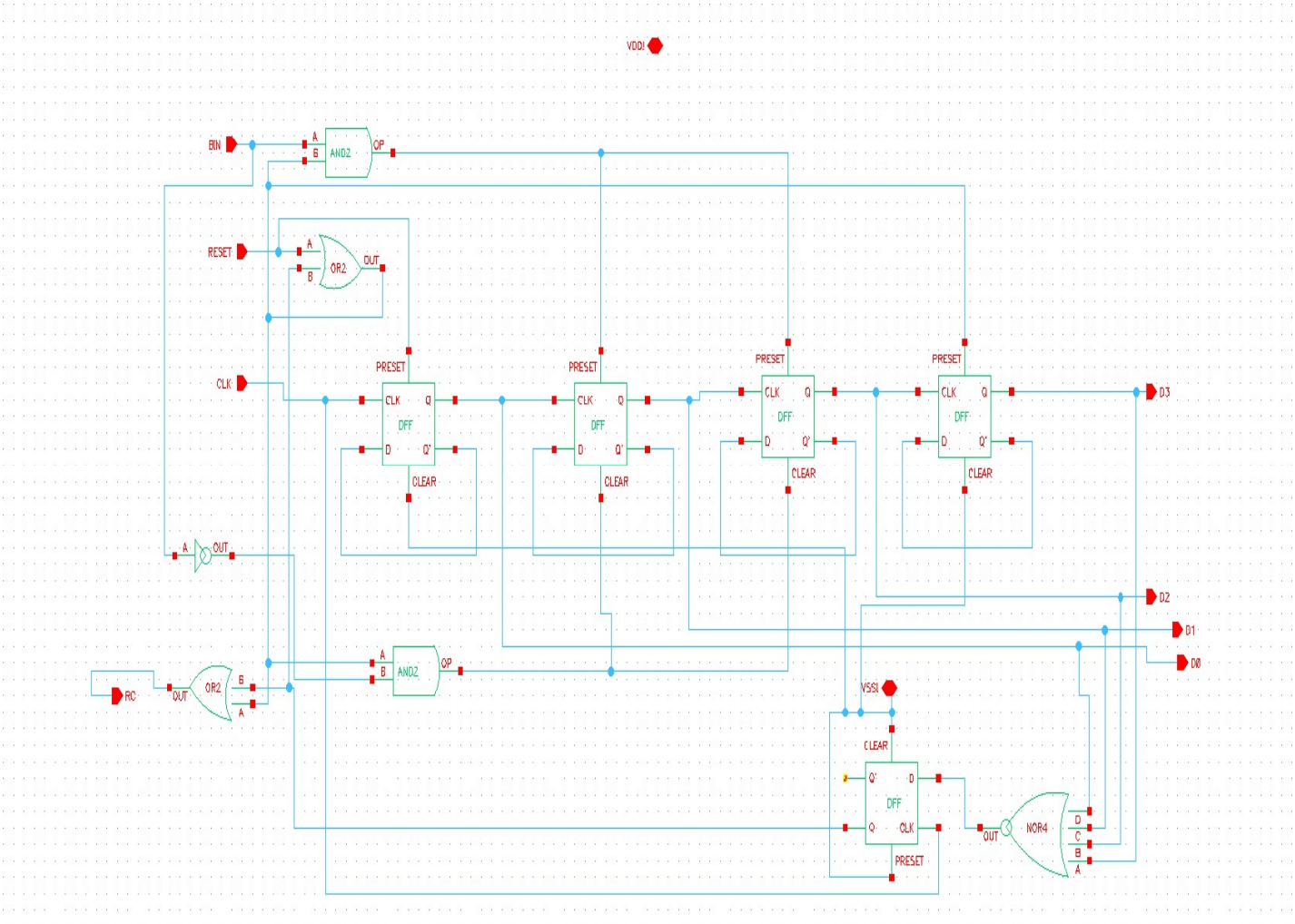
After connecting the circuit as per the circuit diagram I run the simulation.

And as per the manual I had given 2n as clock period.

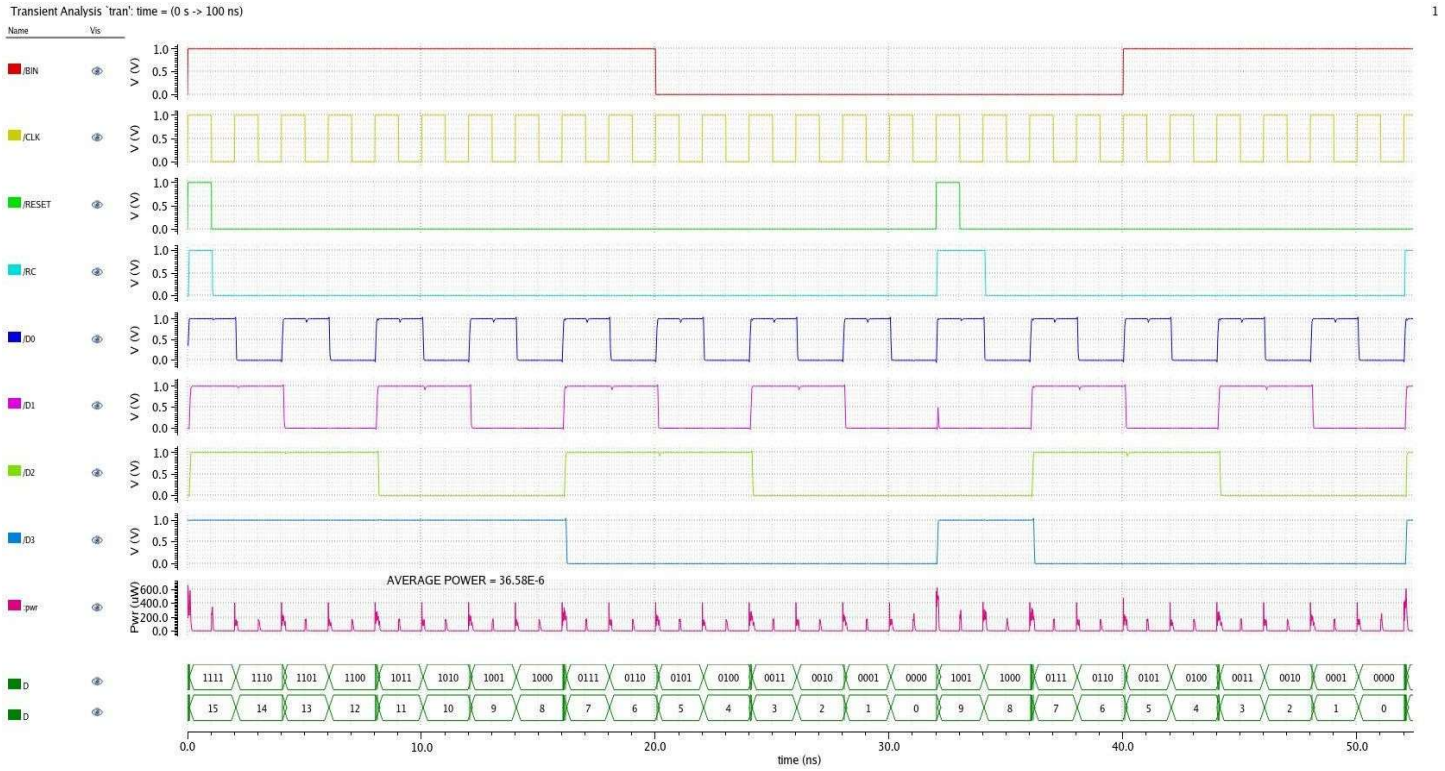
So that the down counter is working fine.

And then I was given clock frequency of 0.125 then there are some disturbances in the circuit and the down counter is not working fine.

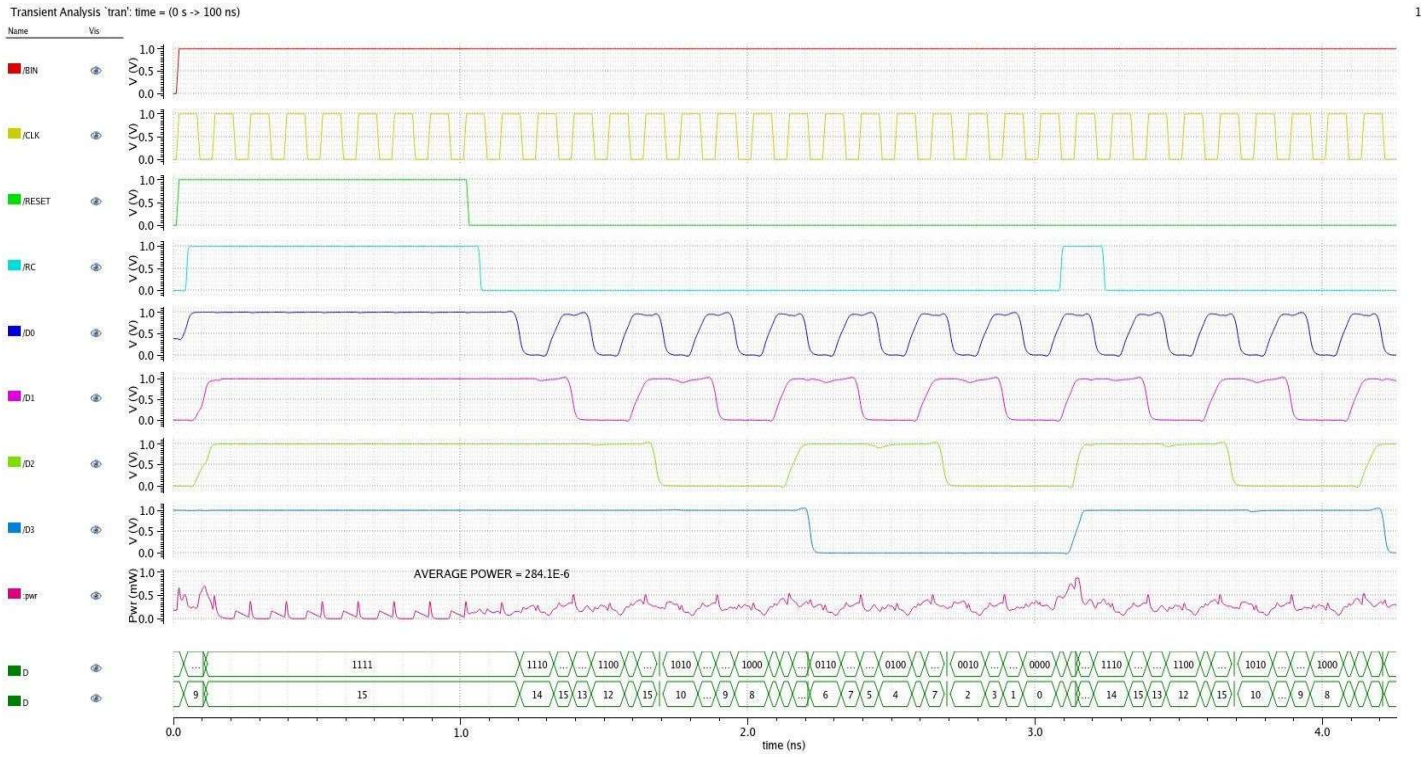
SCHEMATIC:



SIMULATION WAVEFORM OF DOWNCOUNTER WHEN CLOCK = 2n:

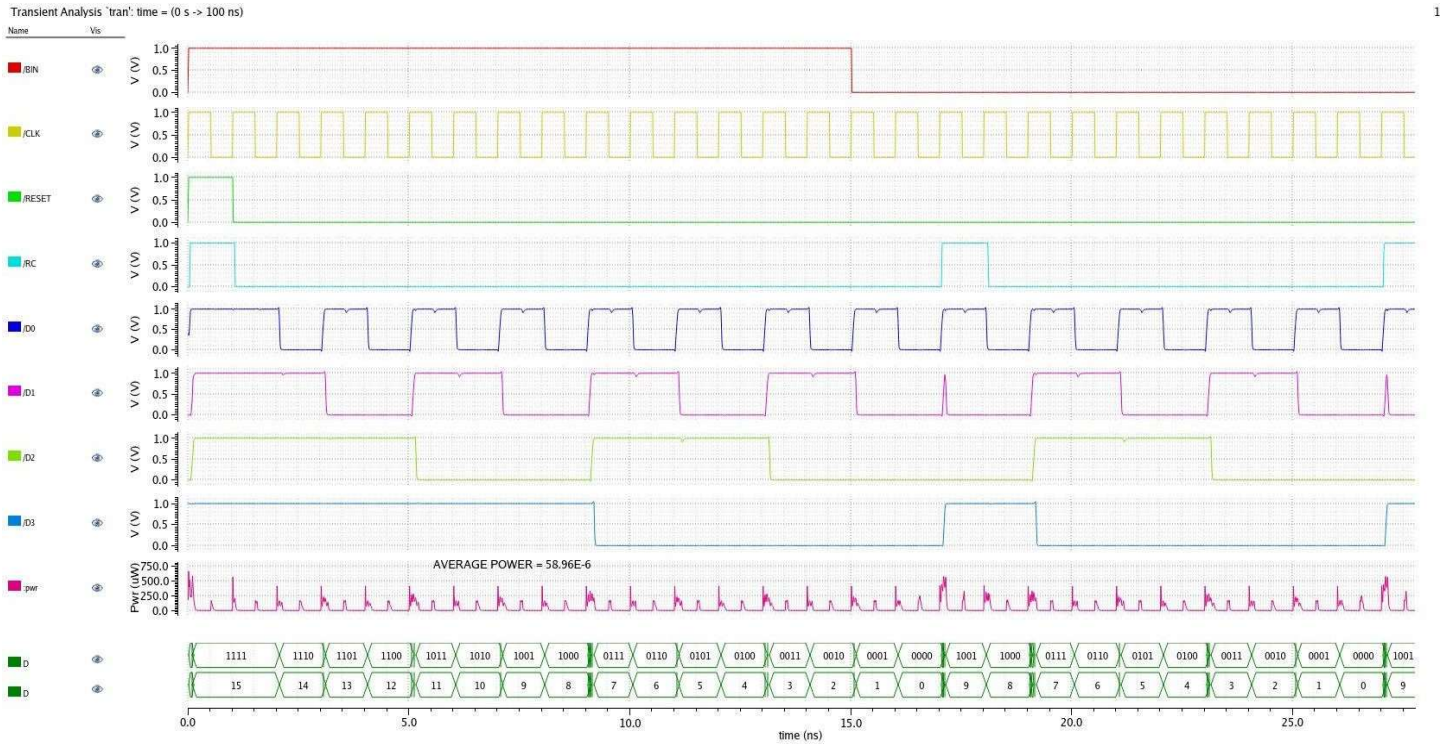


SIMULATION WAVEFORM WHEN CLOCK PERIOD IS 0.125n:



When I changed the clock period to 0.125n down counter is not working fine.

SIMULATION WAVEFORM WHEN CLOCK PERIOD IS 1n:



ADVANTAGE OF HAVING DIFFERENT WIDTHS FOR PMOS AND NMOS:

Improved performance

Power efficiency

Space utilization.

To run the circuits at the highest frequencies we must keep the interconnected lengths shorter and using efficient power distribution helps the circuit run smoothly even at higher frequencies.

Conclusion: In this lab, we designed and implemented a 4-bit binary and decimal down counter to explore the operation of sequential circuits and their practical applications in digital systems. This lab helped reinforce the concepts of binary and decimal counting systems. A 4-bit binary counter counts from 0 (0000 in binary) to 15 (1111 in binary), while a decimal down counter counts from 9 to 0.