EE 4540L/6540L/CEG4322L/CEG6322L

FALL 2023

TA: Kanchan Vissamsetty

Lab section: Lab5

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Name: Vamshikrishna Bavirishetty

"I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code"

Signature: Vamshi **Date:11/06/2023**

Report due date: 11/06/2023

AIM/OBJECTIVE: The main aim of this lab is to implement a positive edge trigger D Flip Flop with asynchronous preset and clear.

Procedure:

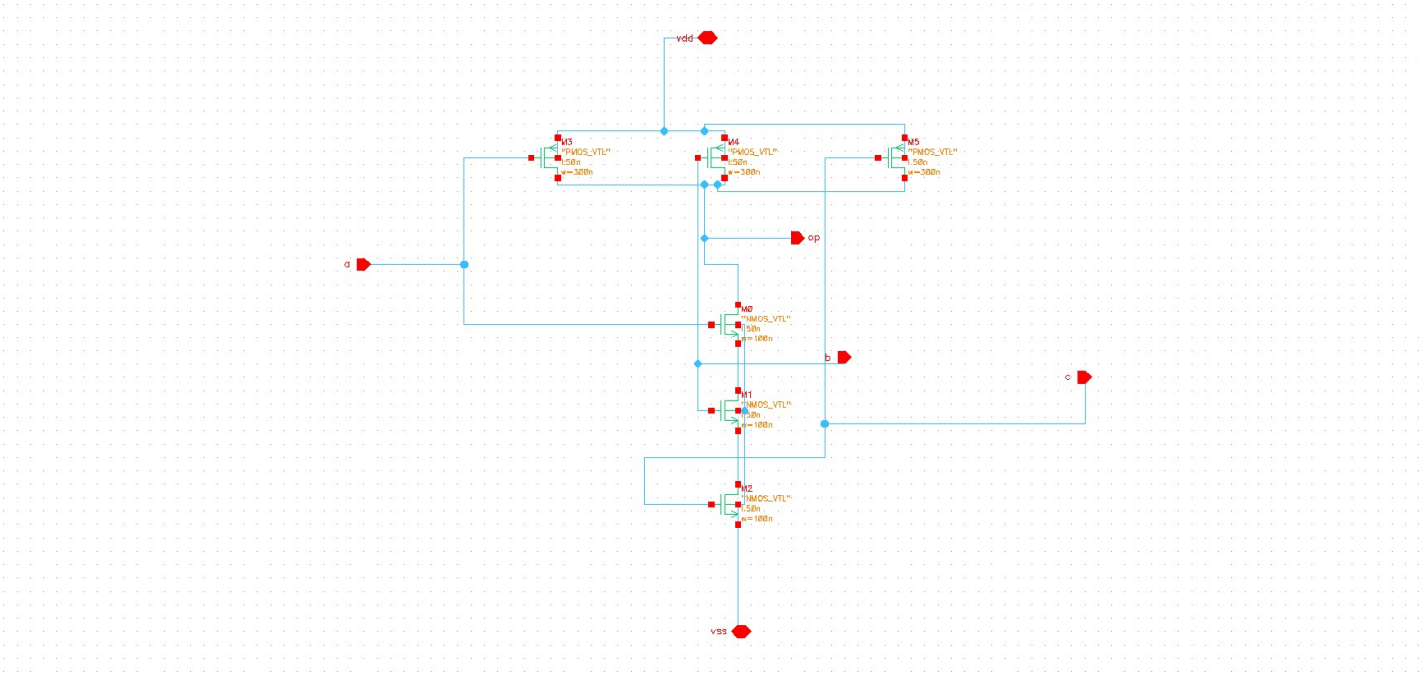
First step is to change the width of PMOS transistors in the NAND schematic to 300w and 150w and then record the propagation delays.

The next step is to change the width of NMOS transistors accordingly. so that we can get the same rising and falling propagation delays.

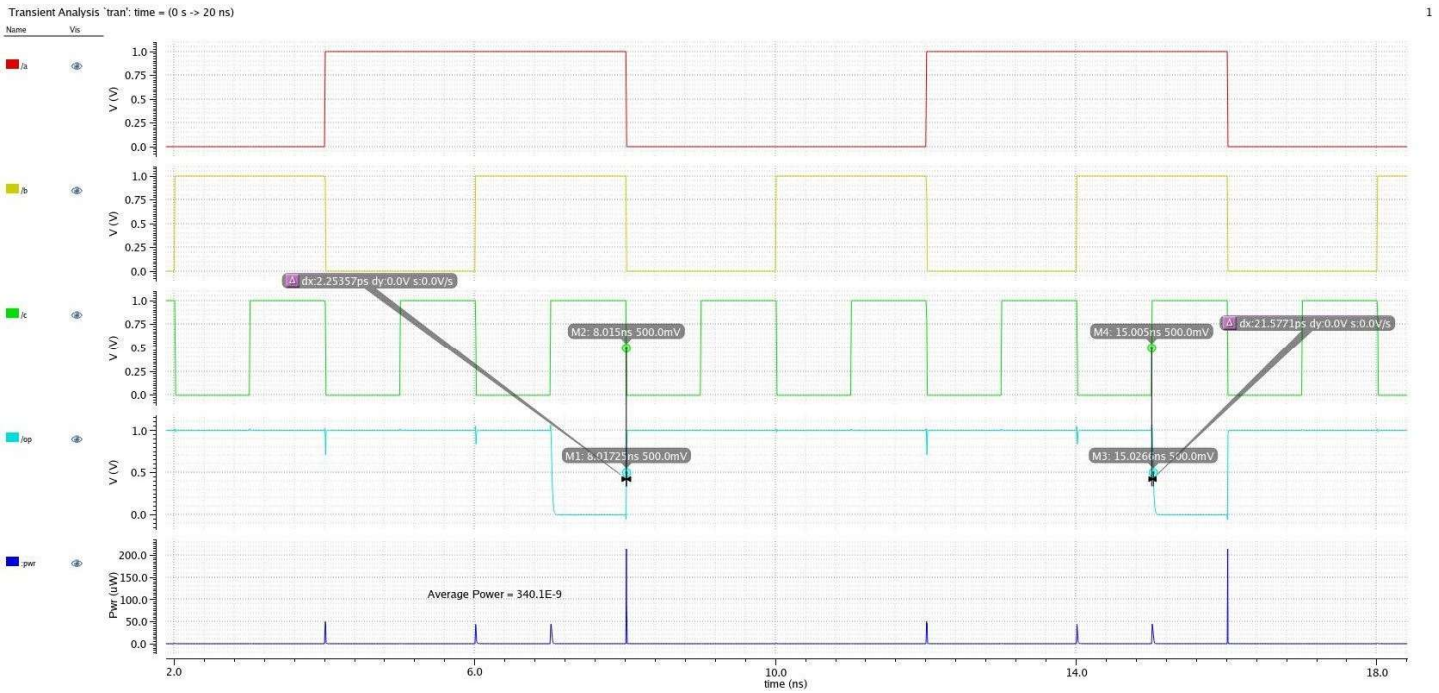
Next according to the logic diagram create a D Flip Flop with the help of NAND and inverter.

And then record the falling and rising propagation delays.

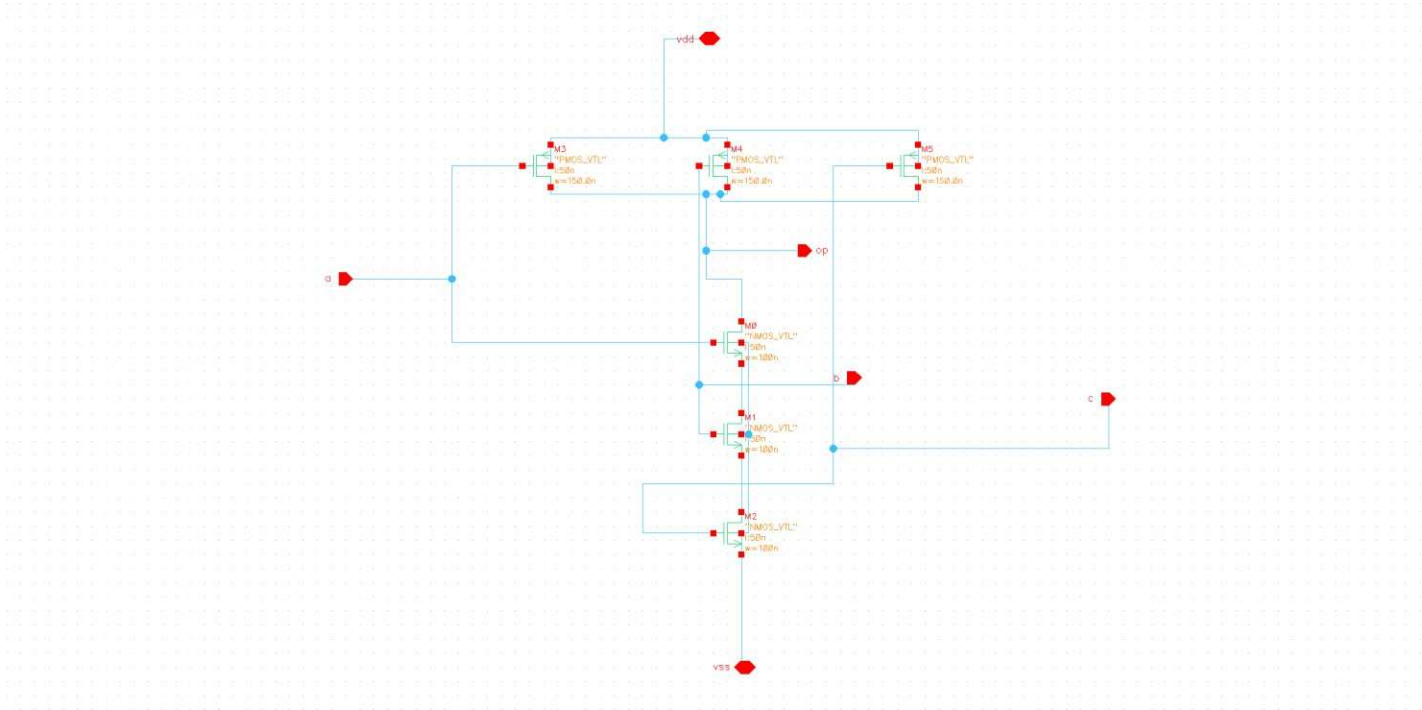
NAND3 SCHEMATIC WITH A PMOS TRANSISTOR WIDTH OF 300:



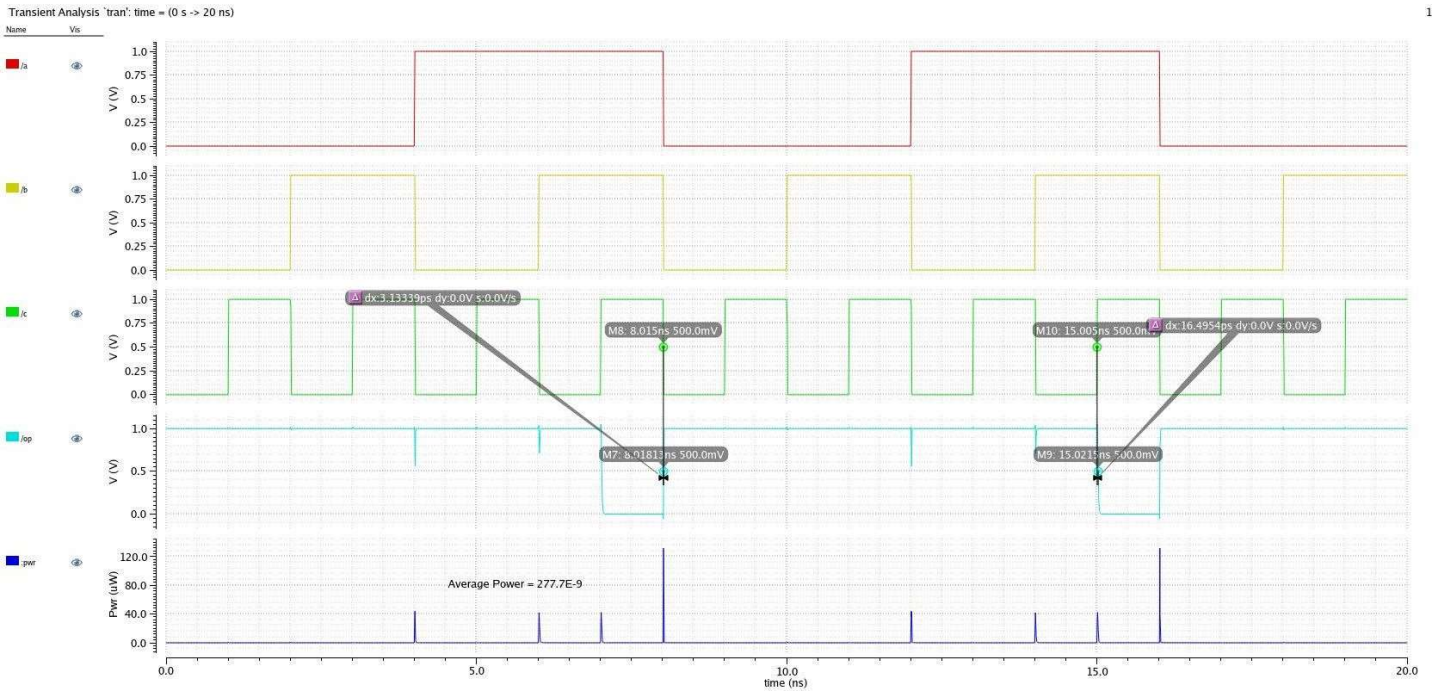
NAND3 WAVEFORM WITH A PMOS TRANSISTOR WIDTH OF 300:



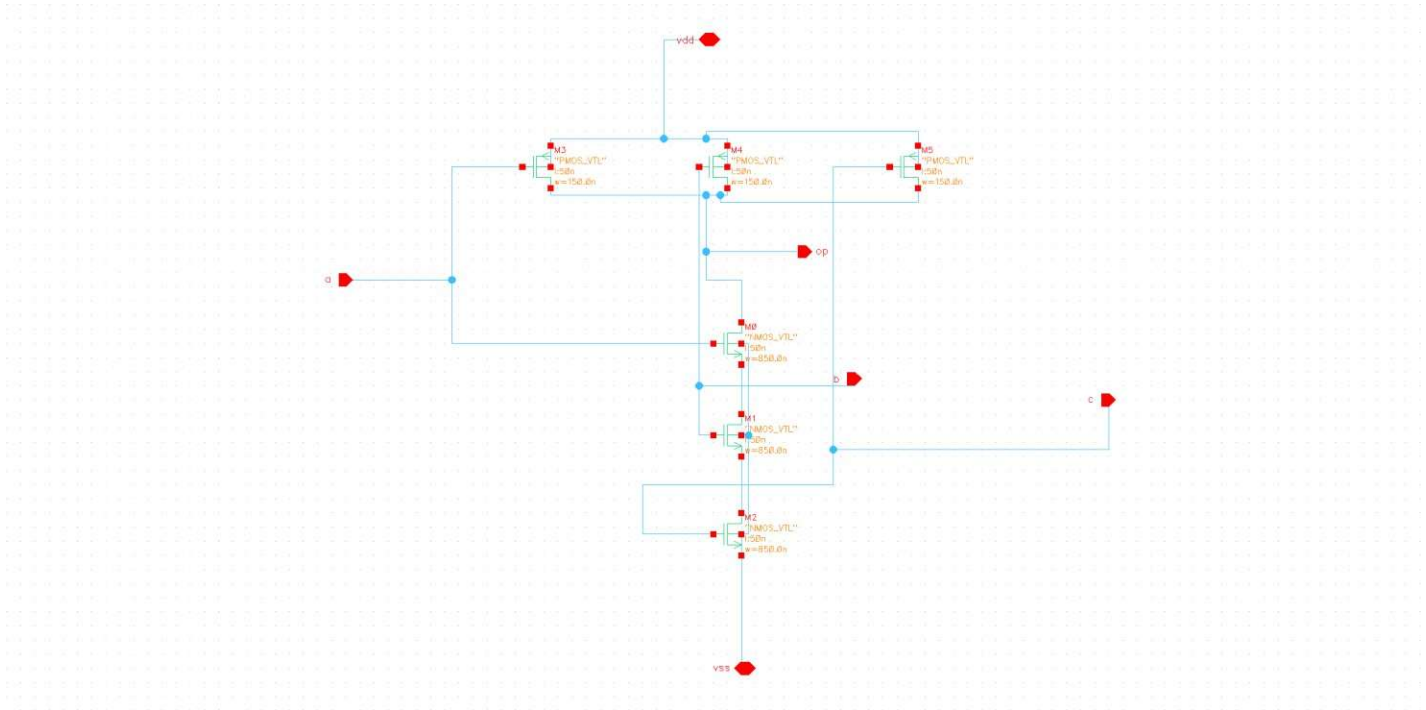
NAND3 SCHEMATIC WITH A PMOS TRANSISTOR WIDTH OF 150:



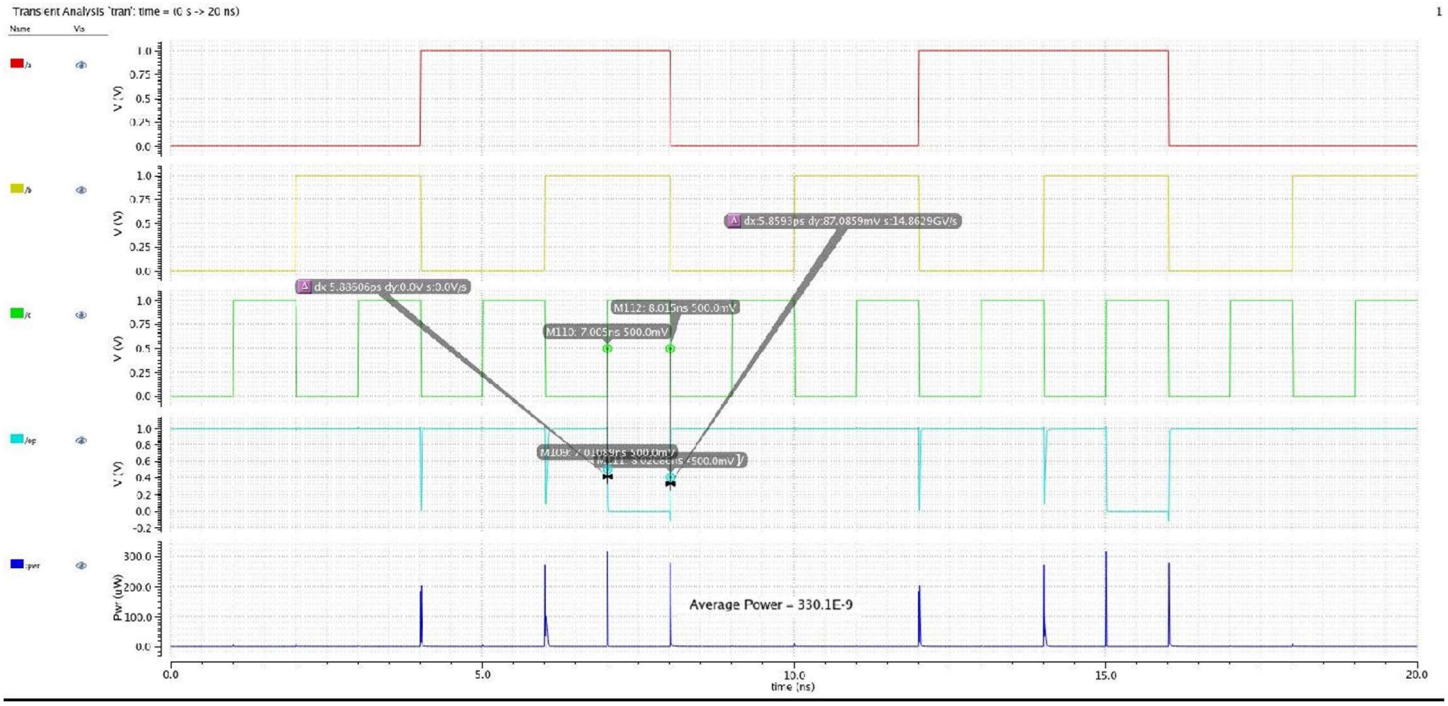
NAND3 WAVEFORM WITH A PMOS TRANSISTOR WIDTH OF 150:



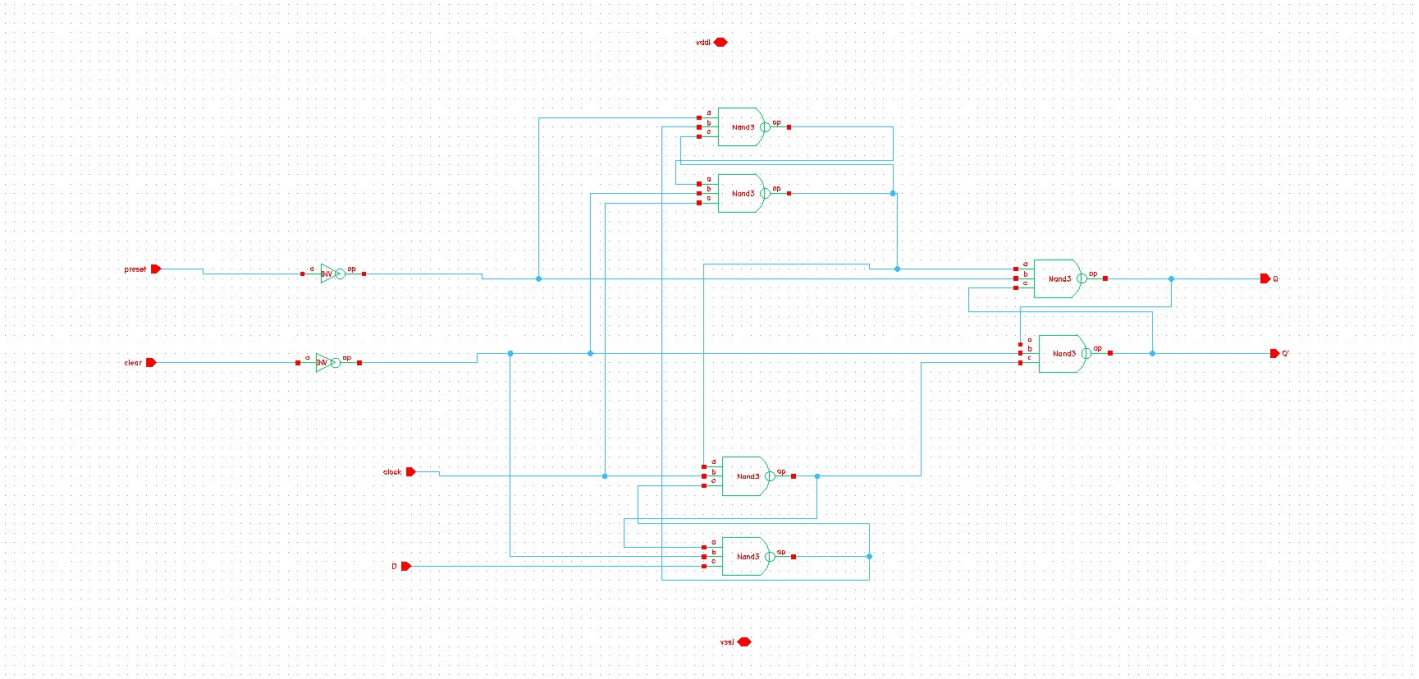
NAND3 SCHEMATIC WITH NMOS TRANSISTOR WIDTH OF 850 TO GET SAME RISNIG AND FALLING PROPAGATION DELAY:



NAND3 WAVEFORM WITH SAME FALLING AND RISING PROPAGATION DELAYS:



D Flip Flop schematic:



D Flip Flop Waveform:

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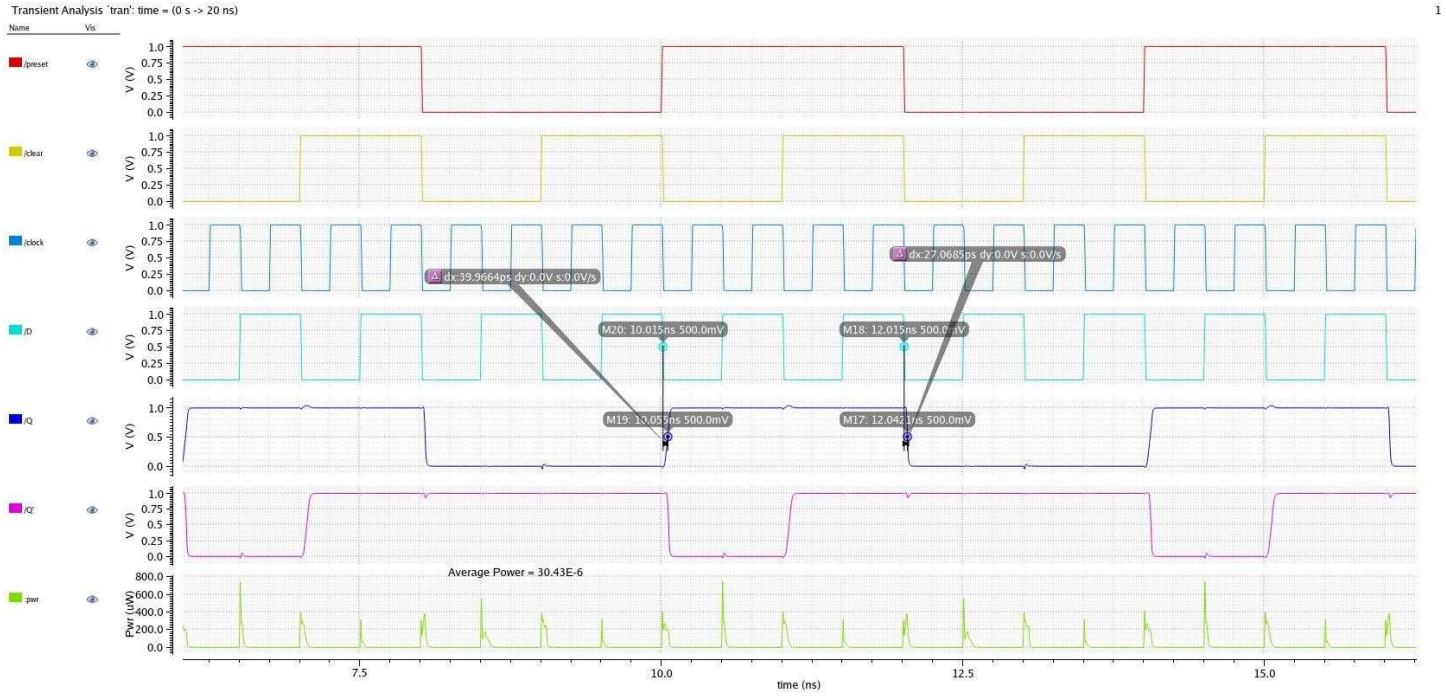
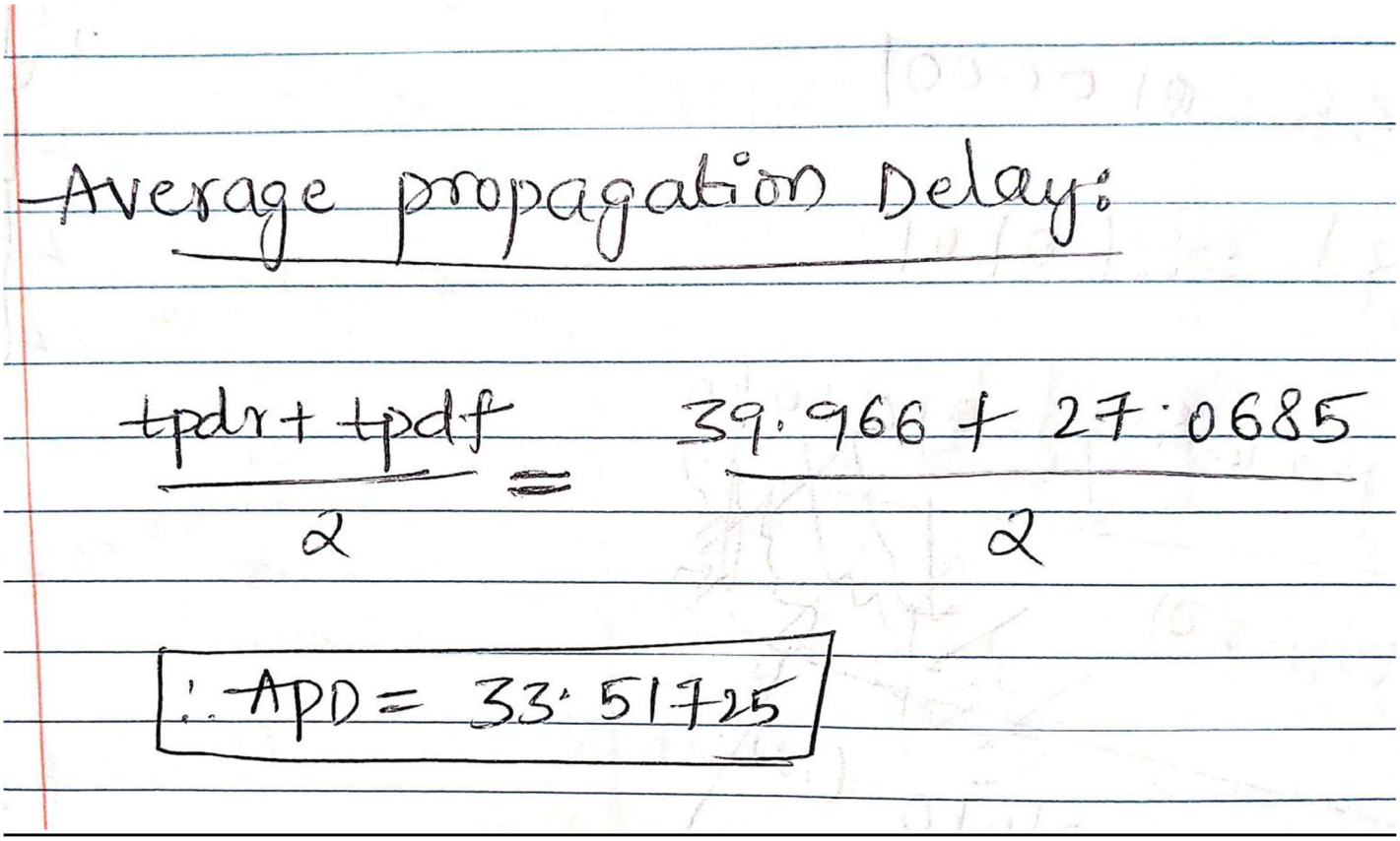
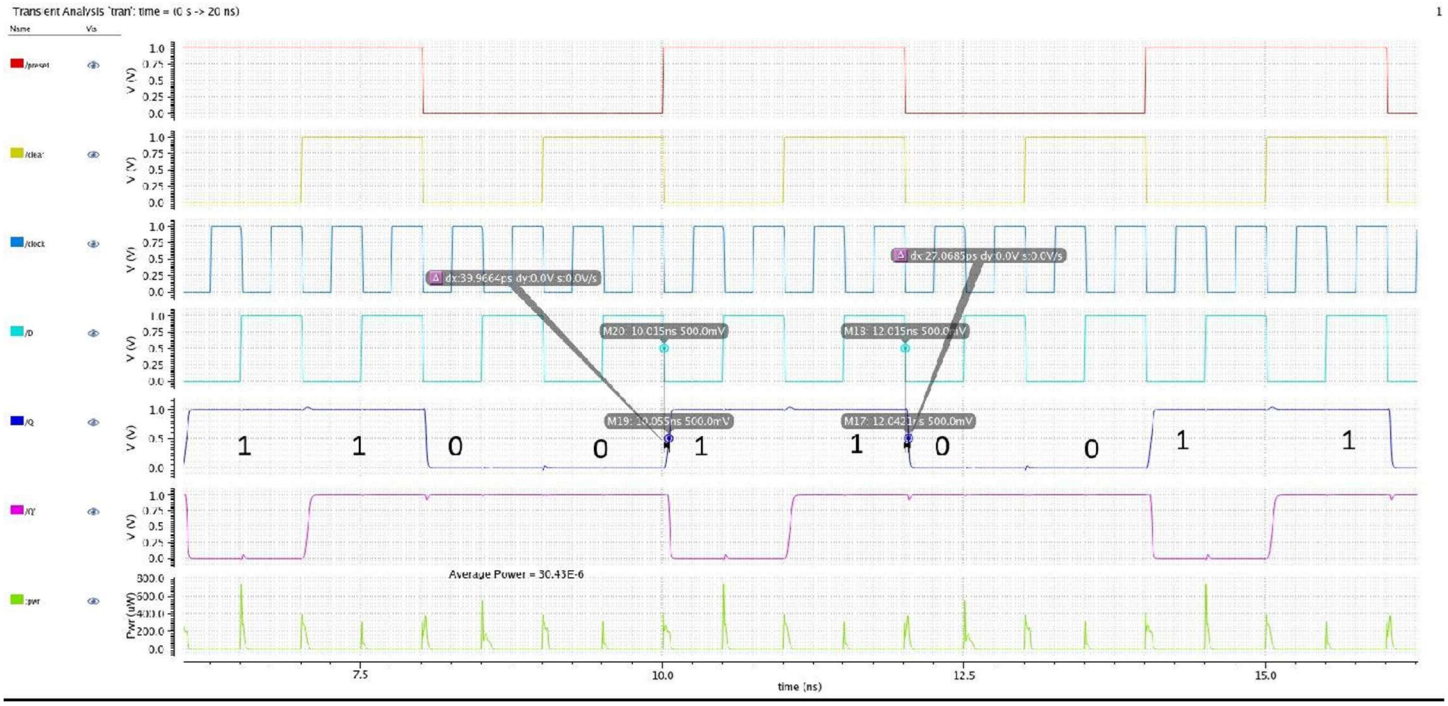


Average propagation delay:



Functional verification (with 0's and 1's on the waveform):



Conclusion:

In conclusion, our lab successfully demonstrated the construction of a D flip-flop using NAND gates and an inverter. We verified its operation and observed how it accurately stores and transfers data based on the input clock signal. This exercise reinforced our understanding of sequential logic circuits and their importance in digital system design. Through practical implementation, we gained valuable insights into the design and functionality of D flip-flops.