EE 4540L/6540L/CEG4322L/CEG6322L

FALL 2023

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Lab section: Lab2

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"I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code"

Signature: Vamshi **Date:10/01/2023**

Report due date: 10/02/2023

AIM/OBJECTIVE:

The main objective of this lab is to create a layout of an inverter and Nand 3 circuit in cadence virtuoso tool.

PROCEDURE

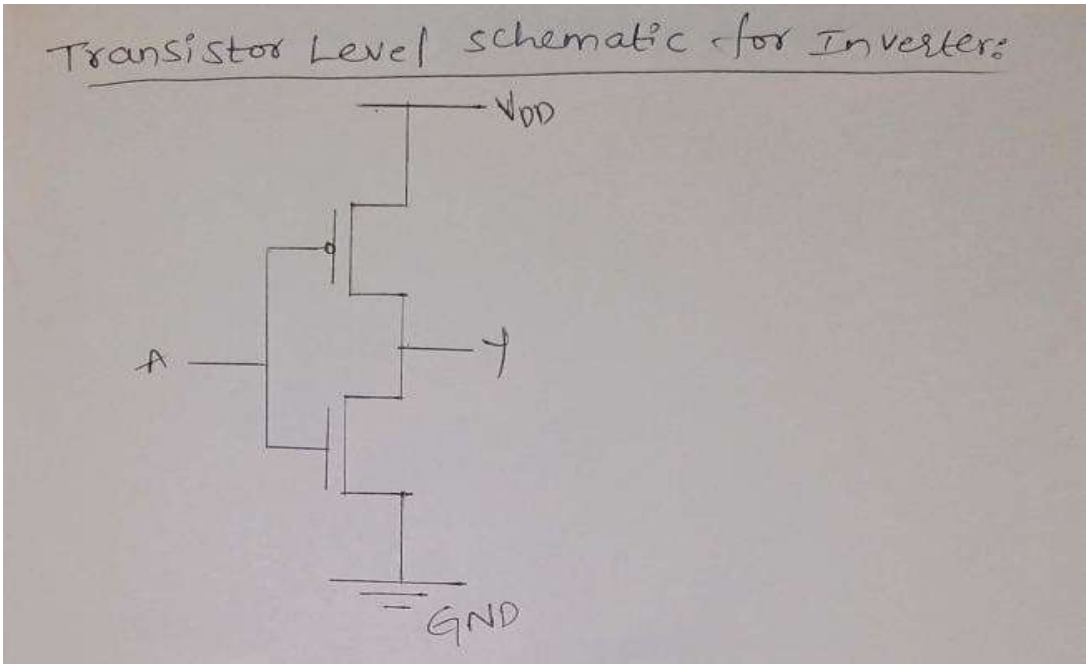
The first step in this lab is to draw transistor level logic.

Then with the help of Euler path we must draw a stick diagram.

And in the last step we must design a layout in the cadence virtuoso tool.

These are the basic steps we must follow in this lab.

Transistor level logic of an Inverter:



After drawing the transistor level logic, we must derive the Euler path from it.

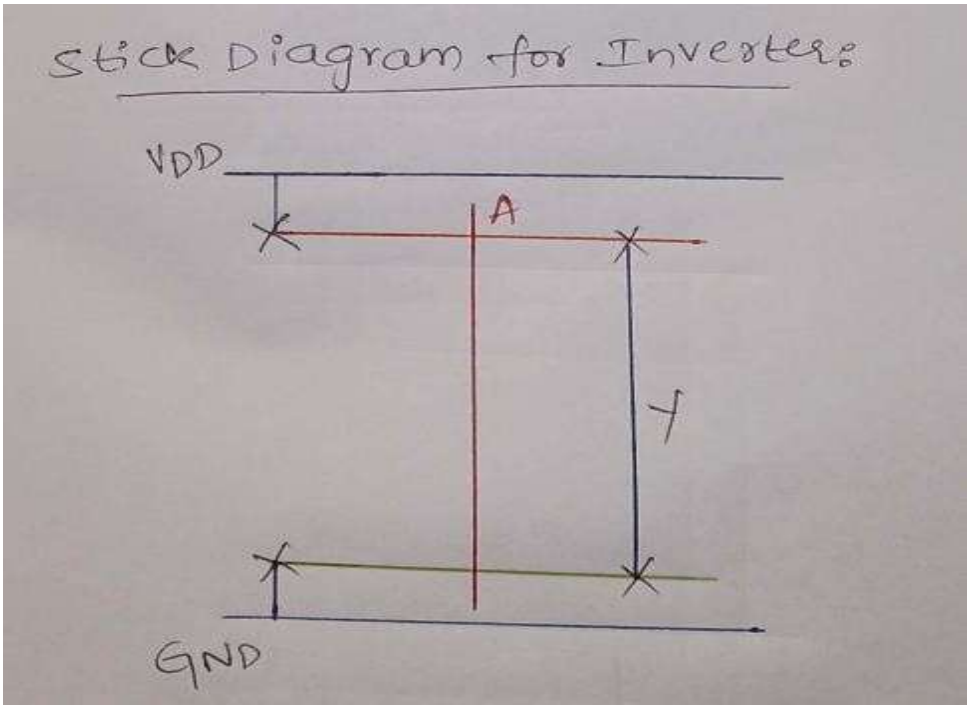
Euler path for pull down Networks

Euler path = {GND, A, Y}

Euler path for pull up Networks

Euler path = {VDD, A, Y}

With the help of Euler path, I had constructed the stick diagram.



In the above stick diagram, I used the following colors for

Blue – Metal 1

Red – Poly

Green – N diffusion

Yellow – P diffusion

Black – Contact

With the help of this stick diagram I had constructed the layout in cadence virtuoso tool.

Procedure for constructing layout in cadence virtuoso tool:

First open the terminal and type virtuoso& and then hit enter

The next step is to create a new library like Lab 2.

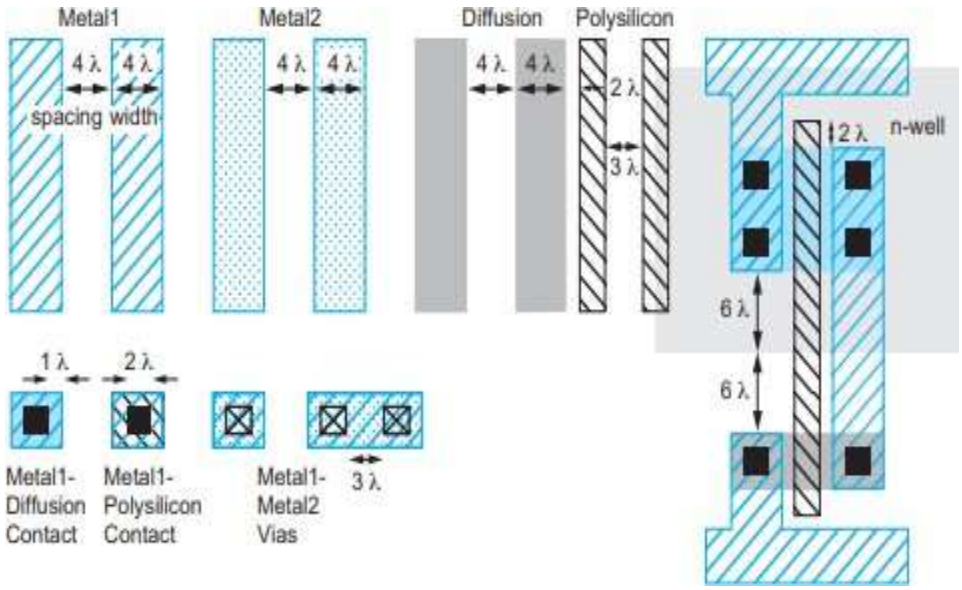
Then create a cell in Lab2

Change the grid options in the new cell.

And then with the design rules start constructing the layouts.

Basic design rules to be followed for constructing layout:

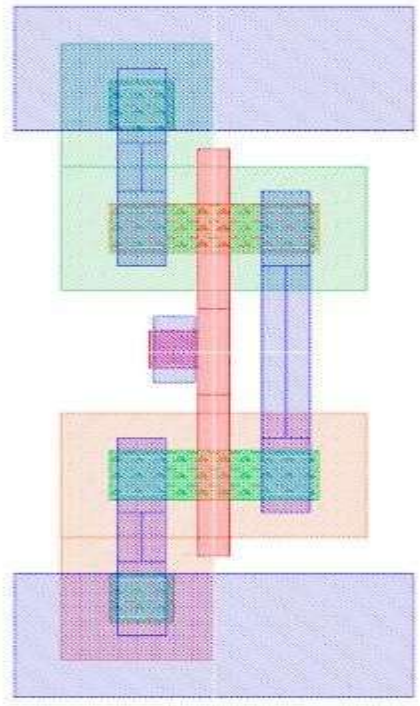
- The minimum width and spacing for metal and diffusion layers is 4 λ.
- Contacts measure 2 λ by 2 λ and require a surrounding area of 1 λ on the layers above and below them.
- Polysilicon should be designed with a width of 2 λ.
- Polysilicon must overlap diffusion by 2 λ in areas where a transistor is to be formed, while maintaining a 1 λ spacing in regions without transistors.
- Additionally, polysilicon and contacts need to be spaced 3 λ apart from other polysilicon or contacts.
- The n-well should be placed 6 λ away from pMOS transistors and kept 6 λ clear of nMOS transistors.



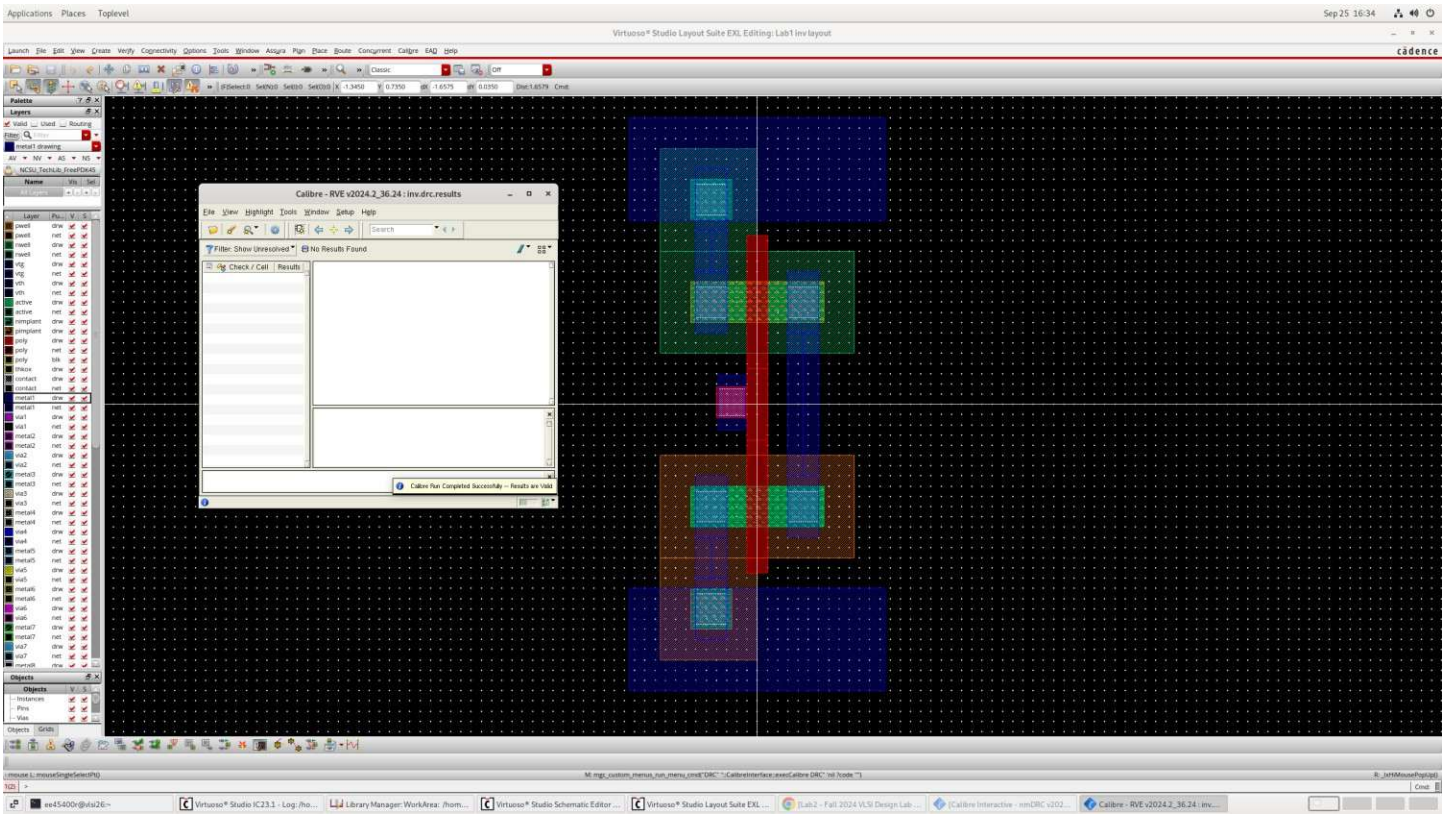
Procedure for constructing an inverter in cadence virtuoso:

- In the layout area, create an active region for the NMOS transistor. Following the design specifications, position the n-implant area 8 λ below the horizontal centerline.
- Then add contacts to the transistor.
- Next step is adding a P well layer to the transistor. And we should ensure that the well surrounds the entire active area by at least 3 λ.
- Add the gate to your transistor using polysilicon. The transistor should consistently have a length of 2 λ and a width of 4 λ.
- Ensure that the polysilicon should extend at least 1.5 λ beyond the well, and the contacts need to be spaced 2 λ away from the polysilicon.
- Form a p-well square that is half the length of the existing p-well surrounding the current n-diffusion region.
- Inside this new p-well area, create both an active region and a p-implant square, adhering to the 3 λ spacing rule.
  - Additionally, place a contact within the new active area, following the 0.5 λ spacing guideline.
  - The next step is to add metal 1 to the contacts and this helps for connections to the contacts.
  - Next, draw the complementary p-type transistor. It's essential that the well areas are spaced at least 9 λ apart to prevent design rule violations. In this case, a spacing of 10 λ was selected to align more effectively with the major spacing markers.
  - And then I copied the NMOS transistor and mirrored it and then I changed the properties from p well to N well and P implant to N implant.
  - Next step is to run a design rule check, once there are no DRC errors then we must route the inverter. It includes making VDD, VSS and output connections.
  - Finally, once again run DRC and if there are any errors we have to fix in the layout.
  - And then we must save the design.

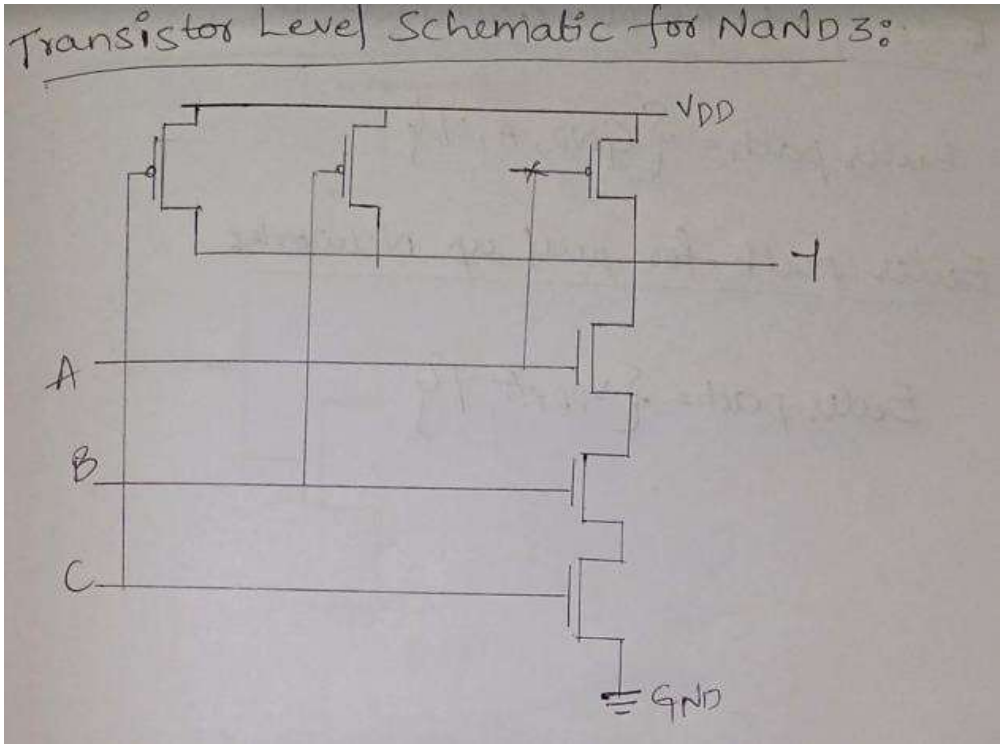
Layout for Inverter:



After following all these above rules, I constructed an inverter with no DRC errors.



Transistor level logic of NAND3:



After drawing the transistor level logic, we must derive the Euler path.

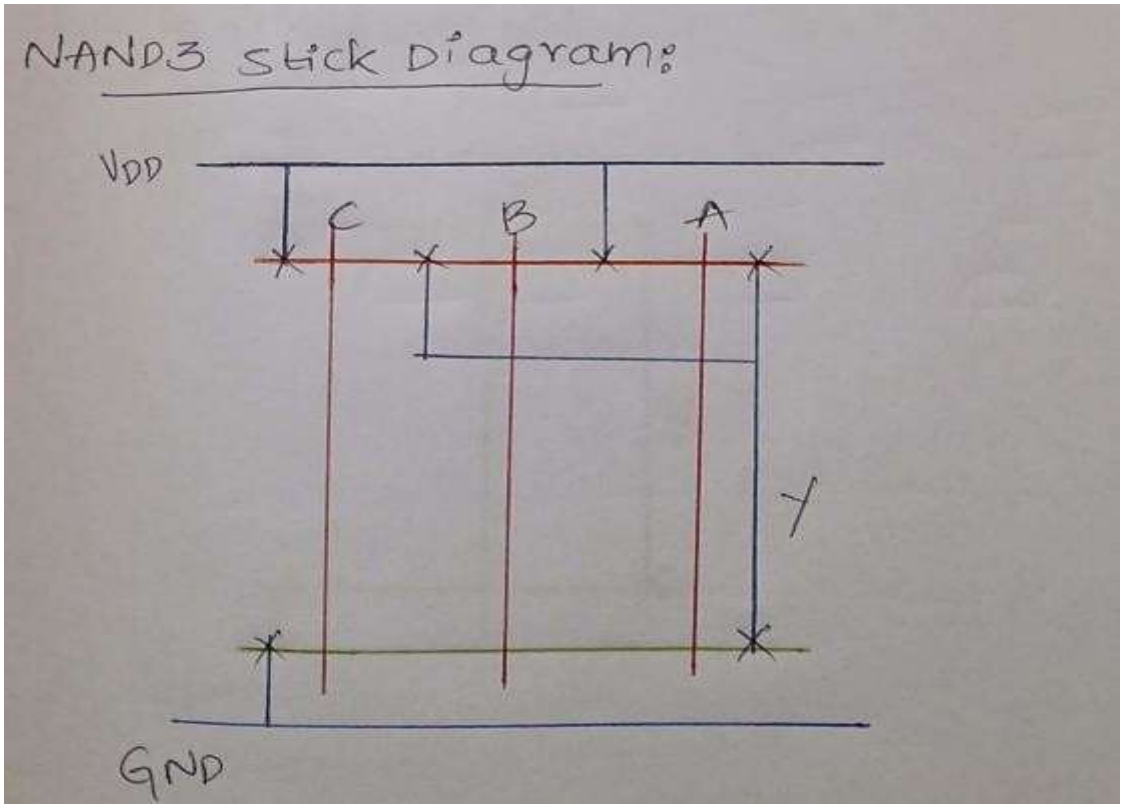
Euler path for pull down Network:

Euler path = {GND, C, B, A, Y}

Euler path for pull up Network:

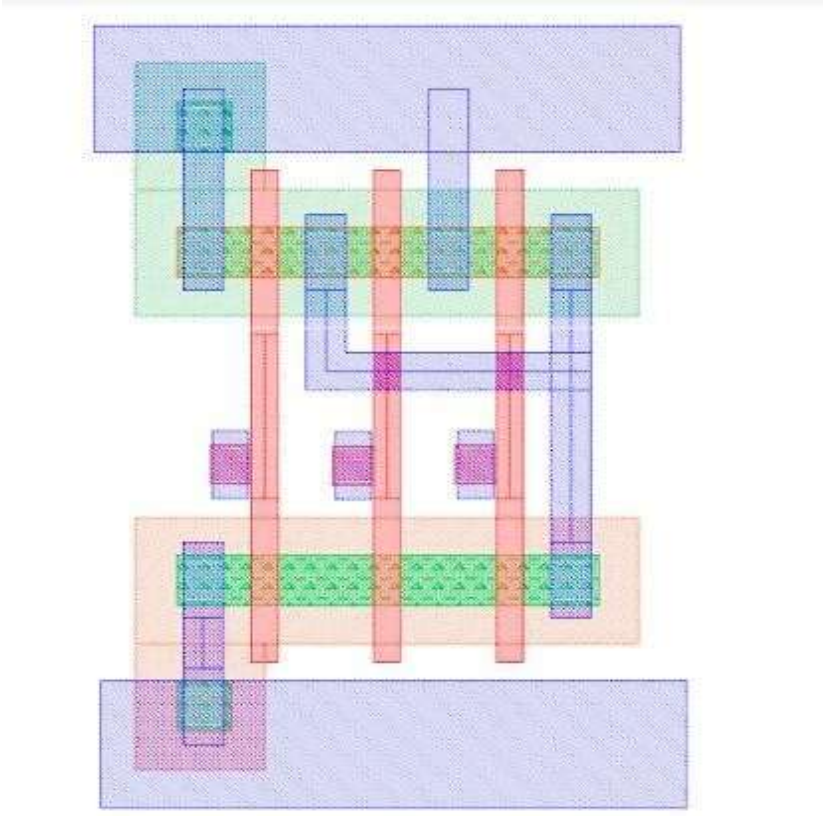
Euler path = {VDD, C, Y, B, VDD, A, Y}

With the help of Euler path we can construct a stick diagram for NAND3.

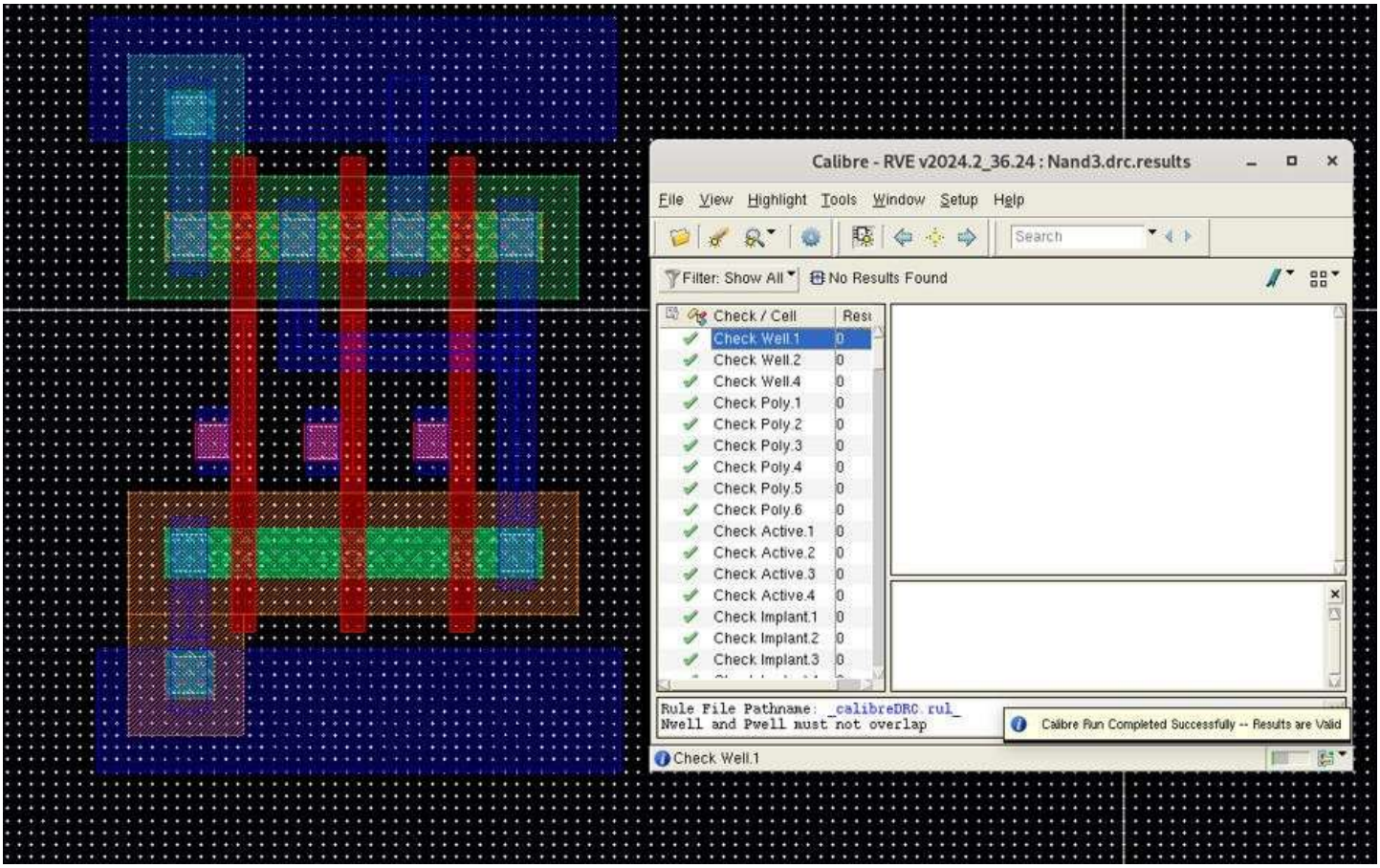


Now with the help of stick diagram we can easily construct a layout for NAND3 in cadence virtuoso tool.
I had followed the same design rules that I had used to construct an inverter layout.

Layout for NAND3:



After following all the mandatory rules, I had constructed NAND3 without any DRC errors.



Conclusion: Therefore, I implemented Inverter and NAND3 layout in cadence virtuoso tool.