Design of High Performance 8-bit Vedic Multiplier

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***Abstract*—Multiplier is an essential functional block of a microprocessor because multiplication is needed to be performed repeatedly in almost all scientific calculations. Therefore, design of fast and low power binary multiplier is very important particularly for Digital Signal Processors. This paper describes a design of fast and low power 8-bit multiplier architecture which implements Urdhva-tiryakbyham sutra of Vedic method of multiplication. The multiplier is designed in 180nm technology using cadence EDA tool and simulated using spectre simulator and found to be working correctly and results have been compared foe pre-layout and post-layout analysis. It is shown that implementation of multiplier using the Vedic sutra leads to a very compact layout leading to significantly smaller Silicon area and very small contribution of interconnections to the overall propagation delay of the multiplier. The performance of the proposed multiplier has been compared with those of other multipliers reported in literature.**

Keywords— Full adder (FA); Half adder (HA); Partial products; Urdhva-tiryakbyham (UT); Vedic arithmetic; Wallace tree.

I. INTRODUCTION

The fast and low power multipliers are required in small size wireless sensor networks and many other DSP (Digital Signal Processing) applications. In implementation of many algorithms such as Fast Fourier Transforms (FFT), Discrete Fourier Transform (DFT) etc, high speed and low power multipliers are of critical importance [1-2]. Two basic multiplication methods namely Booth multiplication algorithm and Array multiplication algorithm have been used for the design of multipliers [3-4]. It has been reported that Booth multiplication algorithm provides for faster multiplication only if operand sizes are small [5]. For fast multiplication, array multipliers are used. This method provides for faster multiplication because all the partial products are obtained simultaneously using AND gates. In array or parallel multipliers the speed of multiplication (as well as power dissipation) is dominantly controlled by the propagation delay of the full / half adders used for the addition of partial products. The schemes for efficient addition of partial products such as Wallace tree [6]; Dadda tree [7] and use of compressors [8] have been reported in literature [9]. Wallace tree multiplier gives the best performance but suffers from disadvantage of highly irregular structure which means that it requires a larger area and involves a complex interconnection which is more difficult to implement.

The overall propagation delay of a multiplier comprises of the delay caused by the transistors and the delay contributed by the interconnect resistance and capacitances. In the array multiplication scheme, the interconnects become more and more complex and lengthy as the operand size increases. The Vedic multiplication method which is basically array multiplication method permits the use of a highly recursive type multiplier architecture resulting in significant improvement in the speed [10-14]. While the same no of basic operations such as AND or 1 bit addition are needed to be performed in Vedic multiplication method and conventional array multiplication method, the layout of Vedic multiplier is highly compact resulting in very small contributions of interconnects to the overall propagation delay as the operand size increases. The importance of using high speed, low power, and low transistor count full adders remains same in Vedic multipliers also.

In this work the adders used in the multiplier are 9T CMOS half adders and 20T low power and high speed CMOS full adders [15]. These adders have been designed using smallest area transistors and a circuit the layout of which requires smaller chip area. The smaller layout area leads to smaller interconnections and reduced propagation delay. The performance of the proposed multiplier has been evaluated for both the schematic and layout designed using UMC 180 nm technology file, at 1.8V supply voltage.

Section II describes the Vedic multiplication method and in section III, a 20T fast and low power full adder reported in [15] has been discussed. In section IV, the proposed 8-bit Vedic multiplier has been discussed and its performance evaluation has been presented in section V. Section VI concludes the paper.

II. VEDIC MULTIPLICATION

Vedic multiplication method is described by Urdhva-tiryakbyham sutra of Vedic arithmetic. The sutra literally means vertically and cross-wise. The application of this method for 8-bit multiplier is shown in Figure 1. The bidirectional arrows indicate the 4 bit numbers to be multiplied. The bits of the multiplier and multiplicand are represented by hollow dots. The grey dots represent the carry from the multipliers and the black dots represent the carry from the full adders of the first reduction stage. It can

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be seen from the diagram that the output of the multiplier is obtained after 2 stages of binary addition. The first reduction stage uses full adders while in the second reduction stage k-bit binary adder (k is equal to [(3/2) m –1] where m is the number of bits in the operands) is required.

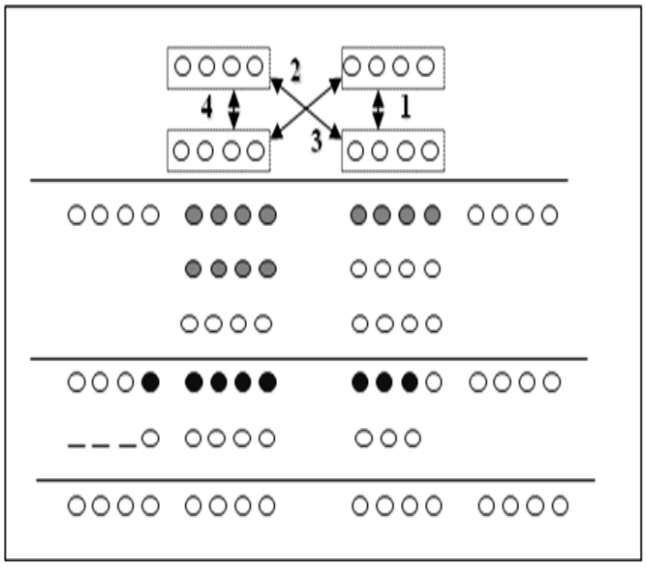

Fig. 1. 8X8 multiplication using UT sutra [1]

Block diagram of a (m x m) binary multiplier based on Vedic arithmetic is shown in Figure 2. It is seen that for (m x m) multiplier, 4 numbers of (m/2) x (m/2) multipliers are required. In addition, the first reduction layer requires 'm' full adders and second reduction stage requires a k-bit binary adder.

From the above described architecture of multiplier it can be seen that for designing a high speed, low power multiplier, it is required that full adders must consume low power and provide for high speed. In addition for k-bit binary adder low power, high speed full adders with efficient scheme for carry generation and propagation is required. Because for large size operands, the value of 'k' will be large so carry look ahead adder scheme is not suitable for the above mentioned k-bit adder.

This architecture is regular. It is highly recursive in nature for designing an m-bit multiplier. The recursive nature of Vedic multiplier permits the design of highly compact layout that is silicon area used is minimum. The compact layout also ensures that the interconnect length is minimum which also leads to higher speed. Further, this architecture is such that the bigger multipliers can be easily built just by adding an adder block and using the smaller multipliers as functional blocks. This permits the reuse of smaller multipliers to a great extent.

I. Full Adder

The multiplication time and power dissipation of a multiplier almost entirely depends on propagation delay and the power dissipation of FA circuits used in the multiplier. For designing a low power and high speed multiplier it is necessary that FA's used in the multiplier must consume minimum power and provide highest speed. In addition to the above, FA should also have equal delay from input to both the outputs i.e. Sum and Carry. This feature will ensure that glitches are minimum.

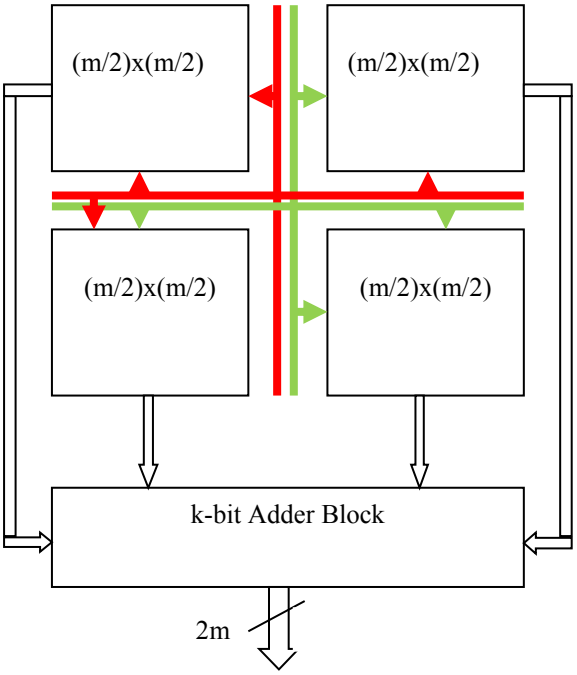

Fig. 2. m x m multiplication using UT sutra [16]

In this work, the 20T FA reported in [15] is used. The circuit of the full adder is shown in Figure 3. The SUM (S) output has been generated using two XOR gates. The XOR function is obtained using pass transistors based XNOR gate followed by an inverter to restore the logic levels. For generating the Carry output, transmission gates have been used instead of single pass transistor to pass inputs A or C. This results in improved logic level at the output of the transmission gate leading to fully restored logic level at Carry (Cout) output a little after one XOR delay because the outputs of first XOR gates of all the full adders are generated in parallel. As a result Carry output is available before the Sum output. The propagation delays from A to Sum and Carry outputs delay are given in TABLE I. The advantage of this FA circuit is that the all the transistors are minimum area transistors i.e. 360n/240n for pMOS and 240n/180n for nMOS. Many other full adder circuits have been reported in the literature. A review of all these circuits has been given in [15]. The performance 28T C-CMOS has been shown to be comparable to the best performance obtained with any other CMOS full adder circuit reported earlier. This circuit also provides a very compact layout of the FA circuit as shown in Fig.4.

Since the number of full adders to be used is rather large, a compact layout is an important requirement for achieving small propagation delay and power consumption.

It has been shown that this full adder [15] provides fully restored logic levels with almost glitch free output up to a switching frequency of 500 MHz with relatively low power consumption because of small area transistors used.

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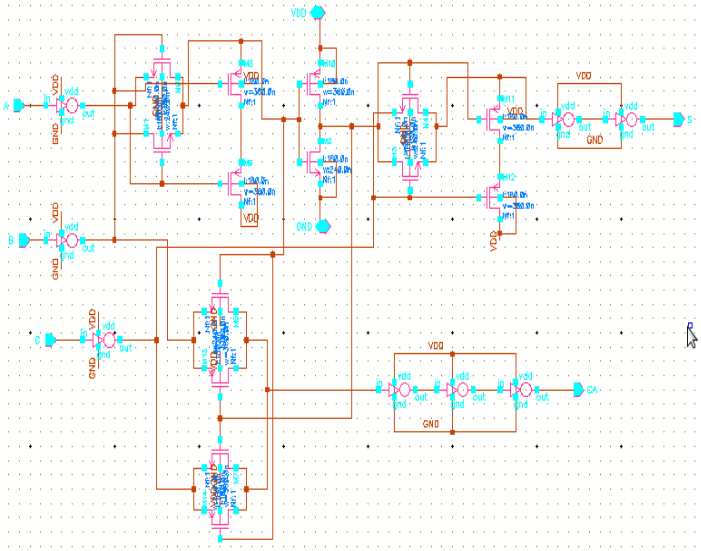

Fig. 3. Schematic of 20T Full Adder [15]

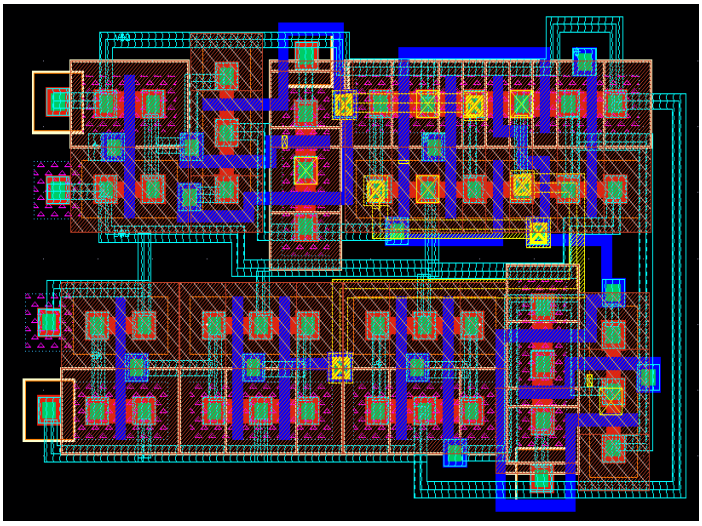

Fig. 4. Layout of Full Adder

The performance of 20T FA circuit is evaluated using Cadence EDA tool (Spectre simulator, Calibre (for parasitic extraction)). The propagation delay as obtained for the FA circuit is compiled in TABLE I.

TABLE I
PROPAGATION DELAY OF FULL ADDER FOR THE PRE LAYOUT AND POST LAYOUT SIMULATION

Full Adder	**Pre layout (ps)**		**Post Layout (ps)**	
	Min.	**Max.**	**Min.**	**Max.**
A to Sum	177.1	268	237.5	401
A to Cout	171	294	222.5	450
Cin to Cout (when Cout change)	171	202.5	222.5	267.5
Cin to Cout (when Cout does not change)	1	1.5	11	14

The performance figures presented in TABLE I indicate that Carry output is available before the Sum output. It is also seen that in case the value of Cin is such that Cout is not required to change then Cin skips to Cout with negligible delay. This makes k-bit adder faster.

The power dissipation of FA was evaluated at the switching frequency of 500MHz. For different input combinations power dissipation is different. It was evaluated for one combination i.e. when all the inputs switch from 1 to 0 or 0 to 1. The average power consumption was determined to be 55µW for pre layout simulation and 72 µW for post layout simulation i.e. with parasitics.

II. PROPOSED 8-BIT MULTIPLIER

The schematic of the proposed 8-bit multiplier implemented using Vedic arithmetic is shown in Fig.5. The layout of the proposed 8-bit multiplier has been designed using Cadence Virtuoso in 180nm CMOS technology is shown in Fig.6. The performance of the multiplier was evaluated by simulation with the power supply voltage of 1.8 volt using Spectre simulator in Cadence Virtuoso for the schematic shown in Fig.5. The post layout performance evaluation of the multiplier was carried out after parasitic extraction using Calibre. The simulation results for the propagation delay are given in TABLE II. The waveforms of some of the multiplier outputs are shown in Fig.7 for pre layout simulation and in Fig.8 for post layout simulation. It can be seen that the output signals are almost glitch free and the logic levels are fully restored.

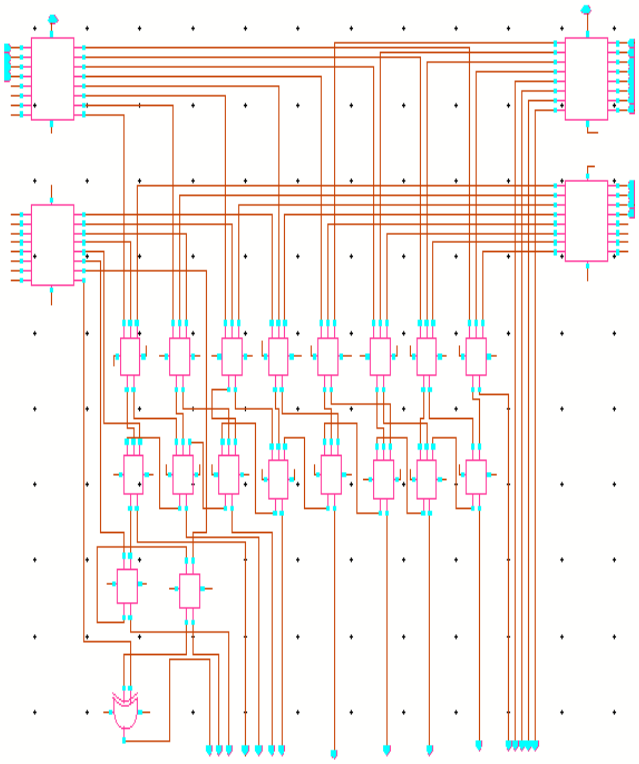

Fig. 5. Schematic of 8-bit multiplier

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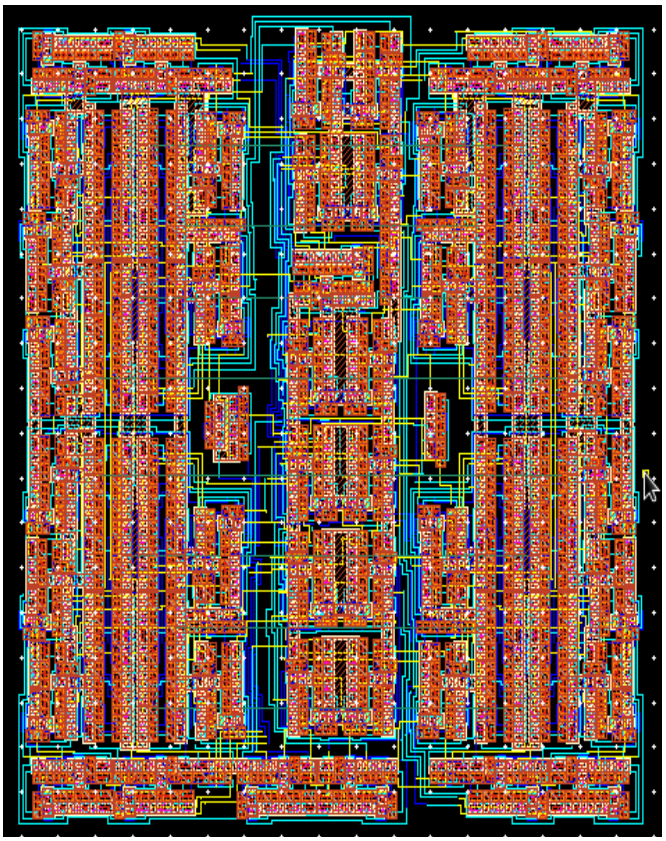

Fig. 6. Layout of 8-bit multiplier

III. Performance Analysis

Performance analysis of the proposed multiplier is performed using Cadence EDA tool in UMC 180nm technology at 1.8V power supply and parasitic extraction is done using Calibre. The pre-layout and post-layout simulation has been done to analyse the operating speed (i.e. propagation delay) and power dissipation (evaluated at 100MHz) of the proposed multiplier. The transistor count, Layout area and its performance is also compared with existing architectures to show the effectiveness of the proposed architecture.

The propagation delays from A0 to M9 and A0 to M15 in 8-bit multiplier and corresponding input/outputs in 4-bit multiplier as obtained by simulation are compiled in TABLE II.

TABLE II
PROPAGATION DELAY FROM A0 TO M5, A0 to M7 FOR 4 BIT AND A0 TO M9, A0 TO M15 FOR 8-bit MULTIPLIER AND FOR PRE LAYOUT AND POST LAYOUT SIMULATION

4bit multiplier			
A0 to M5		**A0 to M7**	
Pre layout (ns)	**Post layout (ns)**	**Pre layout (ns)**	**Post layout (ns)**
0.875	1.4	0.282	0.42

8-bit multiplier			
A0 to M9		**A0 to M15**	
Pre layout (ns)	**Post layout (ns)**	**Pre layout (ns)**	**Post layout (ns)**
1.5	2.5	0.416	0.764

It is seen that A0 to M9 propagation delay is larger than A0 to M15 which is the MSB. This is because of the carry skip adder used. This is explained below.

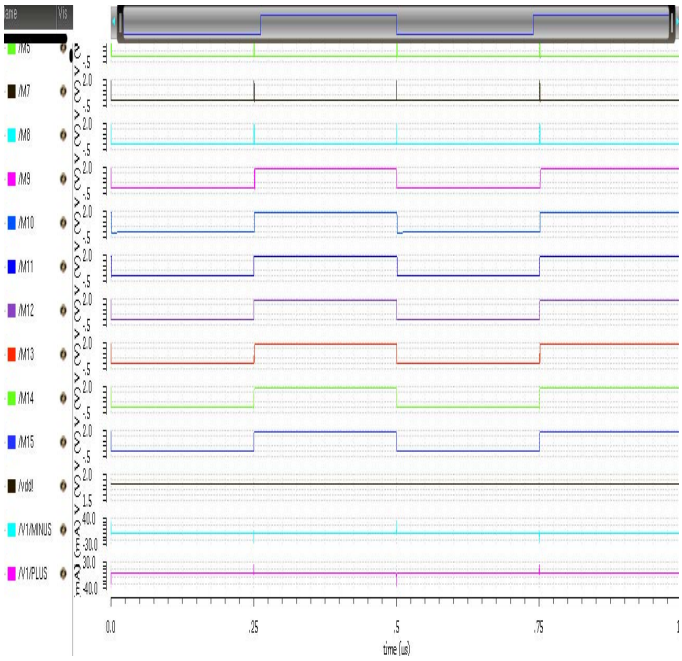

Fig. 7. Waveform of 8-bit Vedic multiplier for pre layout Simulation

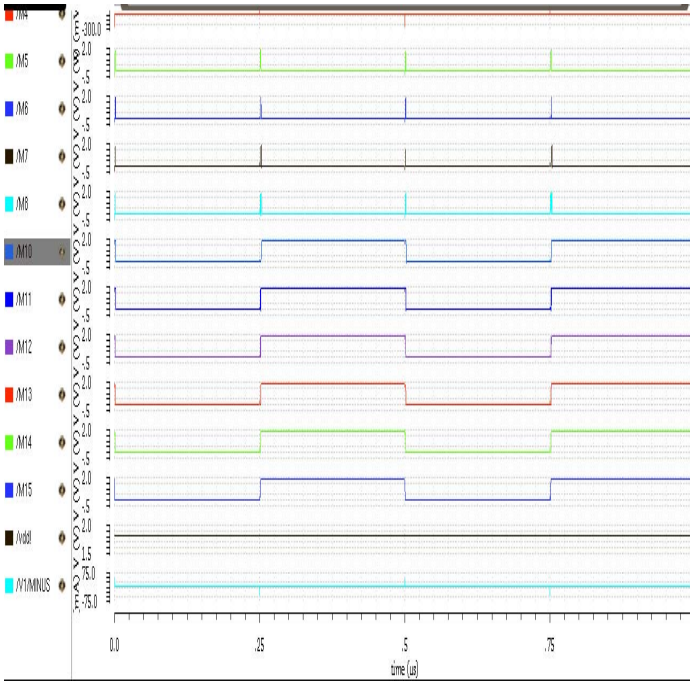

Fig. 8. Waveform of 8-bit Vedic multiplier for post layout Simulation

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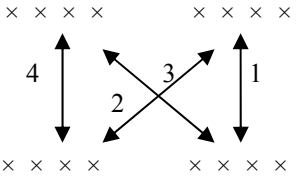
From the Line diagram shown in Fig.9, it can be seen that propagation delay to the output terminal will be large if Carry output of each FA used in second reduction stage changes. For the worst case when all the multiplicand bits are 1 a new carry is generated at each FA stage up to M9. Beyond these stages the carry simply skips the intermediate stage so that M15 is obtained earlier than M9. Same trend was observed in 4 bit multiplier also in which M7 is obtained earlier than M5.



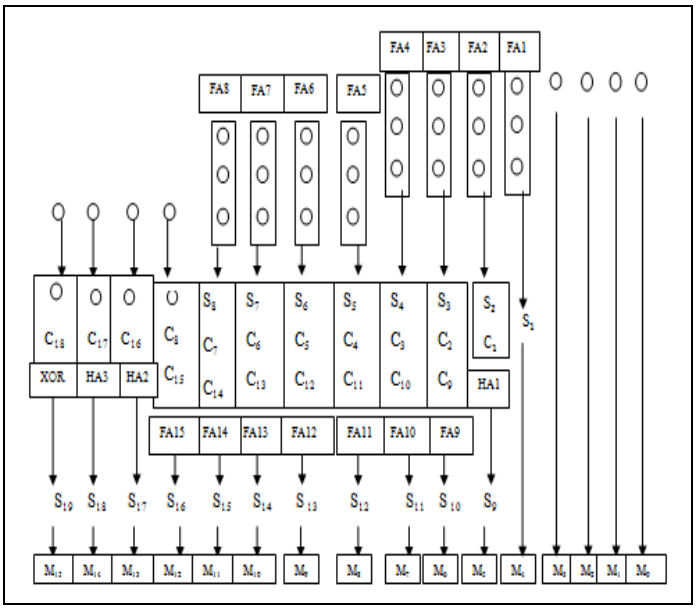


Fig. 9. Line diagram of 8-bit Vedic multiplier

The comparison of transistor count and the silicon area of the proposed multiplier with other Vedic multipliers reported in [18] are given in TABLE III.

TABLE III
TRANSISTOR COUNT AND THE LAYOUT AREA

Name of Topology	Tranistor Count			Layout Area(in um^2)	
	45nm [18]	180nm [20]	180nm (This work)	45nm [18]	180nm (This work)
4bit vedic multiplier	320*	514	417	549.31	1364.454
8bit vedic multiplier	1648*	2634	2151	5080.38	7454.564

*The FA used in the multiplier is 14T

It is seen from TABLE III that the number of transistors used in [18] are smaller than that the number of transistors used in the proposed multiplier. This is because FA used in this work is 20T in comparison to 14T FA used in [18]. However the silicon area consumed by the multiplier in this work is relatively much smaller because of the fact that the transistors used in the 20T FA circuit are minimum area transistors while the 14T [15] uses large area transistor.

The comparison of the propagation delay of the Vedic multiplier designed in this work with other 8-bit multipliers reported in [18-20] is given in TABLE IV.

TABLE IV
PERFORMANCE COMPARISON WITH OTHER MUTIPLIERS

Name of The 8-bit Vedic multiplier	Technology	Propagation Delay (ns)			
		Pre Layout		Post Layout	
		A0 to M9	A0 to M15	A0 to M9	A0 to M15
8-bit Vedic Multiplier	180nm(This work)	1.5	0.416	2.5	0.754
	45nm[18]	0.635**		3.479**	
	90nm[19]	2.02**		--	
	180nm[20]	13.36**		--	

** Not specified whether it is from A0 to M9 or A0 to M15

It can be seen that the propagation delay obtained in the proposed Vedic multiplier is much smaller than that reported in literature [18-20].

IV. Conclusion

The paper presents the design of 8-bit Vedic multiplier implemented in UMC 180nm technology using Cadence virtuoso tool. The multiplier was tested for the correct performance by simulation using Spectre simulator. Both pre-layout and post-layout simulations have been carried out to determine the propagation delay. It has been shown that implementation of Vedic multiplication method results in highly compact layout leading to small contribution of interconnections to the overall propagation delay. This is clearly indicated by relatively small difference between pre-layout propagation delay and post- layout propagation delay as obtained by simulation. The speed of the proposed multiplier design has been shown to be significantly better than those reported earlier. It has been pointed out that Vedic multiplication method offers the advantage of design reuse in the sense that (m/2) x (m/2) multipliers and k- bit binary adders can be reused for design of (m x m) multiplier.

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