CMOS PROJECT

Comparative Analysis of 2-Bit Vedic Multipliers: Traditional CMOS vs. Gate Diffusion Input (GDI) Logic vs. Modified Gate Diffusion Input (MGDI) Logic

(By Vanashree Parate)

Abstract:

This study presents a comparative analysis of three different CMOS layout methodologies applied to a 2-bit multiplier: the conventional CMOS layout, the innovative Gate Diffusion Input (GDI) CMOS layout and the Modified Gate Diffusion Input (MGDI) layout. The objective is to investigate how these layout approaches impact the performance and efficiency of the multiplier circuit. Key parameters such as power consumption, area utilization and transistor count are evaluated to discern the trade-offs between the three methodologies. Through this analysis, insights are provided to aid in the selection of the most suitable layout for arithmetic circuit implementation. The software used are MICROWIND 3.1 and DSCH 2 for layout and designing on 90nm technology.

Introduction:

Digital circuit design plays a pivotal role in modern electronic systems, with arithmetic circuits like multipliers forming essential components [1]. The efficiency and performance of these circuits are heavily influenced by the chosen layout methodology. In this study, we focus on comparing three distinct CMOS layout approaches for a 2-bit multiplier: the traditional CMOS layout, the Gate Diffusion Input (GDI) CMOS layout and the Modified gate Diffusion Input (MGDI) layout.

At circuit/logic level, different CMOS logic design techniques like CMOS complementary logic, Pass Transistor Logic, Pseudo NMOS, Cascade voltage switch logic , Dynamic CMOS, Clocked CMOS logic , CMOS Domino logic, Modified Domino logic and transmission gate logic (TG) have been proposed to reduce power consumption. The MGDI technique allows solving most of the problems occurring in above mentioned various CMOS and PTL techniques. The MGDI technique compared to other techniques allows reduced power dissipation, lower time delay, lower count of transistors and area of digital circuits while maintaining reduced complexity of circuit logic. [5]

By conducting a comparative analysis of these layout methodologies, we aim to provide insights into their respective strengths and weaknesses in the context of 2-bit multiplier design. Key parameters such as power consumption, area utilization and transistor count will be evaluated to elucidate the trade-offs inherent in choosing between traditional CMOS and GDI CMOS layouts. The findings of this study aim to inform future design decisions and contribute to the ongoing optimization of digital circuitry for diverse applications in computing and beyond.

GDI Logic:

Gate Diffusion Input technique is named itself because of one of the inputs are directly diffused into the gates of NMOS and PMOS transistors. GDI reduces power dissipation and area of digital circuits. [3]

The GDI cell contains 3 inputs:

1) G (Common input to the gate of PMOS and NMOS)

2) N (input to the source/drain of NMOS)

3) P (input to the source/drain of PMOS)

N, P, G terminals are could be given to a power supply 'Vdd' or can be grounded or can be supplied with input signal hence effectively minimizing the number of transistors used in case of most logic circuits, leading to smaller area and potentially lower power consumption.

GDI decreases both gate leakage current and sub threshold leakage current as compared to traditional CMOS. But its performance depreciates when used in and below 90nm technology. When the substrate is attached to source, body effect is destroyed. [4]

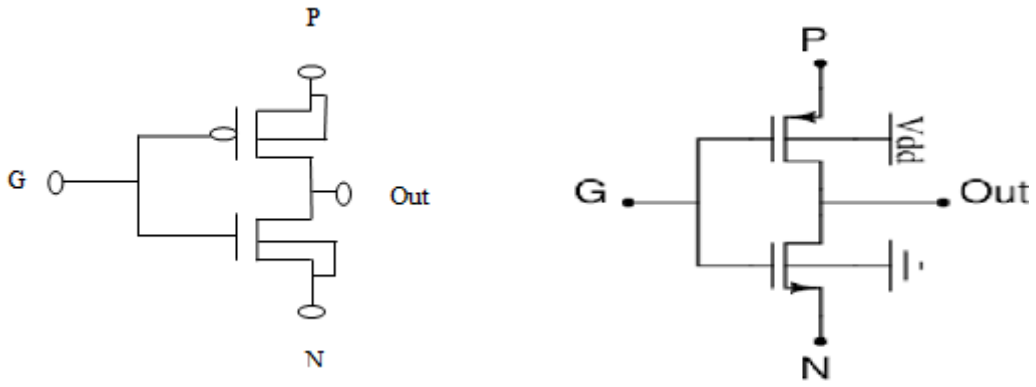


Fig 1: (a) GDI Cell (b) MGDI Cell

MGDI Logic:

MGDI is a new technique adopted from GDI technique. MGDI technique is used to reduce power dissipation, transistor count and area of digital circuits.

Its structure is same as GDI cell except substrates of NMOS and PMOS are connected to ground and Vdd respectively.

MGDI overcomes the drawbacks of GDI cell with improved logic swing [3]. This configuration provides suitability for fabricating the logic cells in CMOS n-well and p-well process, whereas, fabrication of basic GDI cell is not possible in traditional p well progression. Leakage and switching power are lower than traditional. It improves swing degradation and static power characteristics.[4]

Implementation of XOR Gate and AND Gate using GDI logic vs CMOS logic:

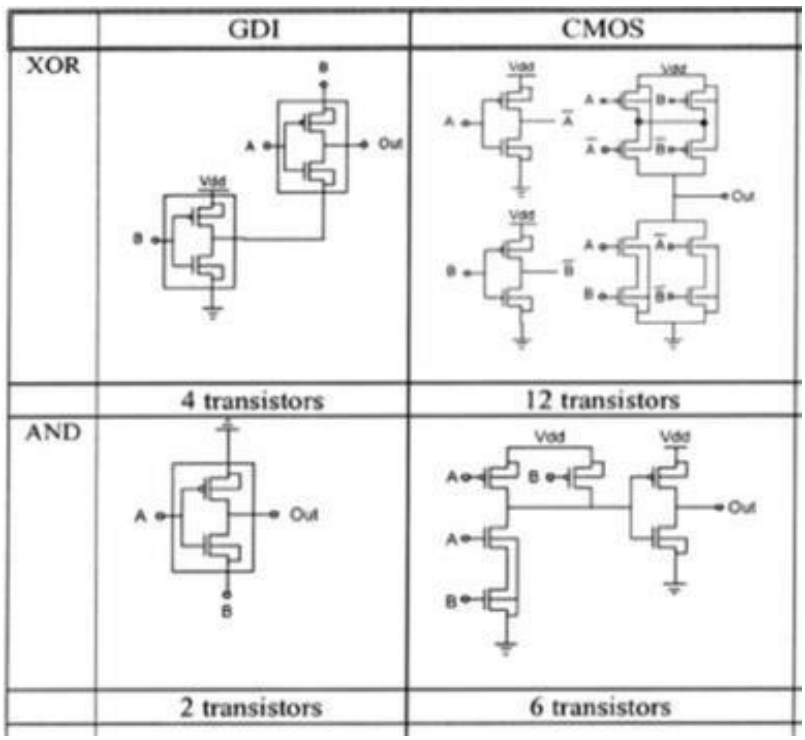


Fig 2: Comparison of XOR and AND Gates using GDI and CMOS logic

Half Adder using GDI logic:

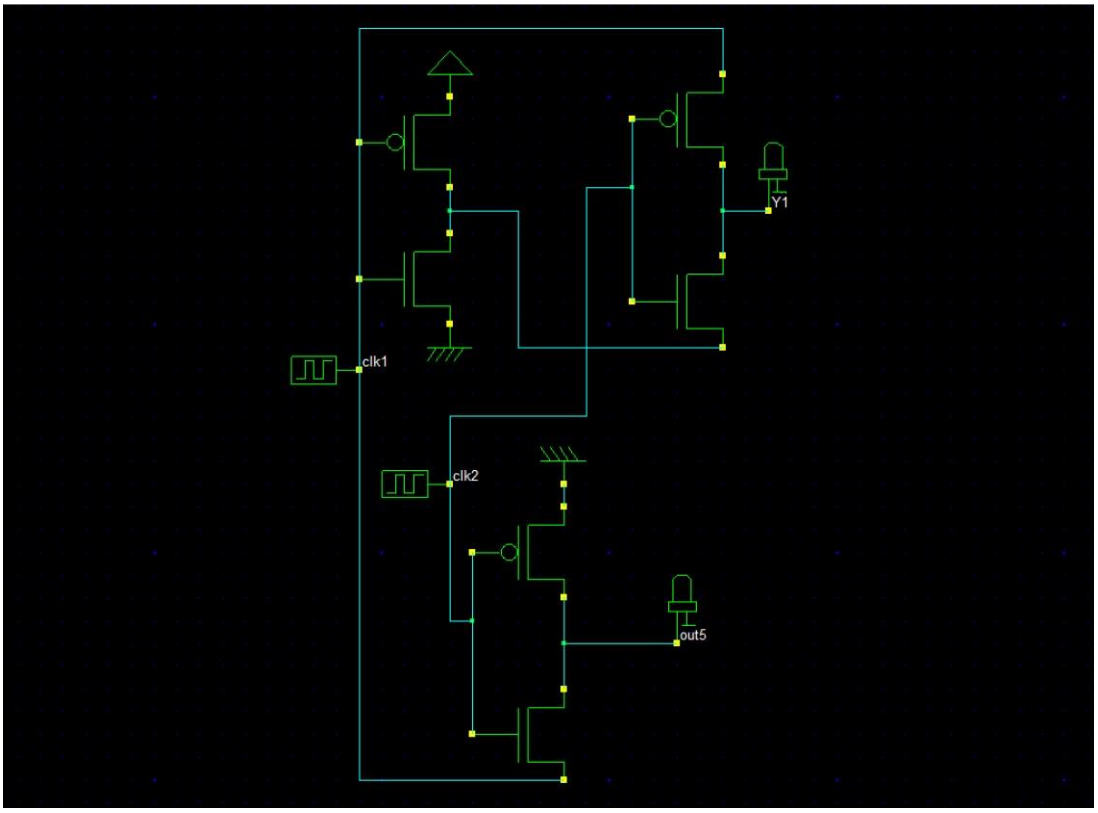


Fig 3: Schematic design of Half Adder on DSCH using GDI on DSCH

Half Adder using CMOS logic:

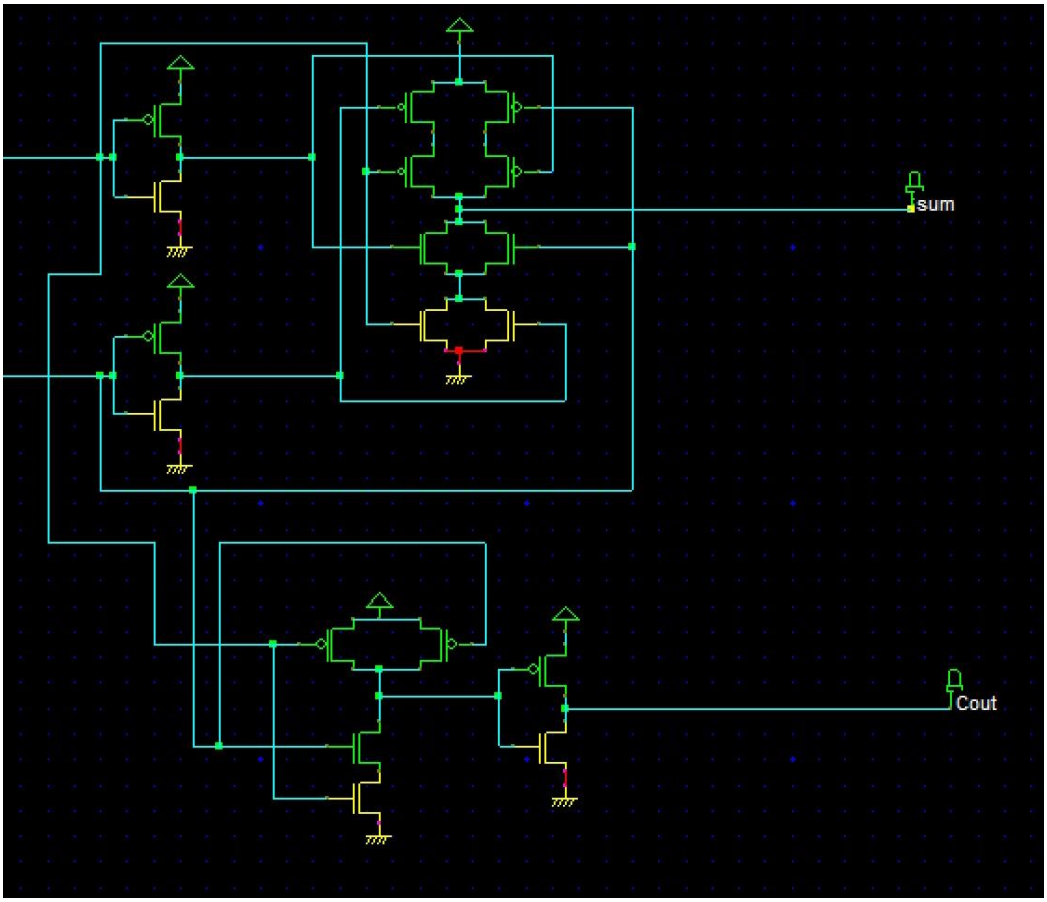


Fig 4: Schematic design of Half Adder on DSCH using traditional CMOS design

VEDIC MULTIPLIER using Urdhva Tiryagbhyam:

It is a generic algorithm applicable to every case of multiplication. This sutra is also applicable for dividing large numbers. This sutra is one of the best-known Vedic sutras and has found many applications. [2]

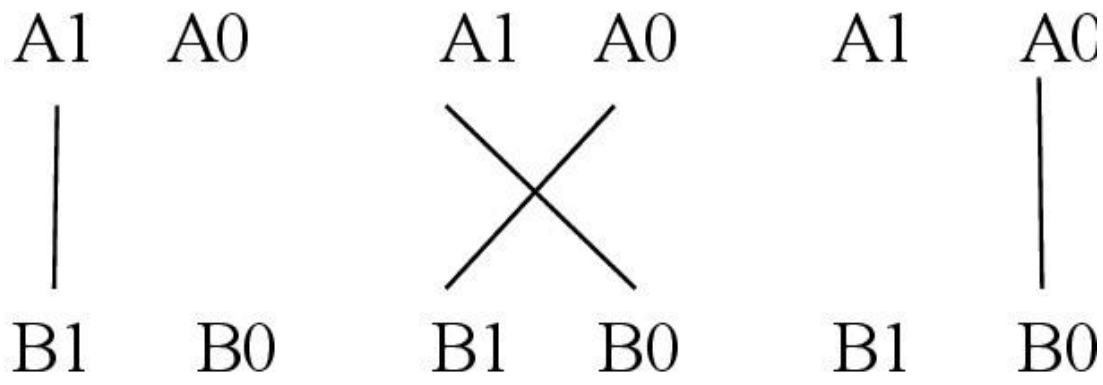


Fig 5: The Vedic Multiplier algorithm for 2 bit binary numbers

Design Implementation of 2-bit multiplier:

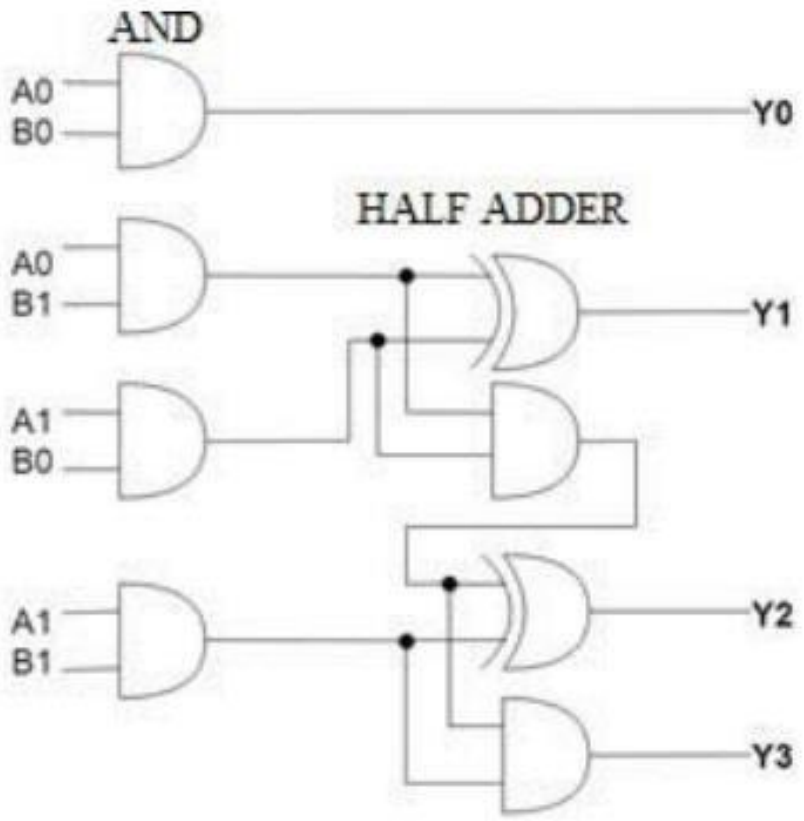


Fig 6: Design implementation using gates for 2bit Vedic Multiplier using Urdhva Tiryagbhyam

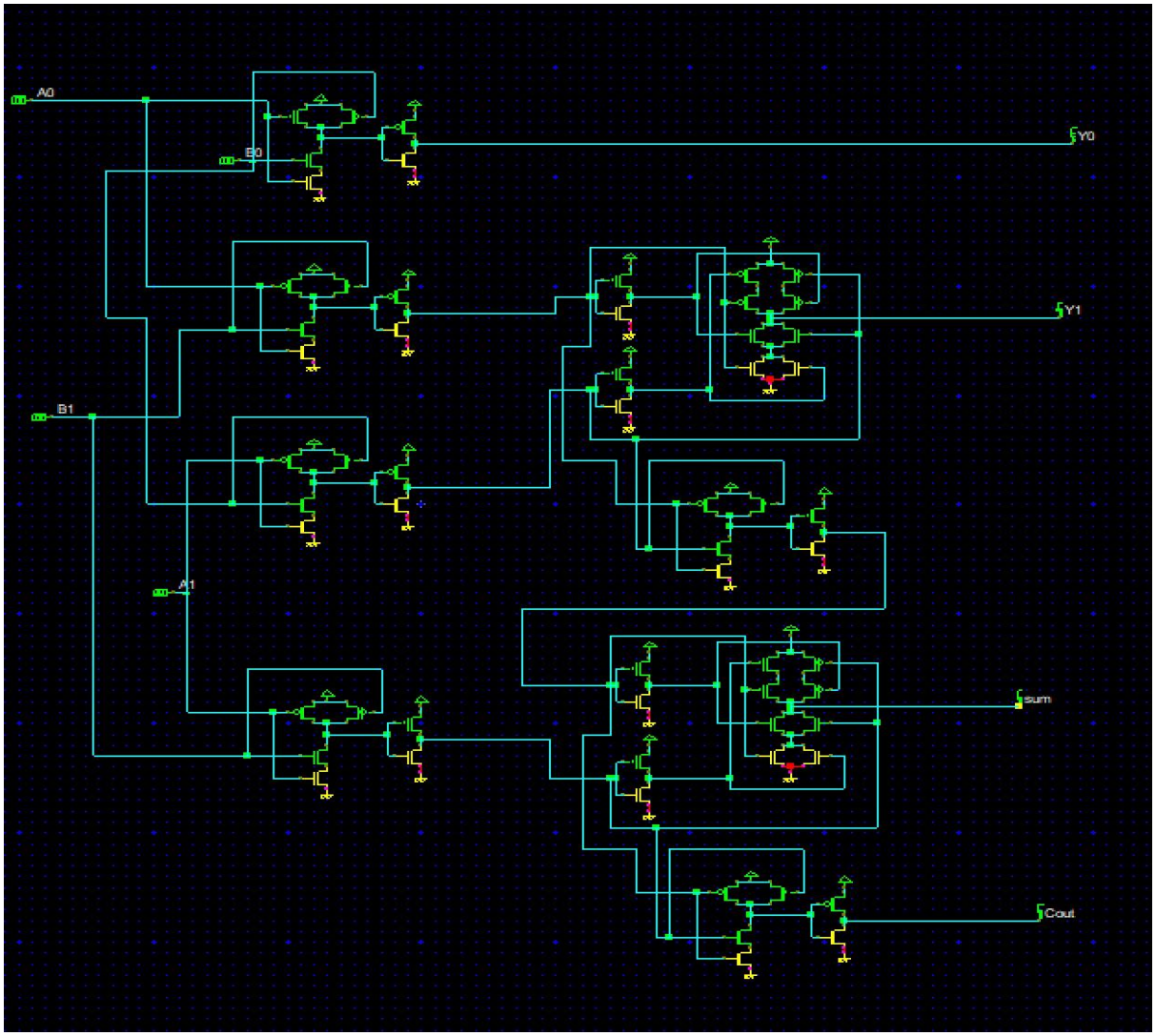
There are three steps in a 2-bit Vedic multiplier:

1) The LSB bits A0 and B0 are propagated through an AND gate to produce Y0.

2) The product A0B0 and A1B0 are summed using a half adder, whose sum output contributes to Y1. The carry out is transmitted to the next stage.

3) The product A1B1 along with the carry from the previous stage is again added using a half adder. The outputs, sum and carry give Y2 and Y3 respectively. [2]

2-bit Vedic Multiplier using CMOS logic:



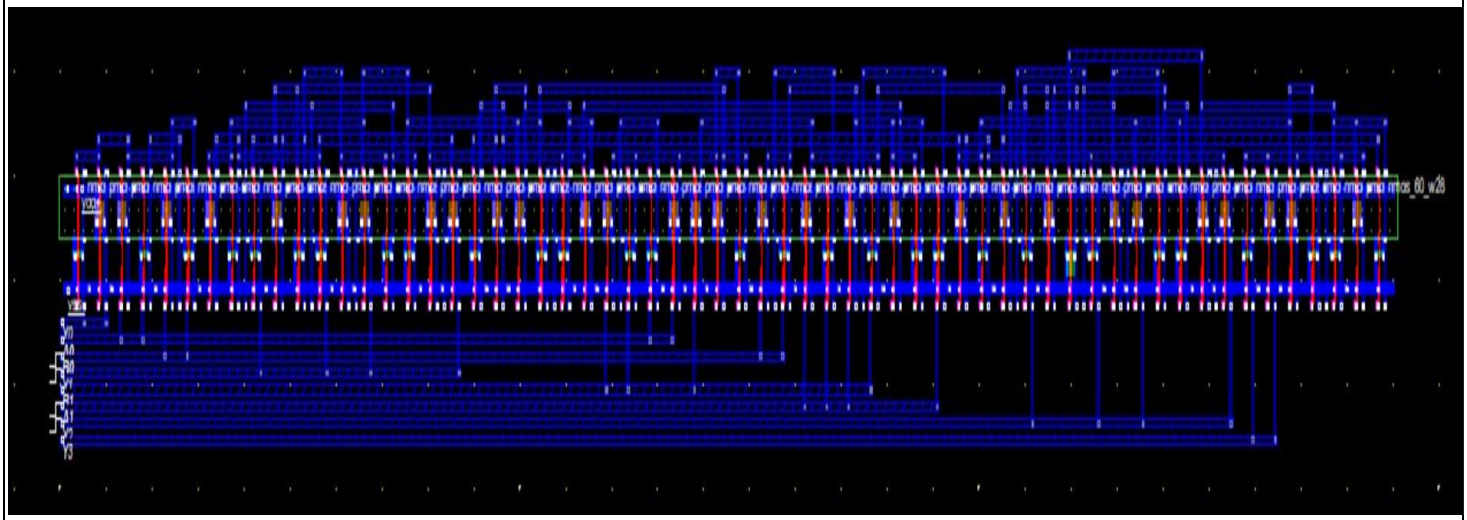


Fig 7: (a) DSCH layout (b) MICROWIND layout of 2-bit Vedic Multiplier using traditional CMOS

2-bit Vedic Multiplier using GDI logic:

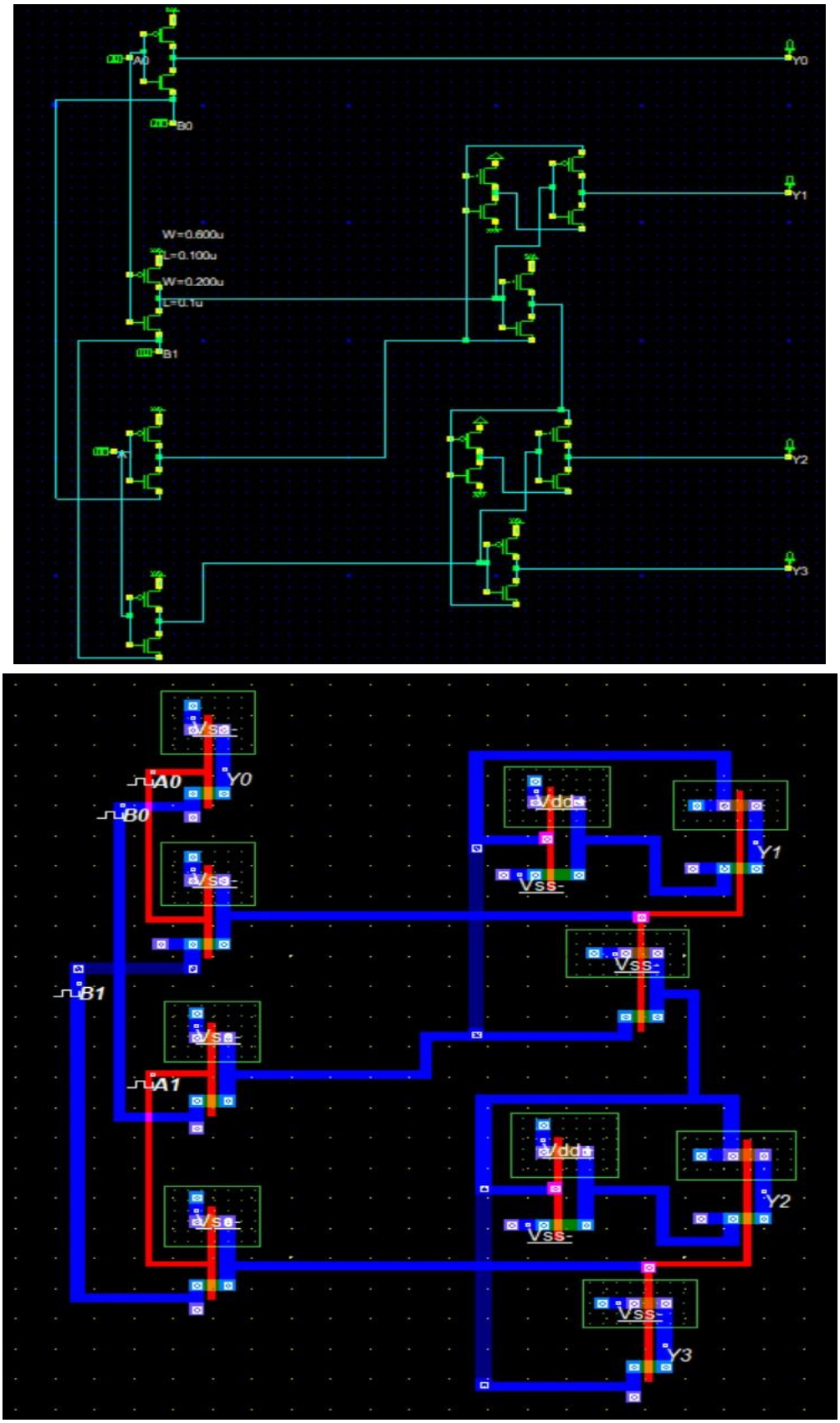


Fig 8: (a) DSCH layout (b) MICROWIND layout of 2 bit vedic multiplier using GDI logic

2-bit Vedic Multiplier using MGDI logic:

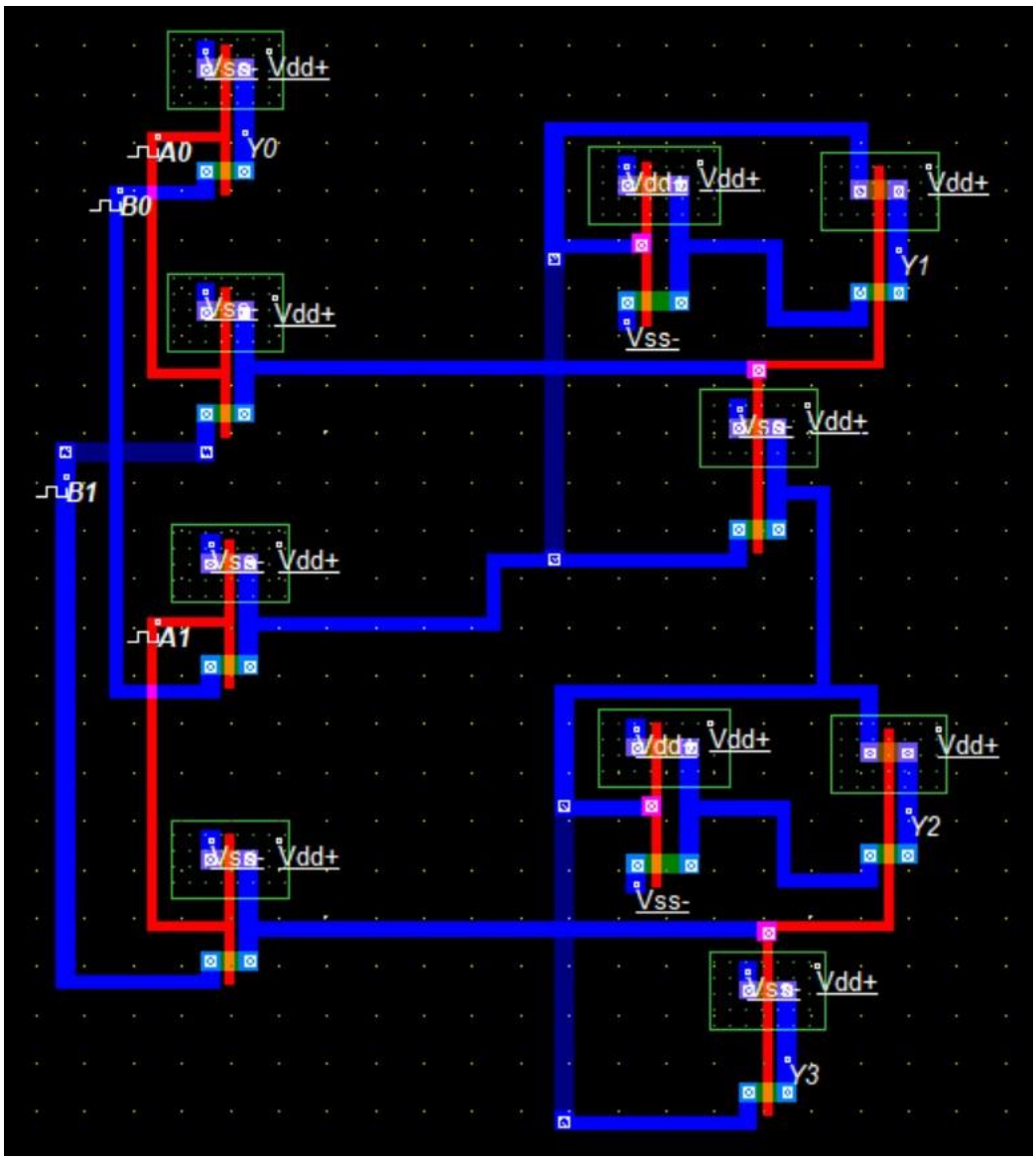


Fig 9: MICROWIND layout of 2-bit Vedic Multiplier using MGDI logic

DSCH Outputs:

CMOS LOGIC:

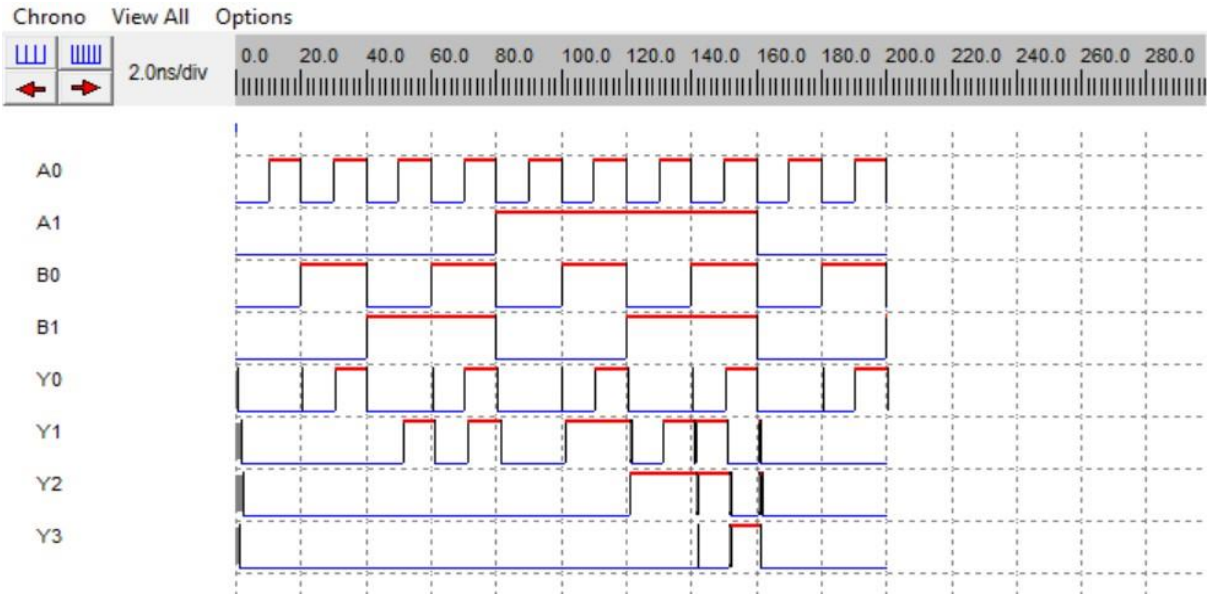


Fig 10: DSCH output waveform of 2-bit Vedic multiplier using traditional CMOS design

GDI LOGIC:

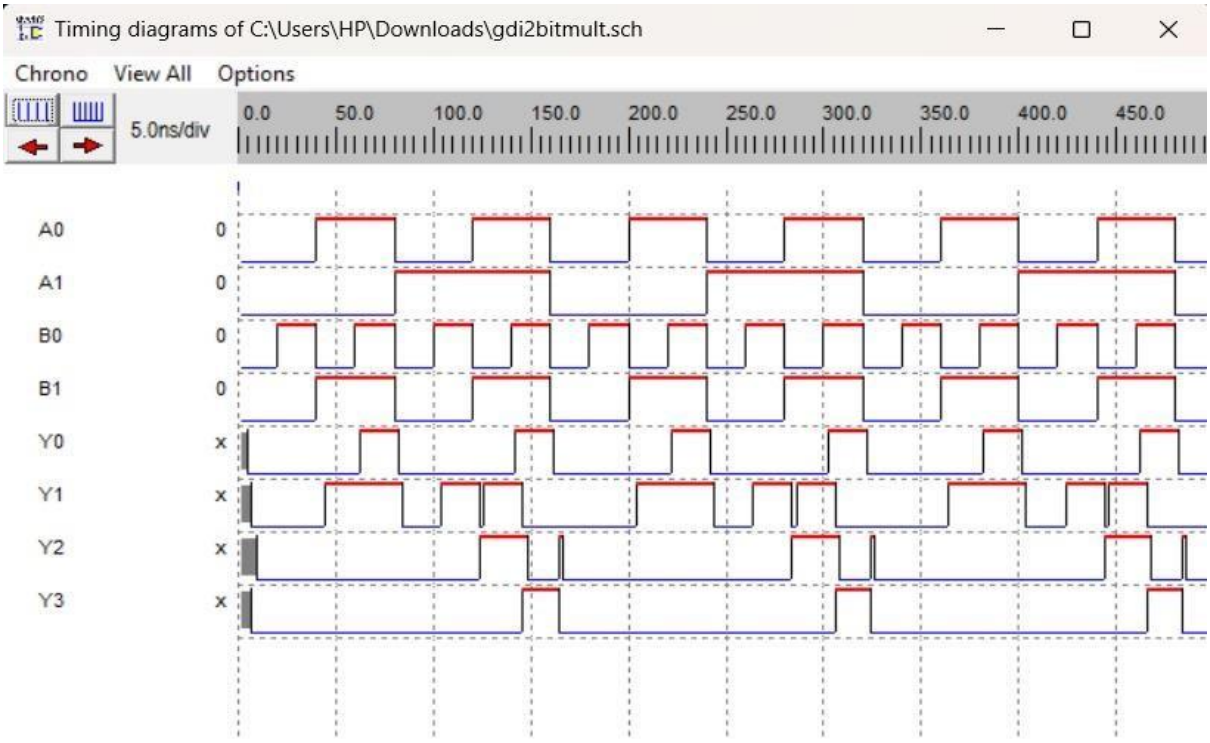


Fig 11: DSCH output waveform of 2-bit Vedic Multiplier using GDI logic

MICROWIND Outputs:

CMOS LOGIC:

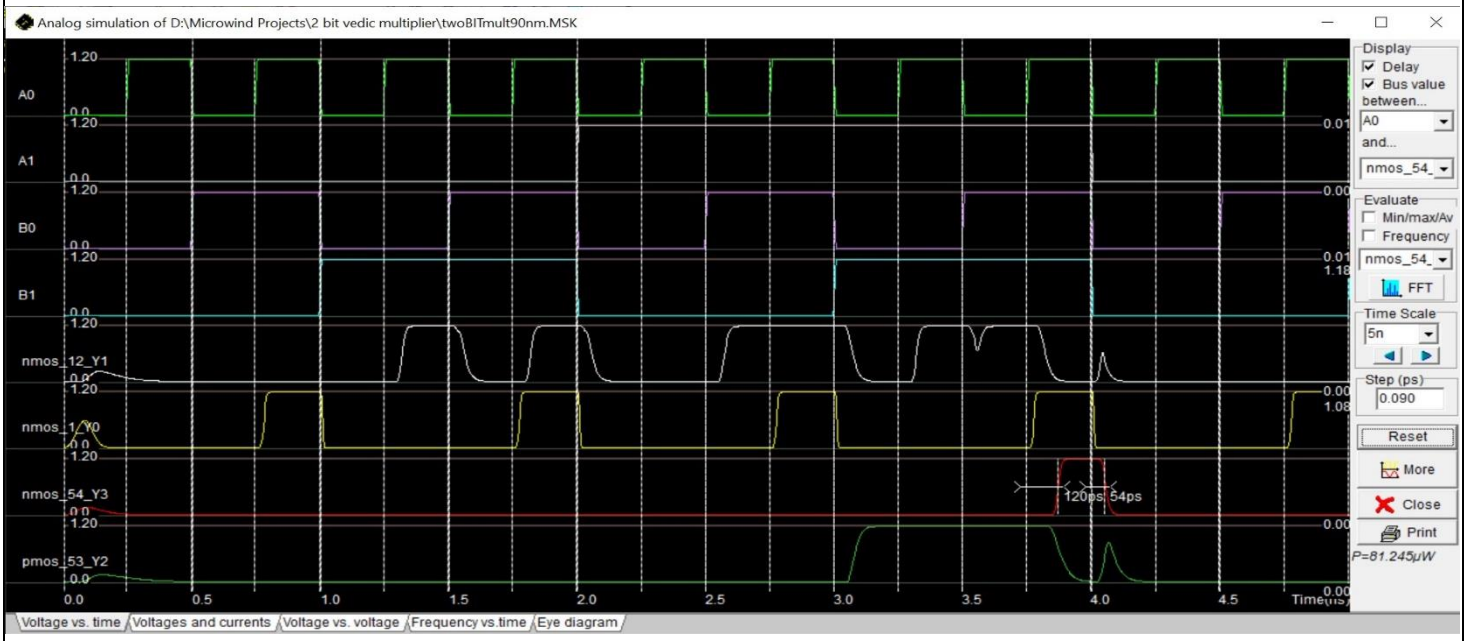


Fig 12: MICROWIND output waveform of 2-bit Vedic Multiplier using traditional CMOS design

GDI Logic:

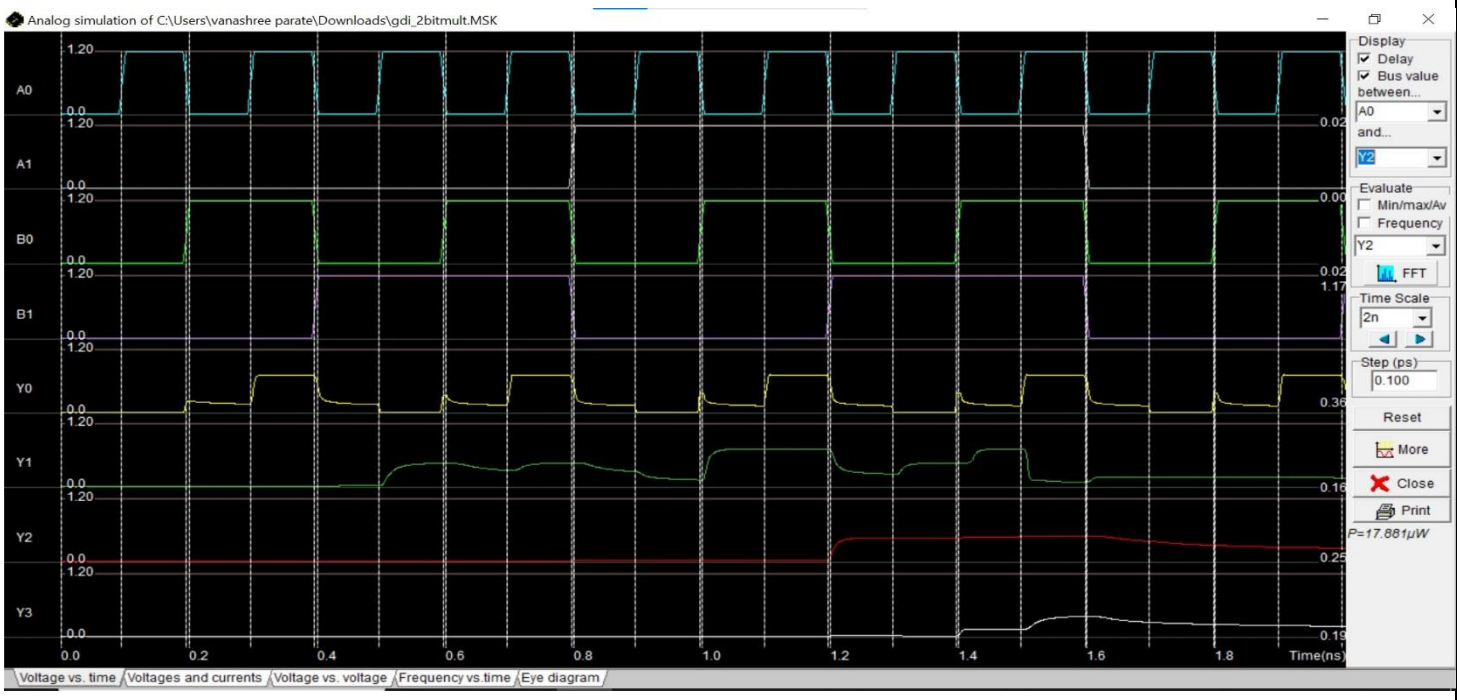


Fig 13: MICROWIND output waveform of 2-bit Vedic Multiplier using GDI logic

MGDI Logic :

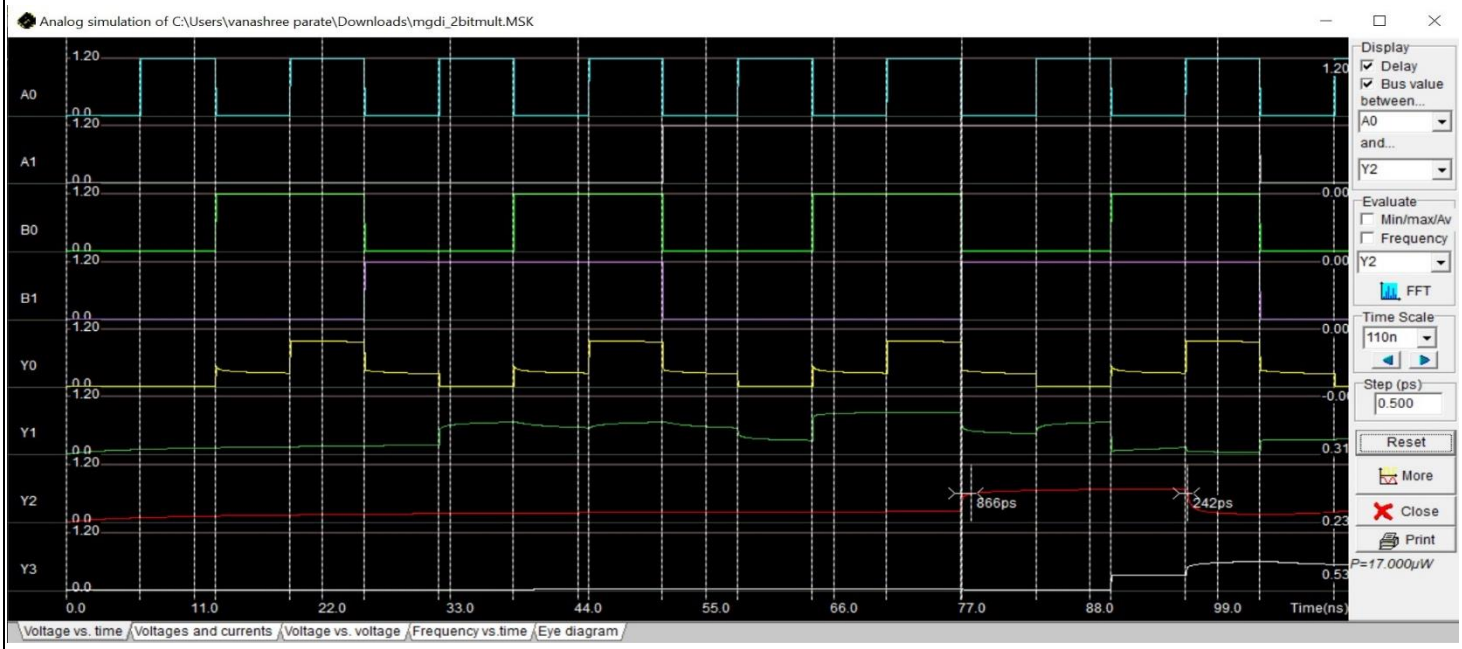


Fig 14: MICROWIND output waveform of 2-bit Vedic Multiplier using MGDI logic

COMPARISIONS:

POWER COMPARISION:

CMOS	GDI LOGIC	MGDI LOGIC
81.245uW	17.881uW	17uW

NUMBER OF TRANSISTORS:

	CMOS	GDI/MGDI
AND Gate	6	2
Half Adder	18	6
Total (4 AND + 2 HA)	60	20

AREA ESTIMATION:

	CMOS	GDI	MGDI
Width	72.9µm (1458 lambda)	9.2µm (184 lambda)	9.2µm (184 lambda)
Height	9.4µm (188 lambda)	11.8µm (236 lambda)	11.4µm (227 lambda)
Surface	685.3µm2 (0.0 mm2)	108.6µm2 (0.0 mm2)	104.4µm2 (0.0 mm2)

Conclusion:

In summary, the comparative analysis of 2-bit multipliers using traditional CMOS, Gate Diffusion Input (GDI) CMOS layouts and Modified Gate Diffusion Input (MGDI) layouts, conducted with DSCH and MICROWIND software, highlights the trade-offs between complexity, efficiency, and performance. While traditional CMOS layouts offer reliability at the expense of higher transistor counts and area overheads, GDI and MGDI layouts show potential for improved efficiency through reduced transistor counts and simplified gate structures.

The disadvantage of the GDI technique is that it is not possible to obtain a strong 0 and strong 1 at the output under certain combinations of inputs. This disadvantage is reduced by using MGDI technique. MGDI gates lower the transistor count and in turn the silicon area required when compared to standard static CMOS and Domino CMOS based approaches. The leakage power and switching power of MGDI gates is lower than the traditional logic styles. [3]

It is not that power dissipation is always reduced by significant amounts in MGDI. We need to analyse all factors and consider all trade-offs in selecting the most appropriate layout for specific application requirements. There are more logics, like, Bi CMOS logic, adiabatic logic, etc., which may be a good fit for the design.

References:

[1] P. Manju et al., “Design of Vedic Multiplier using GDI Method,” International Journal of Recent Technology and Engineering (IJRTE), 2019.

[2] Chiranjit R Patel et al., “Vedic Multiplier in 45nm Technology”, IEEE Xplore,2020.

[3] E. Pavani, Dr. V. Ashok Kumar, A. Jaya Lakshmi, “Performance Evaluation of Gate Diffusion Input and Modified Gate Diffusion Input Techniques for Multipliers and Fast Adders design”, International Research Journal of Engineering and Technology (IRJET), 2019.

[4] Divya Soni, Mihir V. Shah, “Review on Modified Gate Diffusion Input Technique”, International Research Journal of Engineering and Technology (IRJET), 2017.

[5] Nitin Singh, M. Zahid Alam, “Design and Implementation of 8 Bit Multiplier Using M.G.D.I. Technique”, International Journal Of Modern Engineering Research (IJMER), 2014.