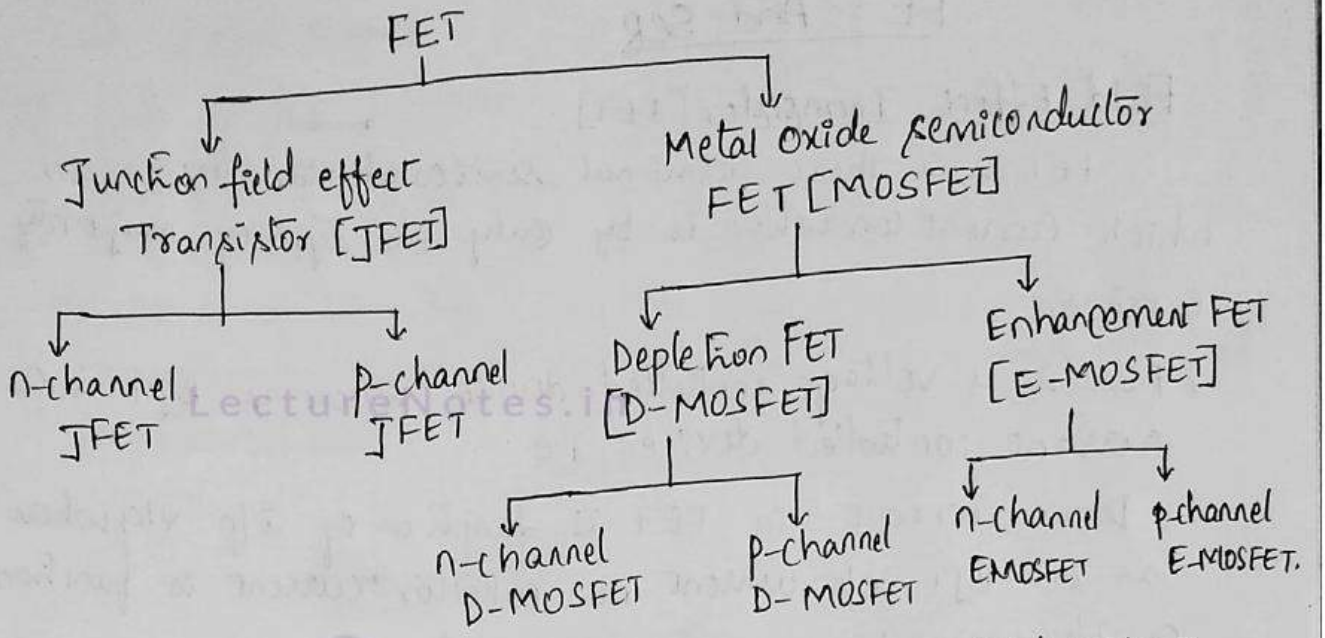
Classification:



MOSFET is also called Insulated gate field effect transistor [IGFETs].

Comparision b/w FET & BJT

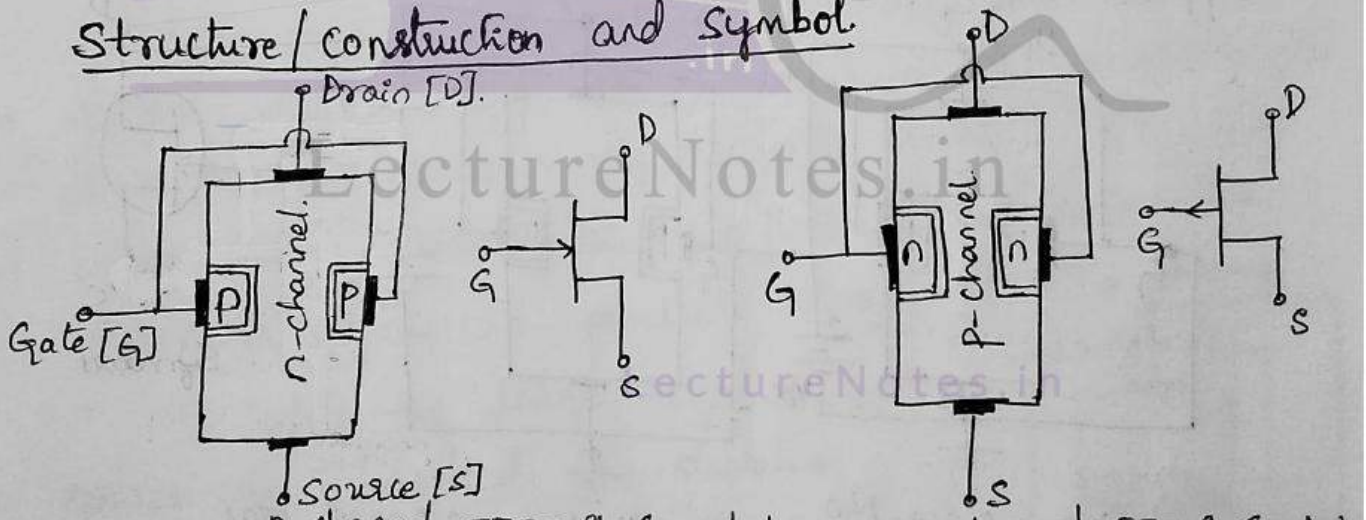
FET	BJT
1). It is a unipolar device	1) It is a bipolar device.
2) It is a v/g controlled device. i/p v/g controls the o/p current.	2) It is a current controlled device. o/p current is controlled by i/p current.
3) It exhibits high i/p resistance typically many mega ohms	3) It exhibits low i/p input resistance typically a few kilo ohms.
4) It is less noisy due to carriers crossing single junction	4) It is too noisy due to carriers crossing two junction.
5) It is immune to radiation	5) It is prone to radiation
6) Smaller in size	6) Large in size
7) Thermal stability is high	7) Thermal stability is high.

8) Less sensitive to changes in input signal	8) Highly sensitive to changes in i/p signal.
9) Gain is less in JFET amplifiers. Hence gain B.W product is less	9) Gain is large in BJT amplifiers. Hence gain Bandwidth product is large.
10) It is of two types namely n-channel & p-channel FETs.	10) BJT is also of two types npn transistor and pnp transistors.

The JFET

The JFET [junction field effect transistor] is a type of FET that operates with a reverse biased pn junction to control current in a channel. Depending on the structure JFETs are classified into n-channel and p-channel JFET.

Structure / construction and symbol



n-channel JFET: The structure and the symbol of n-channel JFET is as shown in fig above. The major part of the structure is the n-type material which forms the channel blw the embedded layers of p-type material. It has four ohmic contacts. The wire leads are connected

to each end of the n-channel. The Drain is the upper end and the source is at the lower end. The two p-type regions are diffused into n-type material to form a n-channel. The p-type regions are connected as gate terminal. In the absence of any applied potential the JFET has two p-n junctions under no-bias conditions.

P-channel JFET: In this the major part is p-type material. The two n-type material is diffused into the p-type material to form a p-channel. The two n-type material are connected together to form a gate terminal. The structure and the symbol is as shown in fig.

Operation of n-channel JFET

Let us consider n-channel JFET biased with V_{DS} [Vlg appked blw drain & source] and V_{GS} [Vlg appked blw gate & source.

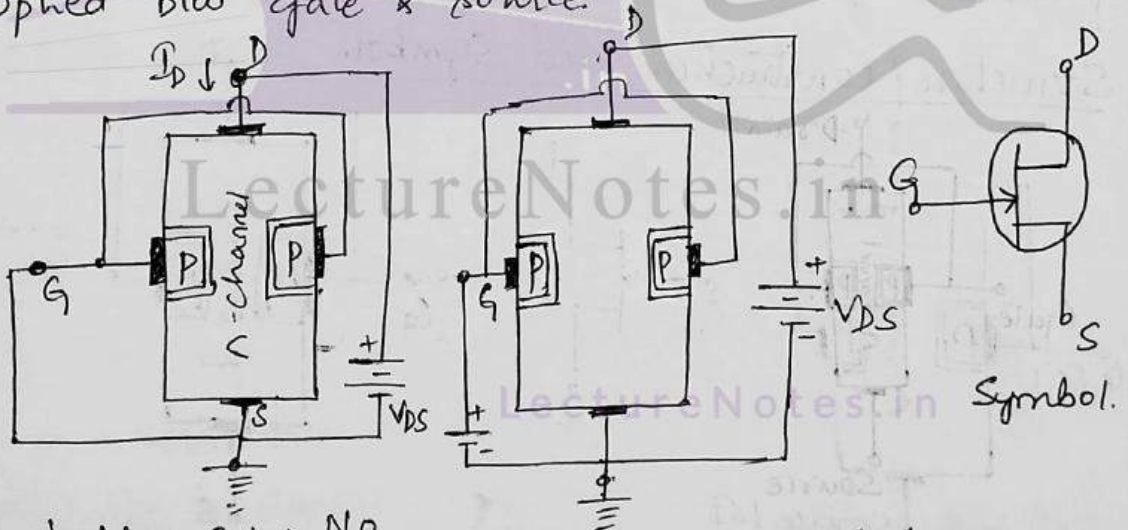


fig: a) $V_{GS}=0$ i.e No bias Vlg is appked at gate

b) V_{GS} = a small bias Vlg is appked at gate.

Case i) when $V_{GS}=0$ and V_{DS} = +ve potential.

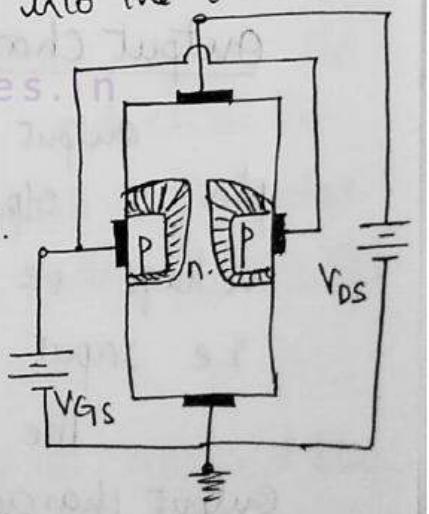
When positive Vlg is appked at the drain, & connecting gate terminal to ground i.e $V_{GS}=0$

i.e the p-n junction blw gate and source is constantly kept in reverse biased conditions. Since the pn junction is reverse biased there will be very small amount of current of eventually it is zero. i.e $I_G = 0$. Because of the V_{DS} applied blw the drain & source, which attaracts the electrons from the n-material which leads to flow of current from Drain to source as shown in figure.

Case② when $V_{GS} < 0$ and $V_{DS} > 0$.

Due to connected vlg, the majority carriers i.e electrons begin to flow from source to drain reducing the depletion region and increases the channel width this stream of electrons makes the drain current. I_D.

Since gate is heavily doped and the channel is lightly doped, the width of the depletion region will spread in the channel. Since n-material is resistive, the drain current causes a vlg across the channel. this vlg drop reverse biases the p-n junction and causes the depletion regions to penetrate slowly into the channel.



when the large negative gate source vlg is applied the depletion region penetrates more into the n-channel. The depletion region width is more at drain side compared to source side as shown in figure. as we go on increasing negative vlg across gate source the depletion regions almost touch each other

which makes drain current to reduce.

Construction and Working of p-channel JFET

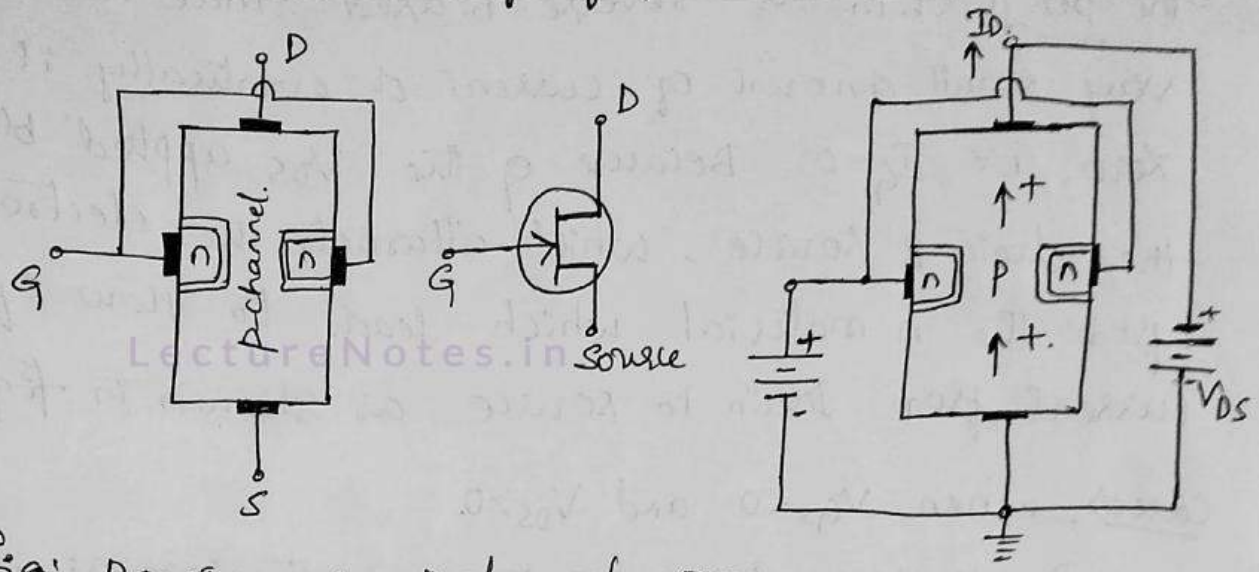


fig: Biasing of p-channel JFET.

The p-channel JFET is constructed similar to the n-channel JFET but with reversal of p and n-type material as shown in figure above. Here all the current and voltage applied will be reversed.

Channel width is maximum for $V_{GS}=0$. The channel width is reduced by increasing positive gate to source voltage. V_{GS} is +ve for p-channel and V_{DS} is negative.

Output Characteristics / Drain Characteristics

Output or Drain characteristics of JFET is a plot of o/p current i.e Drain current versus output voltage i.e Drain to source vlg. Keeping V_{GS} constant i.e input vlg constant.

The experimental setup for measuring the output characteristics are as shown below.

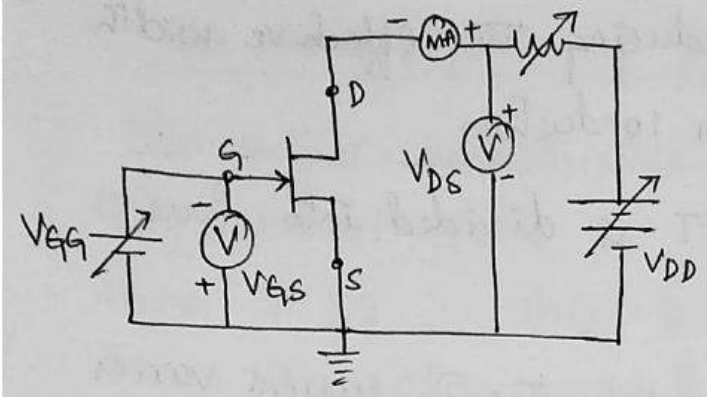
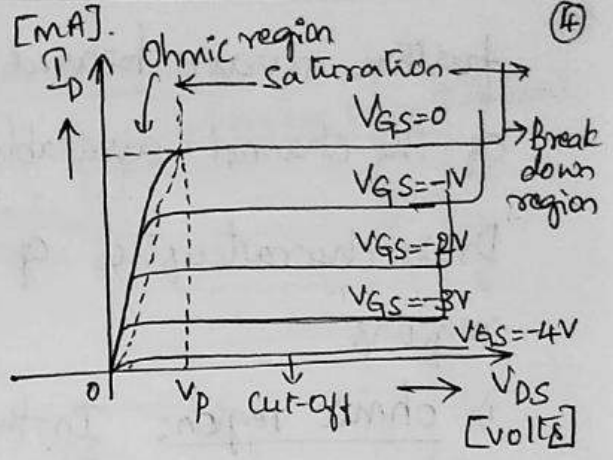


fig: Experimental setup to plot JFET characteristics



Drain characteristics.

i) when $V_{GS} = V_{DS} = 0$. The channel is entirely open. As $V_{DS}=0$ there is no attaractive force for the majority carriers and hence drain current does not flow.

ii) when $V_{GS}=0$ and when a small amount of V_{DS} is applied. The drain current starts to flow. As we increase V_{DS} towards the +ve voltage. it increases the reverse bias on gate source junction and causes depletion region to penetrate into the channel reducing the channel width making the Drain current to be constant.

At some value of V_{DS}, the drain current I_D cannot be increased further due to reduction in channel width. The voltage at which I_D reaches to its constant saturation level is called "pinch off" voltage (V_p).

when the external bias of -1V is applied blw the gate and source. the gate channels junctions

further reverse biased. reducing the effective width of the channel available for conduction.

Drain characteristics of JFET is divided into four regions.

1) **ohmic region:** In this region, the I_D current varies linearly with V_{DS} satisfying the ohm's law hence the name ohmic region.

2) **Saturation region:** This is the region, in which I_D current remains constant and does not vary with V_{DS}.

3) **cutoff:** when V_{GS} made sufficiently negative, I_D is reduced to zero. This is caused by widening of depletion region to point where it completely closes the channel. V_{GS} at cut-off is called $V_{GS(off)}$

4) **Breakdown Region:** If V_{DS} is keep on increasing, the voltage will be reached at which gate channel junction breaks down due to avalanche effect. At this point the drain current increases very rapidly and device may be destroyed.

I_{DSS} is the maximum drain current when $V_{GS} = 0$. It is the saturated current blw the drain & source.

Drain characteristics of p-channel JFET:

The output characteristics of p-channel JFET is as shown in fig. In this the source is positive w.r.t to the drain. It is similar to the n-channel JFET except the voltages V_{GS} and V_{DS} have reversed polarities and current I_D flows in reverse direction.

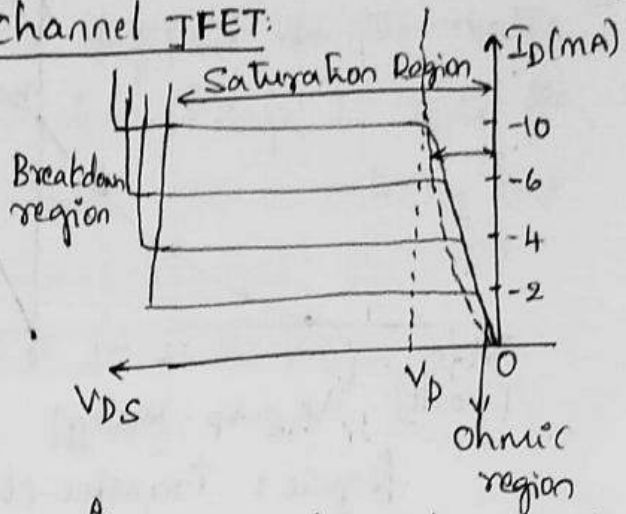


fig: Drain characteristics & VI characteristics of p-channel JFET.

Transfer characteristics of JFET

It is a plot of output current i.e I_D [Drain current] to input voltage i.e V_{GS} [Gate to source v/g] keeping V_{DS} constant.

The relationship b/w I_D & V_{GS} is non-linear. This characteristic is defined by the equation

$$I_D = I_{DSS}\left[1 - \left(\frac{V_{GS}}{V_p}\right)\right]^2$$

where $I_D \rightarrow$ Drain current $\quad V_p \rightarrow$ Constant

$I_{DSS} \rightarrow$ constant $\quad V_{GS} \rightarrow$ control variable.

As V_{GS} decreases I_D increases exponentially. The transfer characteristics of JFET is drawn using,
i) Equation ii) o/p of Drain characteristics.

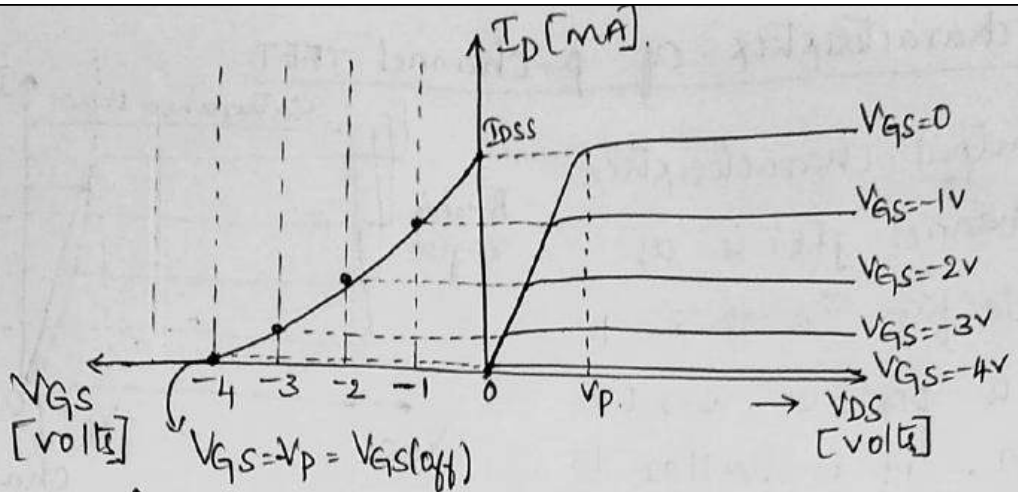


figure: Transfer characteristics of JFET using Drain characteristics.

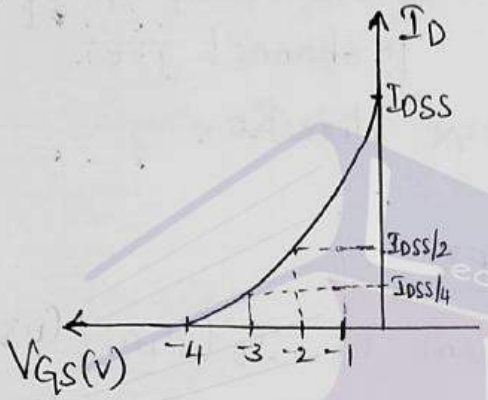


fig: Transfer characteristics of n-channel JFET

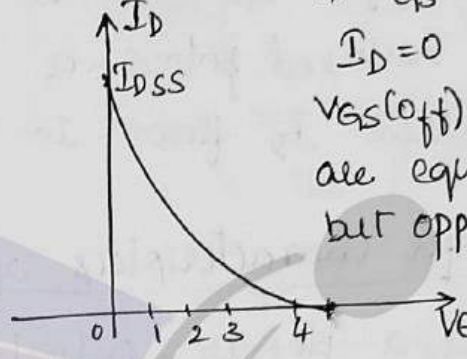


fig: Transfer characteristics of p-channel JFET.

* V_{GS} at which $I_D=0$ is called $V_{GS(off)}$. V_p & $V_{GS(off)}$ are equal in magnitude but opposite in sign.

The above figures shows the Transfer characteristic of n-channel JFET and p-channel JFET. p-channel JFET is similar to the n-channel JFET the only change is that the polarities of V_{GS} and I_D are reversed.

Characteristic parameters of JFET

1) Transconductance (g_m)
2) Input resistance
3) Drain to source resistance (r_d)
4) Amplification factor (μ)
5) power dissipation.

1) Transconductance: (g_m) : It is defined as the ratio of change in drain current for change in gate to source v/g with V_{DS} = constant. It is nothing but the slope of the transfer characteristics of JFET. g_m is also called as mutual conductance. The unit is mS (millisiemen) & mA/V.

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}=\text{constant}}$$

g_{mo}: It is transconductance measured at $V_{GS} = 0$. It is normally given in the data sheet. The approximate value of g_m at any point on the transfer characteristics is calculated using,

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]$$

When g_{mo} is not given in the data sheet:

$$g_{mo} = \frac{2\,I_{DSS}}{|V_{GS(off)}|}$$

2) Input Resistance : JFET operates with its gate-source junction reverse biased, which makes the input resistance at the gate very high. The input resistance can be determined by. $R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$

I_{GSS} will be given in datasheet. I_{GSS} is gate reverse current. The gate reverse current increases with temperature

thus decreases the i/p resistance.

3) AC drain to Source resistance (r_d)

The drain resistance r_d is the ac resistance b/w drain and source terminals when JFET is operating in saturation region. r_d is given by,

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS} = \text{constant}}$$

Above pinch off, the drain current is relatively constant over a range of drain to source v/g. Large change in V_{DS} produces very small change in I_D. Since characteristic is flat in saturation region, r_d is not easily determined. It may also be expressed as an output admittance. The admittance is given by the expression.

$$Y_{os} = \frac{1}{r_d}$$

4) Amplification factor: (μ)

The amplification factor is defined as rate of change of drain to source v/g to rate of change of gate to source v/g keeping drain current constant. The expression for amplification factor is given by,

$$\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D \text{ is constant.}}$$

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \cdot \frac{\Delta I_D}{\Delta V_{GS}} = r_d \cdot g_m.$$

5) Power Dissipation: (P_D)

Power dissipation can be defined as product of drain current and drain to source v/g. The expression for power dissipation can be given by,

$$P_D = I_D \cdot V_{DS}$$

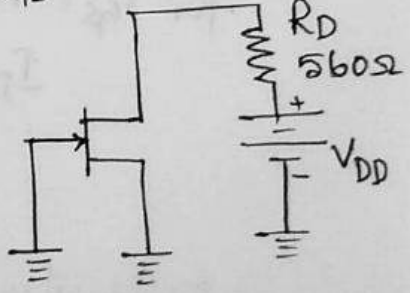
JFET Transfer characteristic is expressed by,

$$I_D \cong I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

The above equation is also called as 'Square Law' or Drain current equation for JFET. I_D can be determined for any V_{GS}, if $V_{GS(off)}$ and I_{DSS} is known. I_D is function of square of appled i/p voltage V_{GS} Hence the name "Square law"

problems:

1) For the JFET shown in fig: $V_{GS(off)} = -4V$ and $I_{DSS} = 12mA$. Determine the minimum value of V_{DD} required to put the device in the constant current region of operation when $V_{GS} = 0V$



Soln: Given $R_D = 560\Omega$, $V_{GS(off)} = -4V$

$\therefore V_p = 4V$, $I_{DSS} = 12mA$.

.... The minimum value of V_{DS} for the JFET to be in constant current region is $V_{DS} = V_p = 4V$

In the constant-current region with $V_{GS} = 0V$

$$I_D = I_{DSS} = 12\,mA.$$

The drop across R_D is

$$V_{RD} = I_D \times R_D = (12mA)(560\Omega)$$

$$\boxed{V_{RD} = 6.72V}$$

Applying Kirchhoff's law around the drain ckt

$$V_{DD} = V_{DS} + V_{RD}$$

$$= 4 + 6.72$$

$$\boxed{V_{DD} = 10.72V}$$

This is the V_{DD} at V_{DD} to make $V_{DS} = V_p$ and put the device in the constant current region.

2) For a 2N5459 JFET, it is given $I_{DSS} = 9mA$ and $V_{GS(off)} = -8V$ (maximum). Using these values. determine the drain current for $V_{GS} = 0V$, $-1V$ and $-4V$.

Soln: $V_{GS} = 0V$,

$$I_D = I_{DSS} = 9mA.$$

for $V_{GS} = -1V$,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$= (9mA)\left(1 - \frac{-1V}{-8V}\right)^2$$

$$= 9 \times 10^{-3}\,(1 - 0.125)^2$$

$$\boxed{I_D = 6.89\,mA}$$

for $V_{GS} = -4V$

$$I_D = (9mA)\left(1 - \frac{-4V}{-8V}\right)^2$$

$$= 9\times10^{-3}(1-0.5)^2 = 9\times10^{-3}\times0.25$$

$$\boxed{I_D = 2.25\ mA}$$

3) The following information is included in the datasheet of 2N5457 JFET. typically, $I_{DSS} = 3.0mA$, $V_{GS(off)} = -6V$ maximum and $g_{mo} = 5000\mu s$. Using these values determine the forward transconductance for $V_{GS} = -4V$ and I_D at this point.

Soln: $g_{mo} = 5000\mu s$, $I_{DSS} = 3\times10^{-3}A$, $V_{GS(off)} = -6V$

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]$$

$$= 5000\left[1 - \frac{-4V}{-6V}\right]$$

$$\boxed{g_m = 1667\mu S}$$

$$I_D \cong I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$= 3\times10^{-3}\left[1 - \frac{-4}{-6}\right]^2$$

$$\boxed{I_D = 333\mu A}$$

4) A Given JFET has following characteristics: $I_{DSS} = 12mA$, $V_{GS(off)} = -5V$ and $g_{mo} = 3000\mu S$ Find

g_m and I_D when $V_{GS} = -2V$.

Soln: Given: $I_{DSS} = 12mA$, $V_{GS(off)} = -5V$ and $g_{m0} = 3000\mu S$

$V_{GS} = -2V$.

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]$$

$$= 3000 \times 10^{-6}\left[1 - \frac{-2V}{-5V}\right]$$

$$\boxed{g_m = 1800\mu S}$$

$$I_D \cong I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$= 12 \times 10^{-3}\left[1 - \frac{-2}{-5}\right]^2$$

$$\boxed{I_D = 4320\mu A}$$

4) A Certain JFET has an I_{GSS} of $-2nA$ for $V_{GS} = -20V$. Determine the input resistance

Soln: given: $I_{GSS} = -2nA$

$V_{GS} = -20V$

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

$$= \frac{20V}{2nA}$$

$$\boxed{R_{IN} = 10,000M\Omega}$$

METAL OXIDE SEMICONDUCTOR FET [MOSFET]

This is very small hence can be used to design high density VLSI ckts. MOSFETs has no pn junction structure. Instead the gate of MOSFET is Insulated from channel by a SiO_2 layer. Due to this I/p resistance is very high.

Because of the insulated gate, they are also called as IGFET's [Insulated Gate FET's].

They are two types.

1) Depletion (D) MOSFET
2) Enhancement (E) MOSFET.

Enhancement MOSFET (E-MOSFET)

E-MOSFET operates only in the enhancement mode and has no depletion mode. There is channel exist blw Drain and the source. we have to create & enhance a channel blw drain and the source hence the name Enhancement MOSFET.

Below figure shows the structure of E-MOSFET.

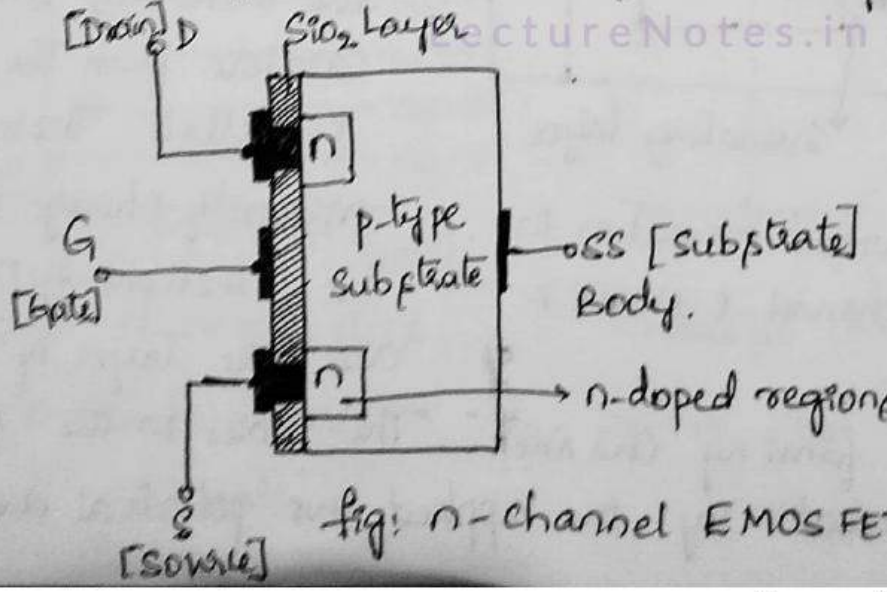


fig: n-channel EMOSFET.

Construction: Two highly doped n regions are diffused into a lightly doped p-type substrate. The source and drain are taken out through metallic contacts to n-doped regions as shown in fig.

There is no direct contact of the gate terminal with the substrate. There is a layer of SiO_2 which acts as a barrier & insulator blw gate terminal and the substrate. It has four terminals. Gate, Drain and the source along with substrate (SS) terminal & body. The substrate and the source terminal is always interconnected. There is no channel exist blw Drain and the source under no bias condition.

Operation:

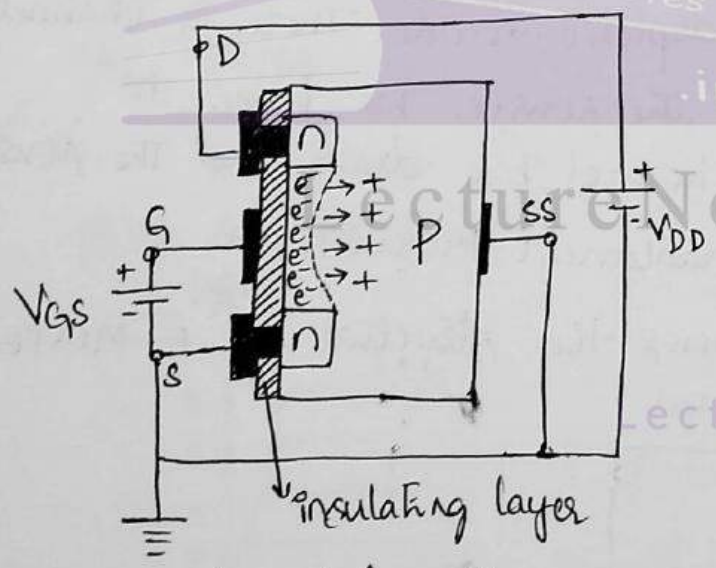


fig: Channel formation in n-channel E-MOSFET.

When a +ve vlg V_{GS} is applied blw the gate and the source terminal as shown in fig.

The +ve potential at the gate terminal attracts the minority charge carriers from the p-type substrate. These attaracted minority charge carriers i.e electrons get accumulated over the layer of p substrate thereby forming channel. The holes in the p substrate gets repelled by the applied +ve potential and will be

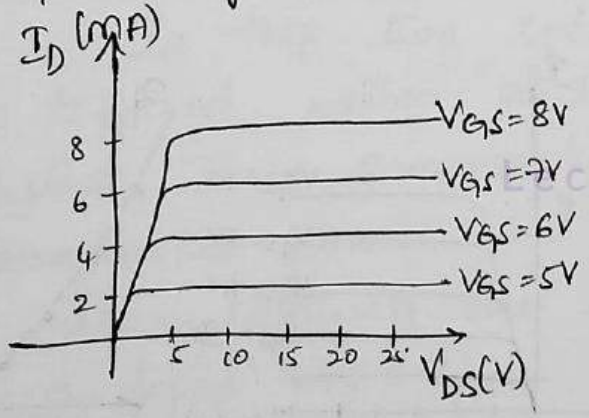
pushed down. The attaracted elections will not be able to cross the gate terminal because of the layer of SiO_2 which acts as barrier and prevents the electrons in the induced channel from being attaracted by gate terminal

The Vlg applied blw Drain and the source i.e V_{DS} attaracts the electrons which will cause the flow of I_D current through the induced channel. As V_{GS} increased more elections will be attaracted and hence increases the I_D current.

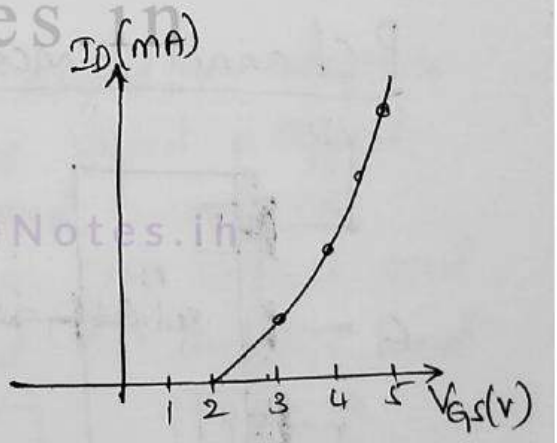
The lowest value of V_{GS} for which these exist I_D current just starts flowing is called "Threshold voltage" (V_T).

Channel does not exist with $V_{GS} = 0V$ and enhanced due to application of a +ve gate to source Vlg. Hence the name enhancement MOSFET.

The Drain characteristics and Transfer characteri-stics are given below.



Drain characteristics



Transfer characteristics.

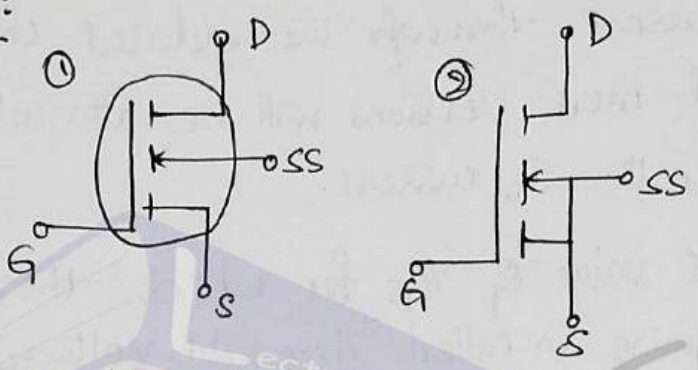
For n-channel MOSFET V_{GS} is +ve and I_D does not flow until $V_{GS} = V_T$.

For $V_{GS} > V_T$ the relationship b/w drain current and V_{GS} is non-linear and it is given by

$$I_D = K(V_{GS} - V_T)^2$$

K = Constant $\qquad K = \dfrac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$

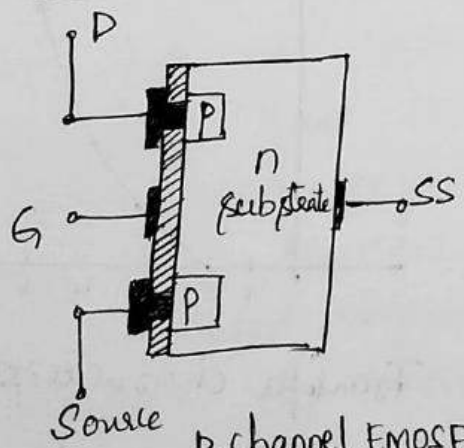
Symbol:



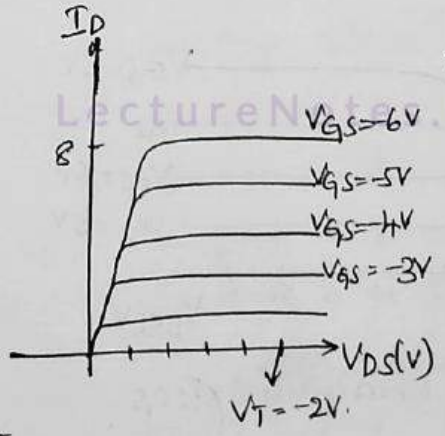
n-Channel E-MOSFET.

The dotted line indicates that there is no channel b/w Drain and the source. In some cases substrate and the sources will be interconnected which is shown in fig②

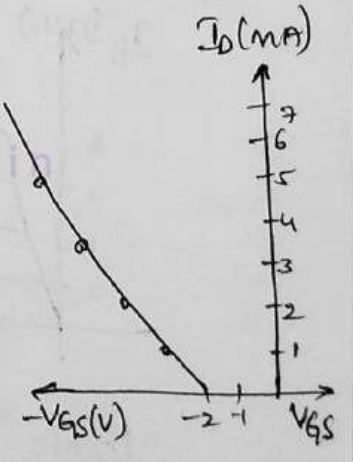
P-Channel E-MOSFET:



p-channel EMOSFET Structure

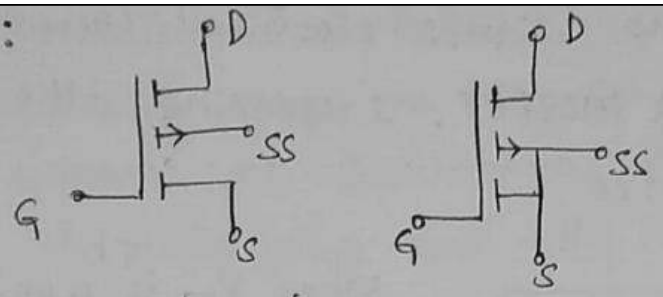


Drain Characteristics



Transfer Characteristics

Symbol:



p-channel E-MOSFET.

p channel E-MOSFET is exactly opposite to that of n-channel MOSFET. Construction, Drain characteristics, Transfer characteristics and symbol are as shown in above fig.

Note: p-channel E-MOSFET and D-MOSFET construction and operation you need to study by yourself.

Depletion MOSFET (D-MOSFET)

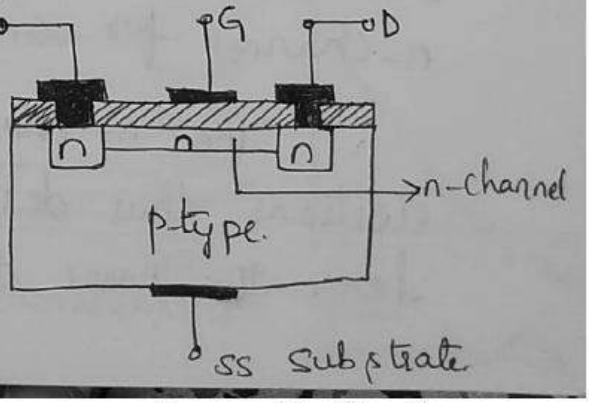
In this type of MOSFET, there exist a depletion layer or channel b/w the drain and the source under no bias condition.

n-Channel D-MOSFET:

In this two specially doped n-regions are diffused within a lightly doped p-typed substrate. These enormously doped n-regions characterises source and drain. The source and the drain terminals are linked via metallic bond to n-doped regions.

attached via n-channel.

The gate is also connected to metal surface but insulated by a very thin layer of SiO_2.



Thus there is no direct electrical connection blw gate & channel of a MOSFET, increasing the input impedance of device.

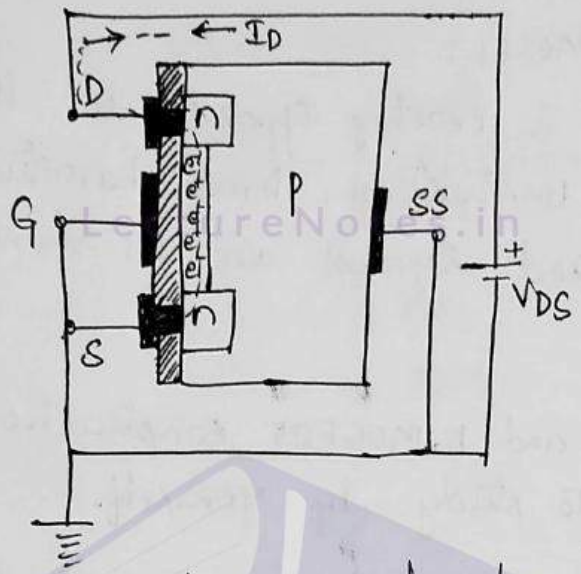


fig: Operation of n-channel D-MOSFET

When V_{DS} is applied keeping $V_{GS}=0$ by directly connecting gate to source terminal free electrons from the n-channel are attracted towards +ve potential of drain terminal.

This establishes current through the channel to be denoted as I_{DSS} at $V_{GS}=0V$.

If we apply -ve voltage across the gate and source terminal. the negative charges on the gate terminal repel and get attracted by the +ve charges in the substrate. This initiates a recombination of repelled electrons and holes from the p substrate. This recombination depends on magnitude of negative voltage applied to the gate. Hence the number of free electrons reduced due to the recombination in n-channel for conduction reducing the Drain current.

The n-channel is depleted some of its electrons thus decreasing the channel conductivity hence the name depletion MOSFET.

The greater the depletion of n-channel electrons with increasing negative bias for V_{GS}. the level of drain current will deduced as shown. in fig. The Drain characteristics and the Transfer characteristics are as shown below.

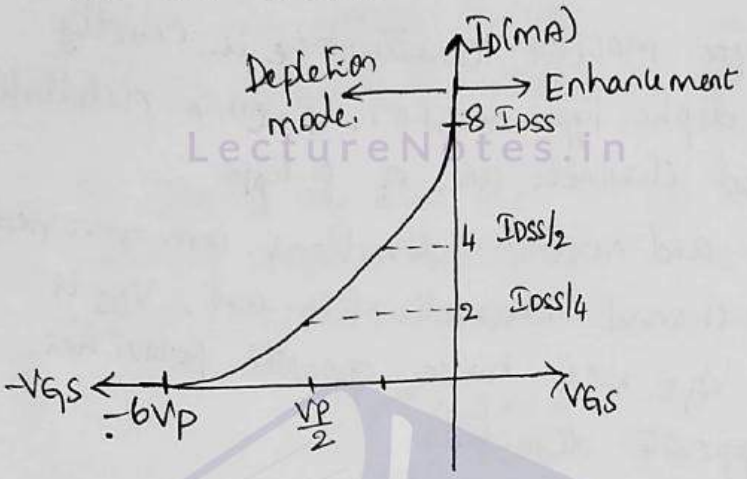


fig: Transfer characteristics

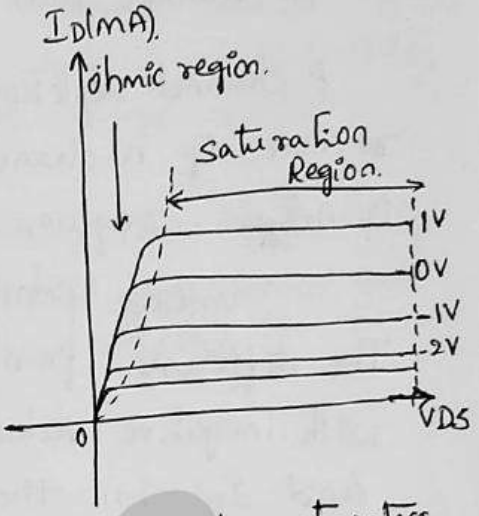
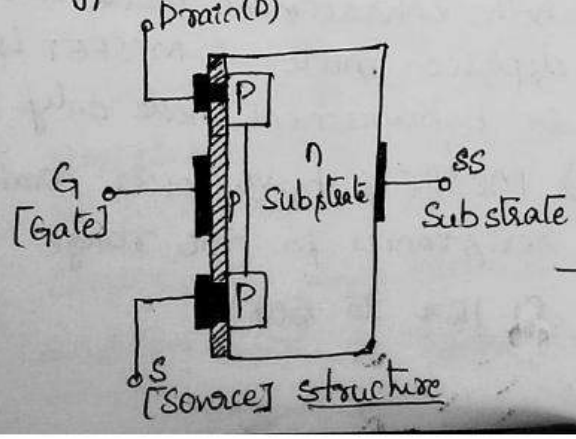


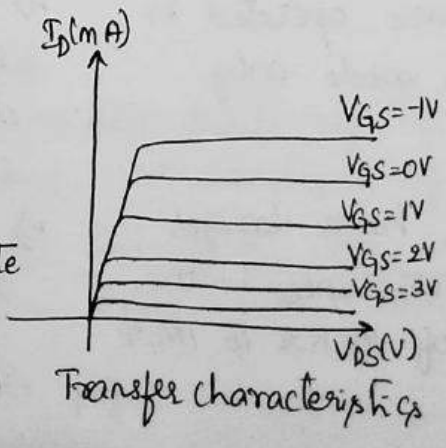
fig: Drain characteristics

If the positive voltage is applied blw the gate and source terminal, which enhances the number of electrons in the channel in contrast to that observed with $V_{GS}=0$. Hence the region of positive gate voltage on the transfer characteristics can be referred as enhancement region.

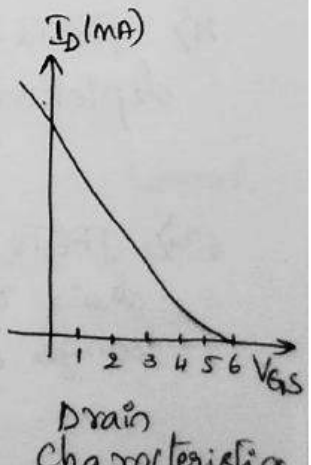
p-Channel Depletion Type D-MOSFET

The below figures shows the structure, transfer characteristics and Drain characteristics of p-channel type D-MOSFET.



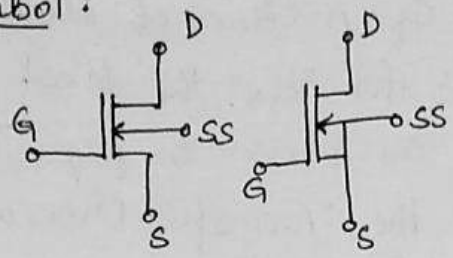


Transfer characteristics

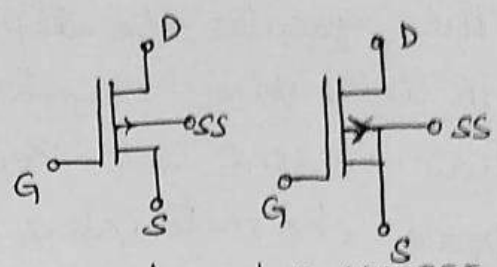


Drain Characteristics

Symbol:



n-channel DMOSFET.



p-channel D-MOSFET.

P-channel depletion type MOSFET construction is exactly reverse of n-channel depletion type MOSFET. In this substrate is n-type, regions and channels are of p-type

Voltage polarities and current directions are reversed. The difference from n-channel characteristics are, V_{DS} is with negative values. V_{GS} will have opposite polarities. and I_D in the opposite direction.

Comparision between JFET & MOSFET

JFET's	MOSFET's
1) JFET is fabricated using a semiconductor bar which acts as a channel	1) MOSFET is fabricated on a semiconductor substrate
2) Fabrication process is complex.	2) Fabrication process is simple and easy
3) JFET does not contain an insulating silicon dioxide layer	3) MOSFET's are fabricated with SiO_2 Layer.
4) JFETs are operated in depletion mode only	4) D-MOSFET is operated in both enhancement mode and depletion mode. E-MOSFET is in Enhancement mode only.
5) JFETs have larger drain resistance in the range of 100KΩ to 1MΩ	5) MOSFETs have lower drain resistances in the range of 1KΩ to 50KΩ.

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