Specification Of Serdes Interface

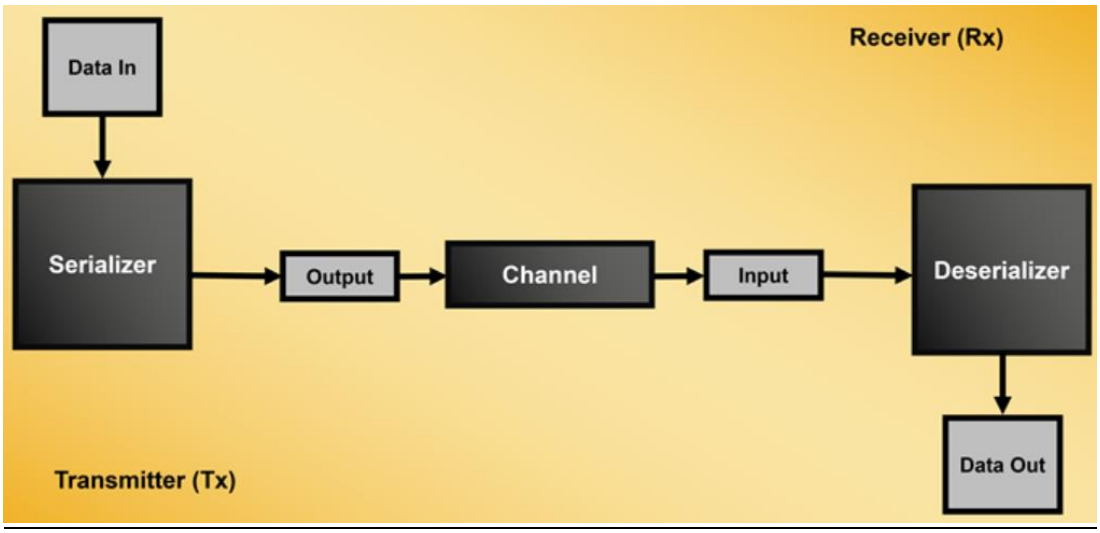
Overview:

This specification defines the SerDes interface of the PMA (Physical Attachment Unit) sublayer, covering the high-speed serial transmit (TX) and receive (RX) Datapath, along with associated clocks, resets.

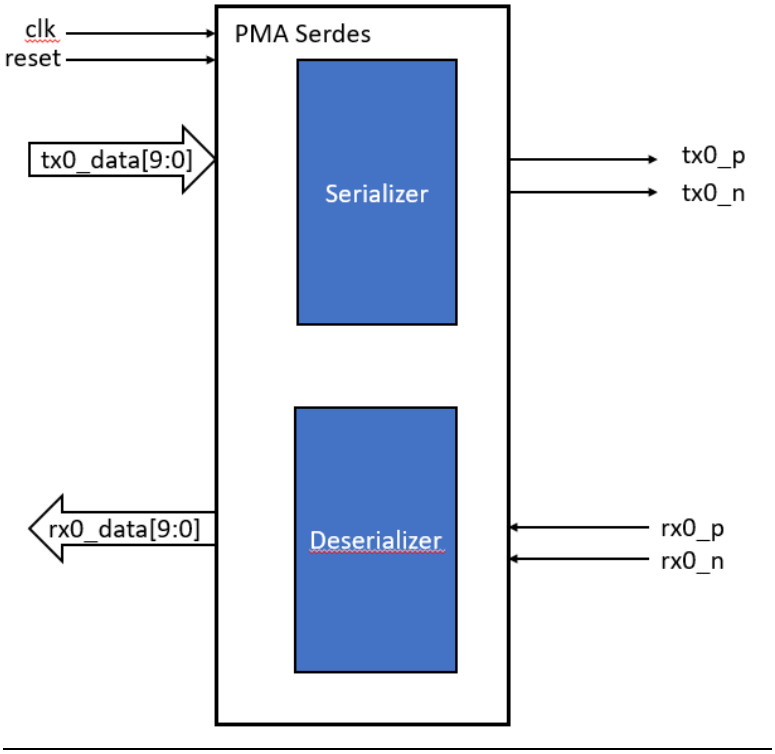
Functionality:

- High-speed serial operation
- Serdes operation
- Differential serial I/O
- Support for loopback
- Support for lane polarity inversion
- Low Power Mode
- Speed selection

Block Diagram:



High-level Diagram:



Explanation:

Serdes is a part of PMA. It has 2 blocks serializer and de-serializer. Serializer will do the conversion of parallel data to serial data and de-serializer will do vice versa. For Tx, the input data will be 10 bits parallel for single lane, the serializer will convert into serial data and transmit on differential signal. The baud rate for parallel and serial will remain same based on the speed selection. Similarly for RX, the input data for PMA will be differential RX signals and de-serializer will convert into the 10 bits parallel data, here also the baud rate will remain same on both sides. The clk and reset will provide as input to PMA.

Configurations:

Here the supported configuration is speed selection from 1G to 10G, the variable no. of lanes, variable parallel data selection, loopback support in which rx data will not be captured, low power mode in which the data and clk will be shut down so the lines will be on high impedance state.

Here the differential signal indicates the polarity inverse of each other i.e. on p and n signals on serial side the data will be compliment of each other.