Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India

(Autonomous College Affiliated to University of Mumbai)

End Semester Examination

August 2021

Max. Marks: 60 **Duration: 2Hrs**
Class: S.E. **Semester: III**
Course Code: ET201/EC201 **Branch: Electronics/ EXTC**
Name of the Course: Computer Architecture and Organization

Instruction:

(1) All questions are compulsory
(2) Draw neat diagrams
(3) Assume suitable data if necessary

Q No.		Max. Marks	CO-BL-PI
Q.1 (a)	Early examples of CISC and RISC design are VAX 11/780 and IBM RS/6000 respectively. Using typical benchmark program the following machine characteristic result: The final column shows VAX required 12 times longer than the IBM measured in CPU time. **Processor** | **Frequency** | **Performance** | **CPU Time** VAX11/780 | 5 MHz | 1 MIPS | 12 x seconds IBM RS/6000 | 25 MHz | 18 MIPS | x seconds (a) What is the relative size of the instruction count of the machine code for this benchmarks program running on two machines? (b) What are the CPI values for the two machines	06	1-3-1.4.1
Q.1 (b)	Differentiate CPU and GPU. "CPU along with GPU increases performance of computer"Justify the statement. OR What is Amadahl's Law? "Amadahl's law demonstrates the law of diminishing returns". Justify the statement with example	03+03	1-2-1.4.1
Q.2 (a)	Perform Restoring division on (-12) / (-5). (Show proper steps and final answer properly) OR Perform (-14) X (+7) using Booth's algorithm. (Show proper steps and final answer properly)	06	2-3-2.1.3
Q.2 (b)	Show how CPU performs floating point division on these numbers $5.78_{10}/10.25_{10}$	06	2-3-2.1.3

Q.3	Design Cache Memory Subsystem for Direct Mapped Cache Organization with following specifications: a) Main memory size = 1 GB b) Block size = 4 bytes c) Cache memory size = 64KB d) Line size in cache = 4 Bytes For the given data, determine the following: a) Address interpretation done by main memory system b) Address interpretation done by cache memory subsystem c) Line entry format d) Process of finding either cache hit or cache miss OR Design Cache Memory Subsystem for Direct Mapped Cache Organization with following specifications: a) Main memory size = 4GB b) Block size = 4 bytes c) Cache memory size = 32KB d) Line size in cache = 4 Bytes For the given data, determine the following: a) Address interpretation done by main memory system b) Address interpretation done by cache memory subsystem c) Line entry format d) Process of finding either cache hit or cache miss	12	3,4-3-2.1.3
Q.4 (a)	A pipeline processor has 4 stages in its pipeline. Experimentally, designers have observed the improvement in the performance approximately 4 times that obtained in non-pipelined processor. You are supposed to mathematically arrive at this conclusion through the derivation. Further, discuss any two challenges in the pipelined processor that will affect the performance in the pipeline.	06	5-2-2.1.2
Q.4 (b)	In computer system, there are typically three methods for I/O data transfer. Compare and contrast these methods .	06	6-2-1.4.1
Q.5 (a)	To execute an instruction of 8086, ADD AX,BX, a control unit is the necessary element. Devise all the micro steps (micro instruction) required by the control unit to accomplish this task.	06	3-2-1.4.1
Q.5 (b)	Compare and contrast different types of memory used in the computer system.	06	4-2-1.4.1