Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (W), Mumbai: 400058, India

(Autonomous College of Affiliated to the University of Mumbai)

Special Examination

August 2023

Maxi Marks: 100 Duration: 3 hours

Class: SE Semester: III

Course code: CS203/AI203/EC201/DS203 Branch: All Branches

Name of the course: Computer Architecture & Organization

Q No		Max Marks	CO
Q.1 (a)	Design Cache Memory Subsystem for Direct Mapped Cache Organization with following specifications: a) Main memory size = 4GB b) Block size = 4 bytes c) Cache memory size = 32KB d) Line size in cache = 4 Bytes For the given data, determine the following: a) Address interpretation done by main memory system b) Address interpretation done by cache memory subsystem c) Line entry format d) Process of finding either cache hit or cache miss **OR** Design Cache Memory Subsystem for Four way Set Associative Cache Organization with following specifications: a) Main memory size = 4GB b) Block size = 4 bytes c) Cache memory size = 32KB d) Line size in cache = 4 Bytes For the given data, determine the following: a) Address interpretation done by main memory system b) Address interpretation done by cache memory subsystem c) Line entry format d) Process of finding either cache hit or cache miss	12	CO 4
Q.1 (b)	Consider a MIPS32 like processor with 32-bit address and 32-bit data bus. Draw memory interfacing diagram with available memory chips (RAM) size of 1 GByte using with and without Memory interleaving	8	CO 4
Q.2 (a)	What is LRU Algorithm? Find the page hit ratio for the following string using FIFO and LRU page replacement policies for the page address stream: 6 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 5 Consider the page frame size n =4.	10	CO 4

<table>
<tr><td>Q.2
(b)</td><td>Explain the instruction cycle of CPU along with data flow diagram for Instruction and Data Fetch, Indirect cycle and Interrupt Cycle

OR
Differentiate between hardwired and microprogrammed control unit design.
Write the control signals for the following instruction:ADD R1, LOCA</td><td>10</td><td>CO3</td></tr>
<tr><td>Q.3
(a)</td><td>Represent 119.16 in IEEE Single Precision Format and Double Precision Format.

OR

Differentiate between Non-Restoring and Restoring Division Algorithms.
Divide 21 by 6 using the Non Restoring Division.</td><td>10</td><td>CO2</td></tr>
<tr><td>Q.3
(b)</td><td>Consider two different machines with instruction sets of 100,000 both of which have a clock rate of 200 Mhz. The following measurements are recorded on two machines running a given set of benchmark programs:
<table><tr><th>Instruction Type</th><th>Instruction Mix (%)</th><th>Cycles per Instruction</th></tr><tr><td><u>Machine A</u>
Arithmetic and Logic
Data Transfer
Control Transfer
Other</td><td>
60
10
15
15</td><td>
2
3
4
2</td></tr><tr><td><u>Machine B</u>
Arithmetic and Logic
Data Transfer
Control Transfer
Other</td><td>
55
20
15
10</td><td>
1
4
3
2</td></tr></table>Determine the effective CPI, MIPS rate and Execution Time for both the machines.</td><td>10</td><td>CO 1</td></tr>
<tr><td>Q.4
(a)</td><td>What are the design Issues arise in Implementing Interrupt I/O. Justify which is the most efficient technique when large volumes of data are to be moved.</td><td>10</td><td>CO6</td></tr>
<tr><td>Q.4
(b)</td><td>Compare Bus Arbitration methods based on their Advantages and Disadvantages</td><td>10</td><td>CO6</td></tr>
<tr><td>Q.5
(a)</td><td>Compare and contrast Non pipelined and Pipelined processor architectures. State and justify the condition to be satisfied to gain the real benefit of the pipelined concept. Discuss the practical hindrance (hazards) that compromises the benefits obtained.</td><td>10</td><td>CO 5</td></tr>
<tr><td>Q.5
(b)</td><td>Which architectures are typically employed for the design of Harvard's style and Von Neumann style? Justify by stating differences between the two architectures.</td><td>10</td><td>CO 3</td></tr>
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