Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (W), Mumbai: 400058, India

(Autonomous College of Affiliated to University of Mumbai)

End Semester Examination

December 2022

Maxi Marks: 100 Duration: 3 hours
Class: SE Semester: III
Course code: CS203/AI203/EC201/DS203 Branch: All Branches
Name of the course: Computer Architecture & Organization

Q No		Max Marks	CO
Q.1 (a)	A Direct Mapped Cache Subsystem needs to be designed having the following specifications: a) Main Memory Size of 1GB b) Block Size of 16 Bytes c) Cache Memory Size of 64 KB d) Line Size of 16 Bytes Answer the following: 1) Address Interpretation by Main Memory 2) Address Interpretation by Cache Memory 3) Design of Line Entry Draw a neat Conceptual Diagram of the System showing all the blocks. OR A Two Way Set Associative Cache Subsystem needs to be designed having the following specifications: a) Main Memory Size of 1GB b) Block Size of 16 Bytes c) Cache Memory Size of 64 KB d) Line Size of 16 Bytes Answer the following: 1) Address Interpretation by Main Memory 2) Address Interpretation by Cache Memory 3) Design of Line Entry Draw a neat Conceptual Diagram of the System showing all the blocks.	12	CO 4
Q.1 (b)	Devise the mechanism to implement Virtual Memory **Segmentation** technique that translates the Virtual Address to its equivalent Physical Address. Your answer must have the supporting diagram of the mechanism.	8	CO 4
Q.2 (a)	Consider the following page reference string: 1,2,3,4,2,1,5,6,2,1,2,3,7,6,3,2,1,2,3,6 How many page faults would occur for the following replacement algorithms, assuming three-page frames? 1. FIFO 2. LRU	10	CO 4

<table>
<tr><td>Q.2
(b)</td><td>Explain the basic organization of the microprogrammed control unit with neat diagram. Write a control store (microprogram) for
(i) ADD R1, R2
(ii) Branch LOCN
OR
Generate the control signals by using Hardwired control unit design for WMFC signal and MARin signal. Use the following instructions:
(i) ADD R1, R2
(ii) ADD R1, LOCA;
(iii) BRANCH LABEL</td><td>10</td><td>CO 3</td></tr>
<tr><td>Q.3
(a)</td><td>What are the largest and smallest positive, finite, normalized numbers that can be represented as IEEE single precision float? Represent 231.56 in IEEE Single Precision Format

OR

Prove how Modified Booths (Bit-Pair Recoding) speed-up the multiplication process as compared to Booths Algorithm by Multiplying the Multiplicand (-17) with the Multiplier (21).</td><td>10</td><td>CO2</td></tr>
<tr><td>Q.3
(b)</td><td>A benchmark program is run first on 200 Mhz and then on 300 Mhz processor. The executed program consists of 1 million instruction execution, with the following instruction mix and clock cycle count:

<table><tr><th>Instruction Type</th><th>Instruction Count</th><th>Cycles per Instruction</th></tr><tr><td>Integer Arithmetic</td><td>4,00,000</td><td>1</td></tr><tr><td>Data Transfer</td><td>3,50,000</td><td>2</td></tr><tr><td>Floating Point</td><td>2,00,000</td><td>3</td></tr><tr><td>Control Transfer</td><td>50,000</td><td>2</td></tr></table>Determine the effective CPI, MIPS rate and Execution Time. Also compare the performance.</td><td>10</td><td>CO 1</td></tr>
<tr><td>Q.4
(a)</td><td>What is the major functionality of I/O Module? Describe the process involved when the user provides input through the keyboard till it is displayed on the monitor.</td><td>10</td><td>CO6</td></tr>
<tr><td>Q.4
(b)</td><td>Compare different Allocation policy and Release Policy for Bus Arbitration.</td><td>10</td><td>CO6</td></tr>
<tr><td>Q.5
(a)</td><td>Compare Instruction level and Processor level parallelism. Discuss in detail data and control pipeline hazards.</td><td>10</td><td>CO 5</td></tr>
<tr><td>Q.5
(b)</td><td>RISC uses Harvard Model and CISC uses Von-Neumann Model", Justify the statement. Explain the important design rules of RISC philosophy.</td><td>10</td><td>CO 3</td></tr>
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