Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (W), Mumbai: 400058, India

ES

(Autonomous College of Affiliated to University of Mumbai)

End Semester Examination

December 2022

Maxi Marks: 100 Duration: 3 hours

Class: SE Semester: III

Course code: CS203/AI203/EC201/DS203 Branch: All Branches

Name of the course: Computer Architecture & Organization

Q No		Max Marks	CO
Q.1 (a)	A Direct Mapped Cache Subsystem needs to be designed having the following specifications: a) Main Memory Size of 16MB b) Block Size of 32 Bytes c) Cache Memory Size of 32 KB d) Line Size of 32 Bytes Answer the following: 1) Address Interpretation by Main Memory 2) Address Interpretation by Cache Memory 3) Design of Line Entry Draw a neat Conceptual Diagram of the System showing all the blocks. OR A Two Way Set Associative Cache Subsystem needs to be designed having the following specifications: a) Main Memory Size of 16MB b) Block Size of 32 Bytes c) Cache Memory Size of 32 KB d) Line Size of 32 Bytes Answer the following: 1) Address Interpretation by Main Memory 2) Address Interpretation by Cache Memory 3) Design of Line Entry Draw a neat Conceptual Diagram of the System showing all the blocks.	12	CO 4
Q.1 (b)	Devise the mechanism to implement Virtual Memory **Paging** technique that translates the Virtual Address to its equivalent Physical Address. Segment translation is **NOT** to be shown. Start translating from the Linear Address onwards. Your answer must have the supporting diagram of the mechanism.	8	CO 4
Q.2 (a)	Consider the following page reference string: 7,0,1,2,0,3,0,4,2,3,0,3,0,3,2,1,2,0,1,7,0,1 How many page faults would occur for the following replacement algorithms, assuming five-page frames? 1. FIFO 2. LRU	10	CO 4

Q.2 (b)	What is the role of a control unit in a processor? What is the difference between a hardwired control unit and a microprogrammed control unit? Explain the relative advantages of a hardwired and a microprogrammed control unit **OR** Write the control signals for the following instructions: (i) ADD R1, LOCA (ii) STORE LOCA, R1 Explain the generation of control signals MDRout, PCin using Hardwired control unit design	10	CO 3
Q.3 (a)	The IEEE single precision floating point standard allows us to represent less than 2^{32} different numbers. Of these numbers, how many are strictly between 2^{13} and 2^{14} ? Represent 56.987 in IEEE Double Precision format. OR Compare Restoring and Non-Restoring Division Algorithm, divide 23 by 11 using the Non-Restoring Division Algorithm.	10	CO2
Q.3 (b)	Consider two different machines with instruction set of 100,000 both of which have clock rate of 400 Mhz. The following measurements are recorded on two machines running a given set of bench mark programs: **Instruction Type** **Instruction Mix (%)** **Cycles per Instruction** Machine A Arithmetic and Logic 50 2 Data Transfer 15 3 Control Transfer 15 4 Other 20 2 Machine B Arithmetic and Logic 65 1 Data Transfer 15 4 Control Transfer 10 3 Other 10 2 Determine the effective CPI, MIPS rate and Execution Time for both the machines.	10	CO 1
Q.4 (a)	Describe the Structure of I/O Module. What are the types of I/O commands that an I/O module may receive when it is addressed by a processor?	10	CO6
Q.4 (b)	Compare different implementation techniques for Centralized bus arbitration.	10	CO6
Q.5 (a)	Describe the Flynn's classification of parallel processing system in detail.	10	CO 5
Q.5 (b)	Compare RISC and CISC design philosophies in detail (atleast five points of difference). Comment on the performance equation given below for RISC and CISC processor approach. $\frac{\text{time}}{\text{program}} = \frac{\text{time}}{\text{cycle}} \times \frac{\text{cycles}}{\text{instruction}} \times \frac{\text{instructions}}{\text{program}}$	10	CO 3