Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (W), Mumbai: 400058, India

(Autonomous College of Affiliated to University of Mumbai)

End Semester Examination

December 2022

Maxi Marks: 100 Duration: 3 hours

Class: SE Semester: III

Course code: CS203/AI203/EC201/DS203 Branch: All Branches

Name of the course: Computer Architecture & Organization

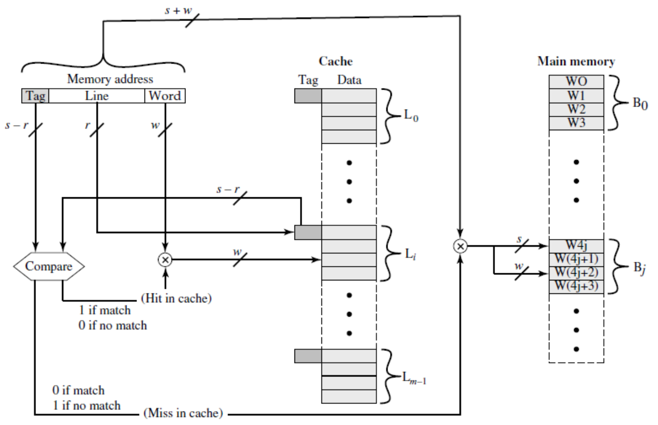
<table>
<tr><th>Q No</th><th></th><th>Max Marks</th><th>CO</th></tr>
<tr><td>Q.1 (a)</td><td>
A Direct Mapped Cache Subsystem needs to be designed having the following specifications:
a) Main Memory Size of 1GB
b) Block Size of 16 Bytes
c) Cache Memory Size of 64 KB
d) Line Size of 16 Bytes
Answer the following:
1) Address Interpretation by Main Memory
2) Address Interpretation by Cache Memory
3) Design of Line Entry
Draw a neat Conceptual Diagram of the System showing all the blocks.
Answer: Address Interpretation by Main Memory
<table><tr><td>Block bits = 26 bits</td><td>Word bits = 4 bits</td></tr></table>
----- 3 marks
Address Interpretation by Cache Memory
<table><tr><td>Page bits = 14 bits</td><td>Line bits = 12 bits</td><td>Word bits = 4 bits</td></tr></table>
----- 3 marks
Design of Line Entry
<table><tr><td>Tag bits = 14 bits</td><td>V bit =1</td></tr></table>
----- 3 marks
Conceptual Diagram


Figure 4.9 Direct-Mapping Cache Organization
----- 3 marks
</td><td>12</td><td>CO 4</td></tr>
</table>

OR

A Two Way Set Associative Cache Subsystem needs to be designed having the following specifications:

a) Main Memory Size of 1GB
b) Block Size of 16 Bytes
c) Cache Memory Size of 64 KB
d) Line Size of 16 Bytes

Answer the following:

1) Address Interpretation by Main Memory
2) Address Interpretation by Cache Memory
3) Design of Line Entry

Draw a neat Conceptual Diagram of the System showing all the blocks.

Answer: Address Interpretation by Main Memory

Block bits = 26 bits	Word bits = 4 bits

----- 3 marks

Address Interpretation by Cache Memory

Page bits = 15 bits	Line bits = 11 bits	Word bits = 4 bits

----- 3 marks

Design of Line Entry

Tag bits = 15 bits	V bit =1

----- 3 marks

Conceptual Diagram

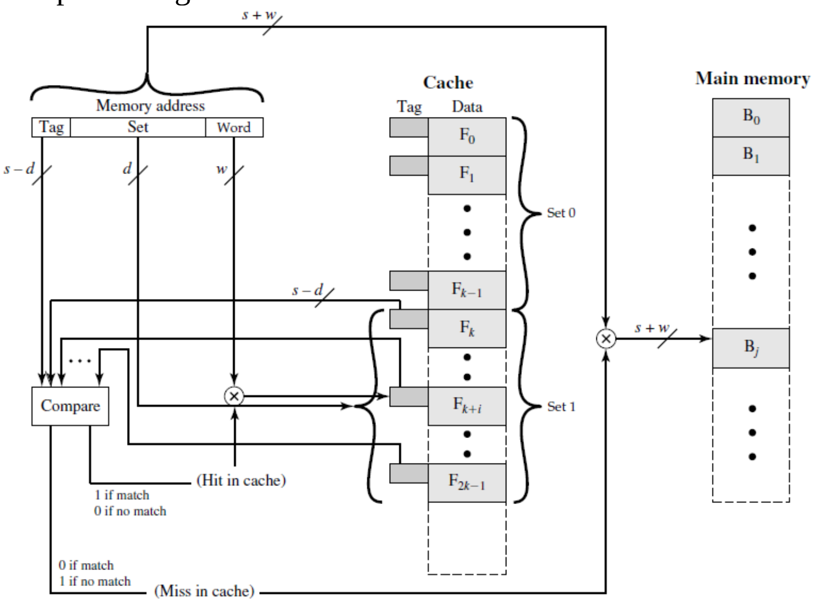
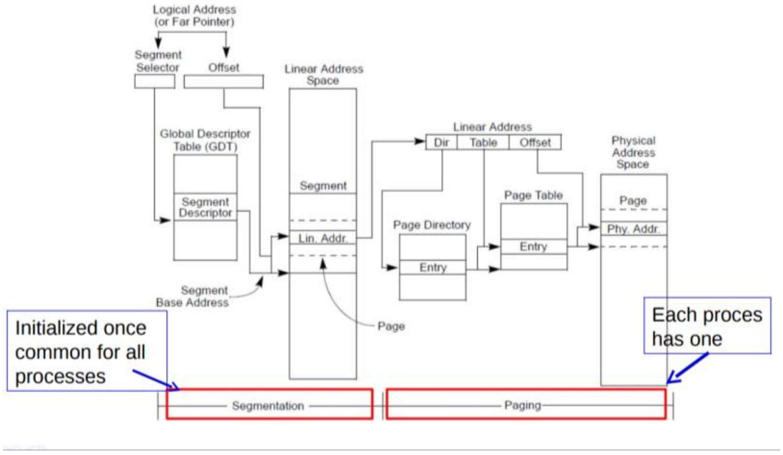


Figure 4.14 *K*-Way Set Associative Cache Organization

----- 3 marks

Q.1 (b)	Devise the mechanism to implement Virtual Memory **Segmentation** technique that translates the Virtual Address to its equivalent Physical Address. Your answer must have the supporting diagram of the mechanism.	8	CO 4



Initialized once common for all processes

Each proces has one

…………8 marks for diagram and explanation

Q.2 (a)

Consider the following page reference string:
1,2,3,4,2,1,5,6,2,1,2,3,7,6,3,2,1,2,3,6

How many page faults would occur for the following replacement algorithms, assuming three-page frames?

1. FIFO
   Page Hits = 4
   Page Fault = 16……………… 5 marks
2. LRU
   Page Hits = 5
   Page Fault = 15…………………… 5 marks

10

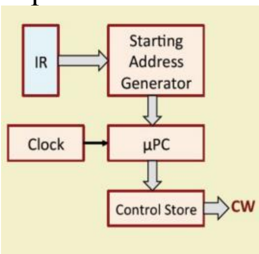
CO 4

Q.2 (b)

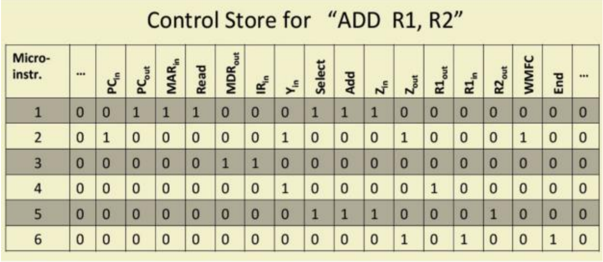
Explain the basic organization of the microprogrammed control unit with neat diagram. Write a control store (microprogram) for

(i) ADD R1, R2
(ii) Branch LOCN

Answer: Microprogrammed Control Unit design : Diagram and explanation…………………………………….. 4 marks



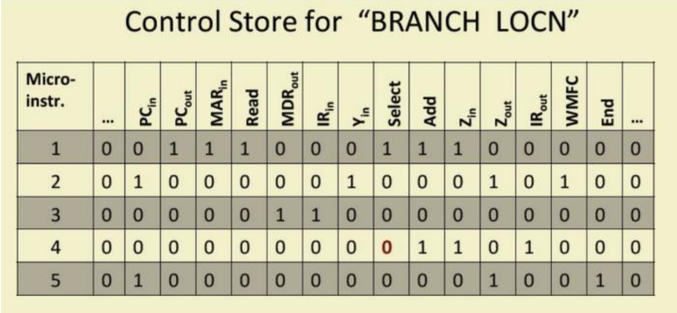
Control store for ADD R1, R2……………………3 marks



Control Store for “ADD R1, R2”

Micro-instr.	…	PC_{in}	PC_{out}	MAR_{in}	Read	MDR_{out}	IR_{in}	Y_{in}	Select	Add	Z_{in}	Z_{out}	$R1_{out}$	$R1_{in}$	$R2_{out}$	WMFC	End	…
1	0	0	1	1	1	0	0	0	1	1	1	0	0	0	0	0	0	0
2	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0
3	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0
5	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0

Control store for BRANCH LOCN……………………3 marks



Control Store for “BRANCH LOCN”

Micro-instr.	…	PC_{in}	PC_{out}	MAR_{in}	Read	MDR_{out}	IR_{in}	Y_{in}	Select	Add	Z_{in}	Z_{out}	IR_{out}	WMFC	End	…
1	0	0	1	1	1	0	0	0	1	1	1	0	0	0	0	0
2	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0
3	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0
5	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0

10

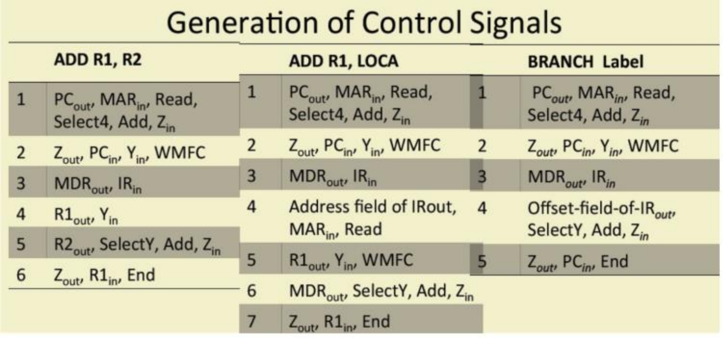
CO 3

OR

Generate the control signals by using Hardwired control unit design for WMFC signal and MARin signal. Use the following instructions:

(i) ADD R1, R2
(ii) ADD R1, LOCA;
(iii) BRANCH LABEL

Control signals for ADD R1, R2…………………………………………...(2)
Control signals for ADD R1, LOCA………………..……………………….…..(2)
Control signals for (i) BRANCH LABEL…………………………………..(2)
Hardwired control design for WMFC……………………………………(2)
Hardwired control design for MARin…………………………………….……(2)



Generation of Control Signals

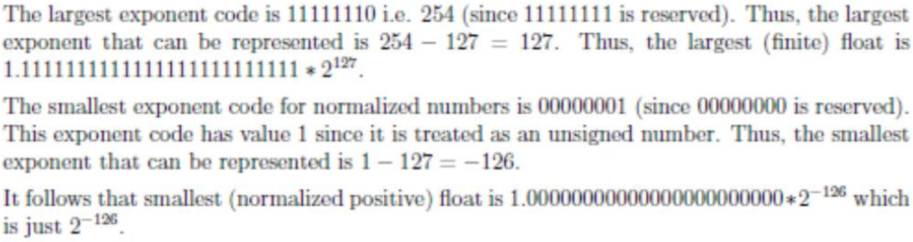
ADD R1, R2		ADD R1, LOCA		BRANCH Label	
1	PC_{out}, MAR_{in}, Read, Select4, Add, Z_{in}	1	PC_{out}, MAR_{in}, Read, Select4, Add, Z_{in}	1	PC_{out}, MAR_{in}, Read, Select4, Add, Z_{in}
2	Z_{out}, PC_{in}, Y_{in}, WMFC	2	Z_{out}, PC_{in}, Y_{in}, WMFC	2	Z_{out}, PC_{in}, Y_{in}, WMFC
3	MDR_{out}, IR_{in}	3	MDR_{out}, IR_{in}	3	MDR_{out}, IR_{in}
4	$R1_{out}$, Y_{in}	4	Address field of IRout, MAR_{in}, Read	4	Offset-field-of-IR_{out}, SelectY, Add, Z_{in}
5	$R2_{out}$, SelectY, Add, Z_{in}	5	$R1_{out}$, Y_{in}, WMFC	5	Z_{out}, PC_{in}, End
6	Z_{out}, $R1_{in}$, End	6	MDR_{out}, SelectY, Add, Z_{in}		
		7	Z_{out}, $R1_{in}$, End		

Q.3 (a)

What are the largest and smallest positive, finite, normalized numbers that can be represented as IEEE single precision float? Represent 231.56 in IEEE Single Precision Format

10

CO2



The largest exponent code is 11111110 i.e. 254 (since 11111111 is reserved). Thus, the largest exponent that can be represented is $254 - 127 = 127$. Thus, the largest (finite) float is $1.11111111111111111111111 * 2^{127}$.

The smallest exponent code for normalized numbers is 00000001 (since 00000000 is reserved). This exponent code has value 1 since it is treated as an unsigned number. Thus, the smallest exponent that can be represented is $1 - 127 = -126$.

It follows that smallest (normalized positive) float is $1.00000000000000000000000 * 2^{-126}$ which is just 2^{-126}.

[5 Marks]

Representation of 231.56[5 Marks]
127+7 =134 (10000110)

OR

Prove how Modified Booths (Bit-Pair Recoding) speed-up the multiplication process as compared to Booths Algorithm by Multiplying the Multiplicand (-17) with the Multiplier (21).

Comparison of Bit-Pair Recoding and Booths Algorithm[4 Marks]

Multiplying the Multiplicand (-17) with the Multiplier (21)[6 marks]

Q.3 (b)

A benchmark program is run first on 200 Mhz and then on 300 Mhz processor. The executed program consists of 1 million instruction execution, with the following instruction mix and clock cycle count:

10

CO 1

Instruction Type	Instruction Count	Cycles per Instruction

	Integer Arithmetic 4,00,000 1 Data Transfer 3,50,000 2 Floating Point 2,00,000 3 Control Transfer 50,000 2 Determine the effective CPI, MIPS rate and Execution Time. Also compare the performance. 1. Effective CPI = 108/100 = 1.8 [3 marks] 2. MIPS(200 MHz)= 111.11 MIPS (300 MHz)= 166.66 [3 marks] 3. XTime1 = 90 ms XTime2 = 60 ms 300 MHz processor is faster by 66%. [4 marks]		
Q.4 (a)	What is the major functionality of I/O Module? Describe the process involved when the user provides input through the keyboard till it is displayed on the monitor. The major functions or requirements for an I/O module fall into the following[5 Marks] categories: • Control and timing • Processor communication • Device communication • Data buffering • Error detection The process involved when the user provides input through the keyboard till it is displayed on the monitor.[5 Marks] • When the user depresses a key it generates an electronic signal that is interpreted by the transducer in the keyboard and translated into the bit pattern of the corresponding IRA code • This bit pattern is transmitted to the I/O module in the computer • On output, IRA code characters are transmitted to an external device from the I/O module • The transducer interprets the code and sends the required electronic signals to the output device either to display the indicated character or perform the requested control function	10	CO6
Q.4 (b)	Compare different Allocation policy and Release Policy for Bus Arbitration. Bus Allocation Policy[6 Marks] • Fixed priority • Each master is assigned a fixed priority • Highest priority master always gets the bus • Priorities can be assigned based on the importance of service • Rotating priority • Priority is not fixed • Several ways of changing priority	10	CO6

	– Increase the priority as a function of waiting time – Lowest priority for the master that just received the bus • Fair policies • A fair policy will not allow starvation – Rotating priority policies are fair • Fair policies need not use priorities • Fairness can be defined in several ways – A window-based request satisfaction – Within a specified time period » In PCI, we can specify the maximum delay to grant a request • Hybrid policies • Both priority and fairness can be incorporated into a single policy Release Policy[4 Marks] • Non-preemptive – Current master voluntarily releases the bus – Disadvantage » May hold bus for long time 1. Transaction-based release 2. Demand-driven release • Preemptive – Forces the current master to release the bus without completing its bus transaction		
Q.5 (a)	Compare Instruction level and Processor level parallelism. Discuss in detail data and control pipeline hazards. Compare Instruction level and Processor level parallelism.[4 Marks] Data Hazards[3 Marks] • Read after write (RAW), or true dependency – An instruction modifies a register or memory location – Succeeding instruction reads data in memory or register location – Hazard occurs if the read takes place before write operation is complete • Write after read (WAR), or antidependency – An instruction reads a register or memory location – Succeeding instruction writes to the location – Hazard occurs if the write operation completes before the read operation takes place • Write after write (WAW), or output dependency – Two instructions both write to the same location – Hazard occurs if the write operations take place in the reverse order of the intended sequence Control Hazards[3 Marks] • Occurs when the pipeline makes the wrong decision on a branch prediction	10	CO 5

	• Brings instructions into the pipeline that must subsequently be discarded • Dealing with Branches: – Multiple streams – Prefetch branch target – Loop buffer – Branch prediction – Delayed branch		
Q.5 (b)	RISC uses Harvard Model and CISC uses Von-Neumann Model", Justify the statement. Explain the important design rules of RISC philosophy. Justification of statement with explanation …………… 5 marks Harvard makes it harder to write ♣ Self-modifying code (data values used as instructions) ♣ Less reprogrammable ♣ Harvard allows two simultaneous memory fetches. ♣ Harvard architectures are widely used because • The separation of program and data memories ◊ greater memory bandwidth ◊ higher performance for digital signal processing • Speed is gained at the expense of more complex electrical circuitry. Reduced Instruction Set Computer (RISC) ♣ Compact, uniform instructions ◊ facilitate pipelining ♣ More lines of code ◊ poor memory footprint ♣ Allow effective compiler optimization Design Rules of RISC philosophy….. 5 rules … 5 marks --One instruction per cycle. – Register–to–register operations. – Simple addressing modes. – Simple instruction form ---Load Store architecture --- pipelining can be easy --- Fixed instruction format ---- Complexity in compiler	10	CO 3