Sardar Patel Institute of Technology

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(Autonomous College of Affiliated to University of Mumbai)

End Semester Examination

December 2023

Maxi Marks: 100 Duration: 3 hours

Class: SE Semester: III

Course code: CS203/AI203/EC201/DS203 Branch: All Branches

Name of the course: Computer Architecture & Organization

Q No		Max Marks	CO
Q.1 (a)	You have a program that consists of two parts: a serial portion that takes up 30% of the execution time and a parallel portion that takes up the remaining 70%. If you parallelize the entire parallel portion perfectly on a system with 8 processors, calculate the theoretical overall speedup obtained according to Amdahl's law.	05	CO1
Q.1 (b)	In a RISC ISA implementation, you have four instruction types with the following characteristics: Load Instruction: Frequency = 25%, CPI = 5 Store Instruction: Frequency = 10%, CPI = 4 ALU Instruction: Frequency = 55%, CPI = 2 Branch Instruction: Frequency = 10%, CPI = 3 Additionally, if you were to achieve a 30% reduction in the CPI of the ALU instruction by implementing some optimizations, what would be the new weighted Average CPI for this mix of instructions?	05	CO1
Q.1 (c)	Consider a computing system with the following characteristics: Original Instruction Count (IC): 60,000,000 Original Clock Rate (CR): 2.2 GHz (2,200,000,000 Hz) Original CPI (Cycles Per Instruction): 3.5 Now, an upgrade to the system is proposed with the following changes: a. The new compiler reduces the Instruction Count to 50,000,000 (New IC). b. However, the new CPU architecture has a higher CPI of 4.0 (New CPI). c. The clock rate of the new CPU is faster, with a Clock Rate of 3.0 GHz (3,000,000,000 Hz). Calculate and compare the execution times (ET) for both the original and upgraded scenarios.	05	CO1
Q.2(a)	Compare Restoring and Non-Restoring Division algorithms. Divide 33 by 10 using Non-Restoring Division with flow chart.	08	CO2

Q.2 (b)	The following numbers use the IEEE 32-bit floating point numbers. What is the equivalent decimal value? (1) 11000001111000000000000000000000 (2) 00111111010100000000000000000000	07	CO2
Q.3 (a)	In a CPU, control unit can be designed by two different methods viz. Hardwired and Microprogrammed. Compare and contrast Hardwired and Microprogrammed control unit design. One of the processors from INTEL has 125 control signals which can be divided into 5 groups of mutually exclusive signals as follows: Group 1: 20 signals, Group 2: 70 signals, Group 3: 2 signals, Group 4: 10 signals, Group 5: 23 signals. How many bits of the control word (microinstruction register) can be saved by using **Diagonal** Microprogramming over **Horizontal** and **Vertical** Microprogramming? **OR** Design the hardwired control unit to generate **MDRout** and **R1out** signals. Use the following instructions: (i) **STORE R1, [R2];** Stores the content of register R1 into the memory location whose address is in register R2. (ii) **LOAD R1, [R2];** Loads the content of the memory location whose address is in register R2 into register R1. (iii) **BRANCHZ R1, LABEL;** Branches to the instruction labelled "LABEL" if the content of register R1 is zero.	10	CO3
Q.3 (b)	Compare and contrast RISC and CISC architectures in terms of their key design principles, advantages, and disadvantages. Discuss how the differences between RISC and CISC architectures impact instruction execution, memory utilization, and overall performance. Design efficient instruction sequences for sorting an array of integers in ascending order on both a RISC (Reduced Instruction Set Computing) and a CISC (Complex Instruction Set Computing) processor.	10	CO3
Q.3 (c)	Describe the states of instruction and draw its state diagram showing the possible flow of data-path in any instruction	05	CO3
Q.4 (a)	A Direct Mapped Cache Subsystem needs to be designed having the following specifications: a) Main Memory Size of 4GB b) Block Size in Main Memory of 64 Bytes c) Cache Memory Size of 128KB d) Line Size in Cache Memory of 64 Bytes Answer the following: 1) Address Interpretation by Main Memory 2) Address Interpretation by Cache Memory 3) Design of Line Entry associated with each line of cache. Draw a neat Conceptual Diagram of the System showing all the blocks. **OR** A Two Way Set Associative Cache Subsystem needs to be designed having the following specifications: a) Main Memory Size of 4GB b) Block Size in Main Memory of 64 Bytes c) Cache Memory Size of 128 KB	10	CO 4

	d) *Line Size in Main Memory of 64 Bytes* Answer the following: 1) Address Interpretation by Main Memory 2) Address Interpretation by Cache Memory 3) Design of Line Entry associated with line of cache. Draw a neat Conceptual Diagram of the System showing all the blocks.		
Q.4 (b)	Consider the following page reference string: P,Q,R,S,Q,P,T,U,Q,P,Q,R,V,U,R,Q,P,Q,R,U How many page faults would occur for the following replacement algorithms, assuming three-page frames? 1. FIFO 2. LRU	10	CO 4
Q.4 (c)	Virtual Memory Concept creates some kind of illusion in programmer's mind. Discuss about this illusion and hence compare Segmentation and Paging in brief.	5	CO 4
Q.5 (a)	Compare and contrast Non-Pipelining and Pipelining Processors. To avail all the benefits of Pipelining Processors, one needs to eliminate or minimize various types of Pipeline Hazards. Discuss these hazards in detail.	10	CO 5
Q.5 (b)	Compare and contrast any two I/O data transfer methods in detail.	05	CO6
Q.5 (c)	Discuss Flynn's classification for Parallel Computing	05	CO6