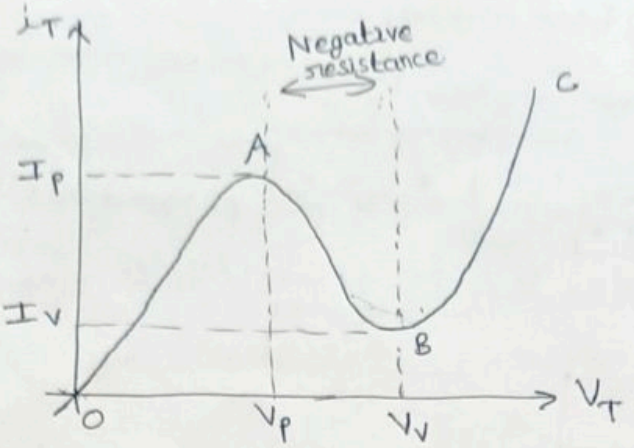
Fig (iii) V-I characteristics



$\uparrow R = \frac{V\uparrow}{I\downarrow}$

→ In p-type semi-conductor, there is increased concentration of holes in the valence band.

Fig (ii)(a) No forward bias :-

When the N-type materials are joined, the EBD under no-bias condition becomes as shown in Fig (ii) a). The junction barrier produces only a rough allignment of the 2 materials. Here the depletion region between the two is extremely narrow due to high doping on both sides of the junction.

→ The potential hill is also increased as shown.

Fig (ii b) Small Forward bias :-

When small forward voltage ($\cong 0.1$ V.) is applied, there is downward movement of the N-region, than the P-region V.B will be exactly aligned with the N-region conduction band.

→ At this stage, electrons will tunnel through the depletion layer with high velocity and produces peak current (I_p)

Fig (ii c) Large forward bias :-

When the forward bias is further increased, the 2 bands get out of allignment. Hence, ~~de~~ tunneling of electrons stop thereby decreasing the current.

→ Since current decreases with increase in applied voltage (i.e dv/dI is negative), the junction is having negative resistance at this stage

(iii) V-I characteristics

→ The resistance increases throughout the negative region.

→ When applied forward voltage is increased further, the current starts increasing once again as in a normal junction diode

V-I characteristics :-

→ As shown in fig (iii), as soon as forward bias is applied, significant current is produced. At the particular voltage called peak voltage (V_p) (point A), the current quickly rises to its peak value 'I_p'.

→ When forward voltage is increased further, diode current starts decreasing till it achieves minimum value called valley current 'I_v' corresponding to valley voltage (V_v) (point B).

→ For voltages greater than 'V_v', current starts increasing as in an ordinary junction diode.

→ Tunnel diode is having negative resistance in the region AB.

* SCR Working principle

SCR is the silicon Controlled Rectifier. It is used to control AC to DC conversion. So the name Silicon Controlled Rectifier.

Working :- It operates in 4 modes.

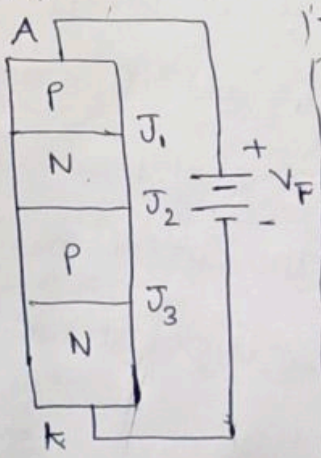
(1) Forward blocking mode (FBM)
(2) Forward Conduction mode (FCM)
(3) Reverse blocking mode (RBM)
(4) Reverse conducting mode (RCM)

* SCR will conduct only when,

$J_1 \rightarrow$
$J_2 \rightarrow$
$J_3 \rightarrow$
} Forward Bias (F·B)

(1) Forward blocking mode.

Here $J_1 \rightarrow$ F·B ✓
$J_2 \rightarrow$ R·B ×
$J_3 \rightarrow$ F·B ✓

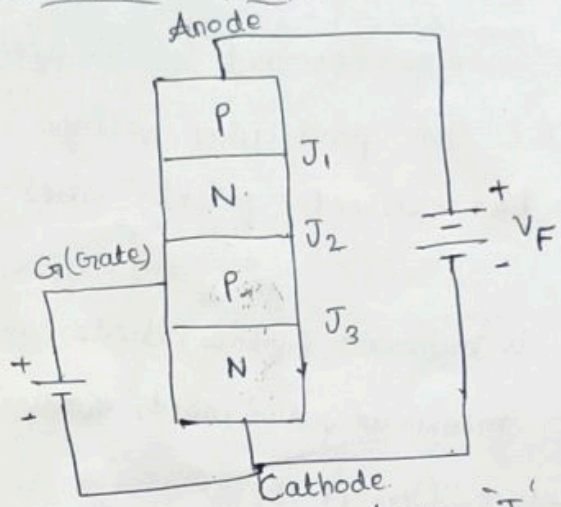


→ As no anode current 'I_A' flows in the circuit, the device is said to be in off state and leakage current which flows through SCR is called off state current.

(iii) T characteristics:

Here, as junction J_2 is Reverse biased, SCR will not conduct. So if we increase the voltage, very less current is produced.

2) Forward Conduction Mode



Here $J_1 \rightarrow$, $J_2 \rightarrow$, $J_3 \rightarrow$ } Forward biased

→ Without break down of junction, J_2 SCR can be made 'on' by applying a positive voltage to gate w.r.t cathode.

→ Thus, due to gate potential there is a diffusion of electrons from N region to P region and diffusion of holes from P region to N region across the junction J_3.

→ The injection of electrons in P region force this region to loose its identity as 'P' region.

→ Because of this injected electrons, P region has both electrons and holes as majority carriers.

→ ∴ junction J_2 has electrons as majority carriers on its both sides and thus it is disappeared and the device starts conducting as junctions J_1 and J_3 are already in forward biased.

→ As J_1, J_2, J_3 are forward biased, there is free flow of electrons in the SCR and the current flows in the SCR.

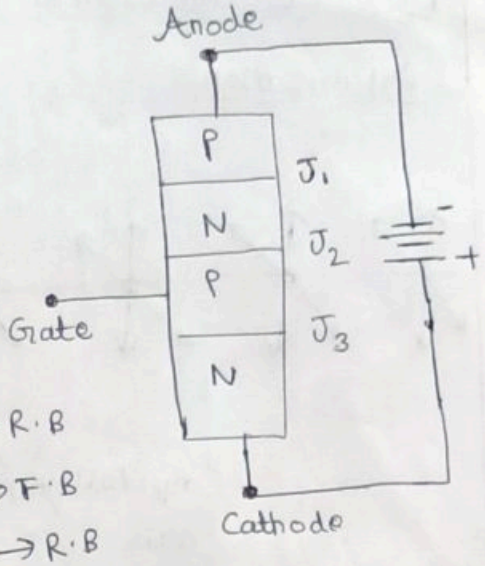
→ The forward voltage at which device starts conducting depends on gate current.

(iii) T characteristics..

3) Reverse blocking mode:-

When cathode voltage is positive w.r.t anode, the junction 'J_2' is forward biased and junctions J_1 and J_3 are reverse biased.

→ Due to two reverse bias junctions, only reverse leakage current known as reverse current flows in the device and device said to be in reverse blocking state.

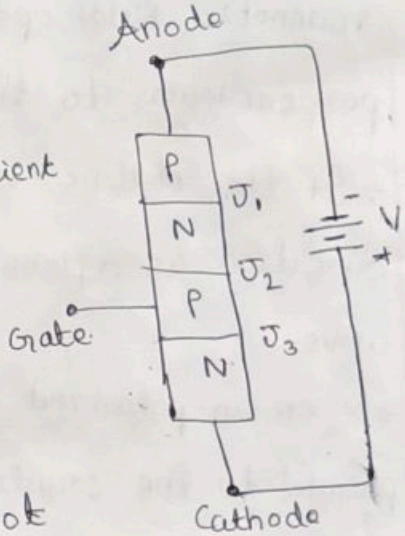


$J_1 \rightarrow R \cdot B$
$J_2 \rightarrow F \cdot B$
$J_3 \rightarrow R \cdot B$

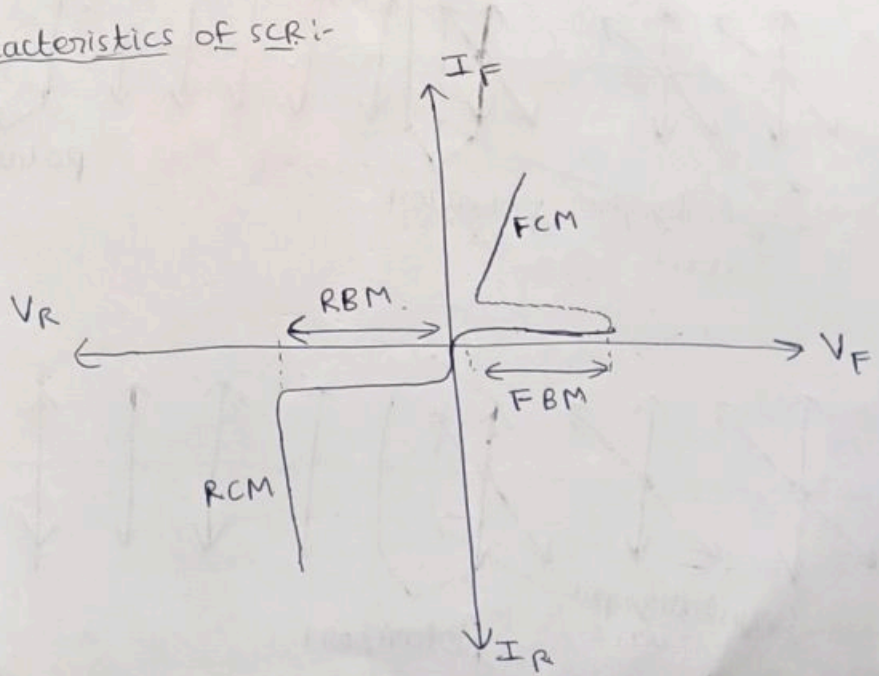
4) Reverse conducting mode:-

If the reverse voltage is increased to a sufficient large value, the breakdown of junctions J_1 and J_3 takes place and device will conduct.

→ This avalanche breakdown of junctions could be destructive and hence device is not used in this mode of operation.



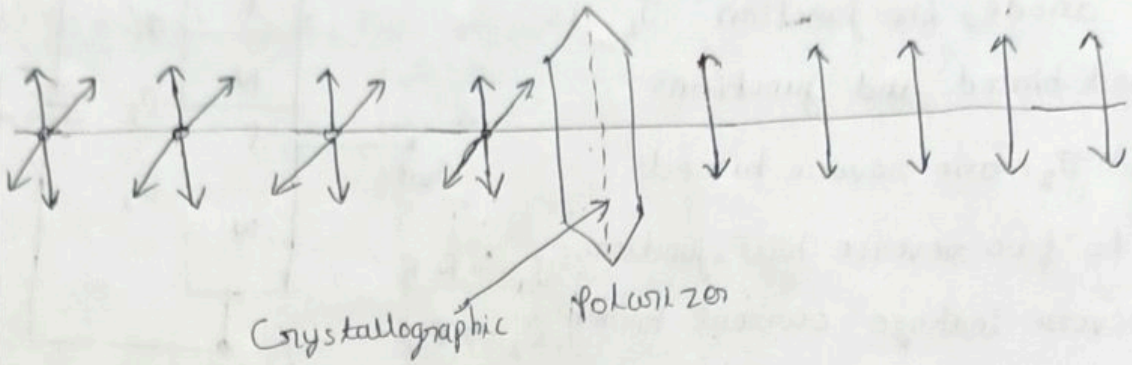
V-I characteristics of SCR:-



(iii) + chromatometer

* LCD (Liquid Crystal Display)

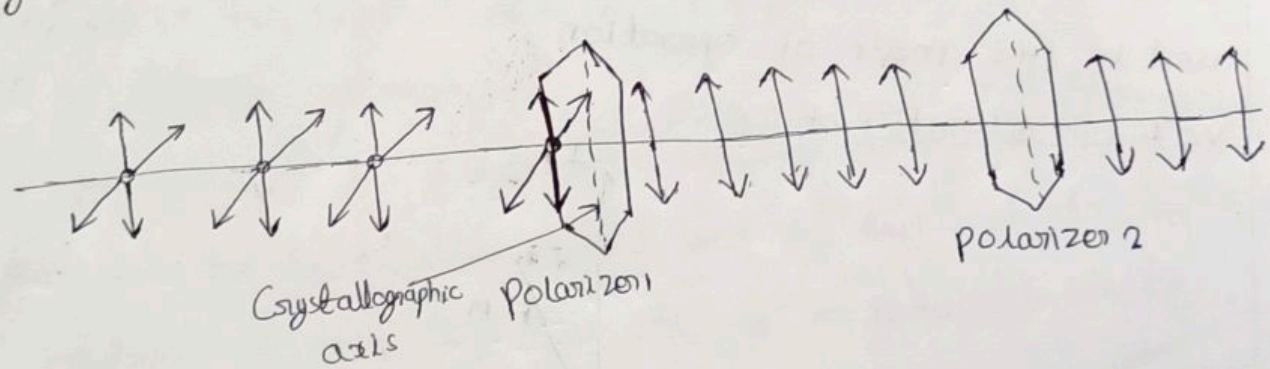
Polarization

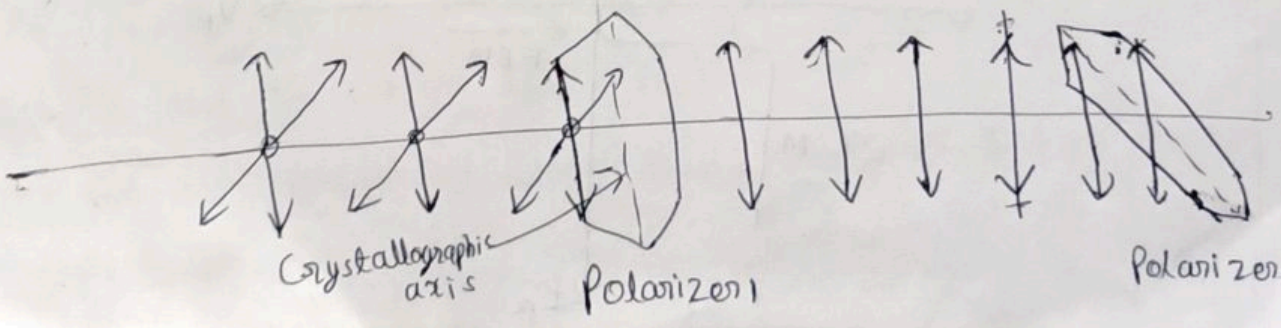


⇒ Light is the electromagnetic wave, that has electric and magnetic fields perpendicular to each other & these fields are perpendicular to the light

⇒ If the electric vector vibrations are confined to a particular direction in a plane then such light wave is called as polarized light wave.

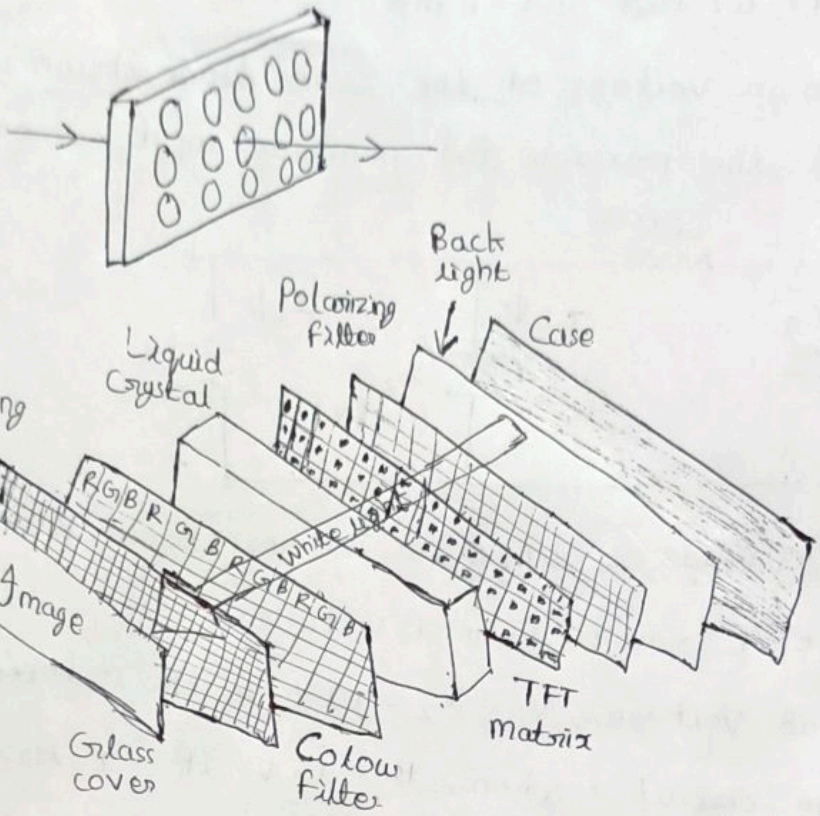
⇒ When un-polarized light passes through a polarizer, the vibrations parallel to the crystallographic axis only pass through and polarized light is obtained.



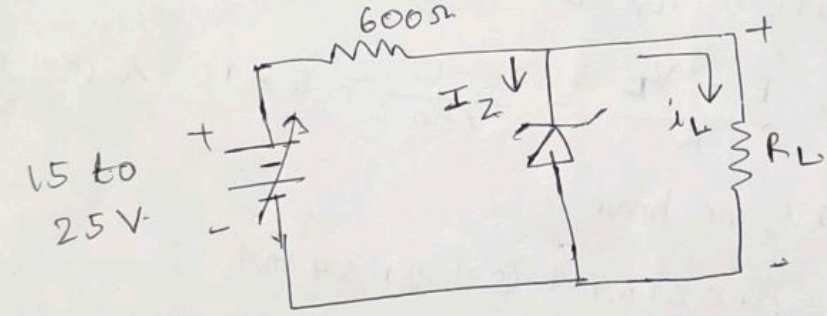


(iii) I characteristics

Liquid Crystal Display:-



2) In the below fig. if $R_L = 3\,k\Omega$, find the maximum and minimum zener currents. Given break down voltage is 12V.



Sol: Given voltage across R_L is $V_L = V_Z = 12V$ (fixed), &

$R_L = 3\,k\Omega$ (fixed).

Load current, $I_L = \frac{V_L}{R_L} = \frac{12}{3000} = 4 \times 10^{-3}\,A$ (or) $4\,mA$

(i) When $E = 15V$, $I = 5\,mA$.

We have, $I = I_L + I_Z$ (or) $I_Z = I - I_L$

$\therefore I_Z = 5 - 4 = 1\,mA$

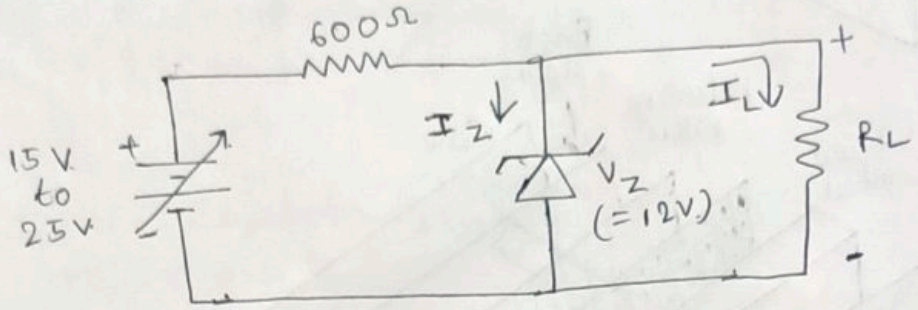
(ii) When $E = 25V$, $I = 21.67\,mA$.

$I_Z = 21.67 - 4 = 17.67\,mA$

Hence maximum and minimum zener currents are;

17.67 mA and 1 mA.

4) The breakdown voltage of the zener diode shown in the figure is 12 V. Find the maximum and minimum input currents.



Sol Given zener voltage, $V_Z = 12\,V$, series resistance, $R = 600\,\Omega$ and supply voltage 'E' ranges from 15 V to 25 V.

We have load voltage, $V_L = V_Z = 12\,V$, & this is fixed.

(i) From the circuit, when $E = 15\,V$, if 'I' is the current supplied by the source, we have:

$E = IR + V_Z$ ((or) V_L) by KVL applied to the loop,

$$\therefore I = \frac{E - V_L}{R} = \frac{15-12}{600} = 5 \times 10^{-3}\,A \text{ (or) } 5\,mA.$$

(ii) When $E = 25\,V$, we have:

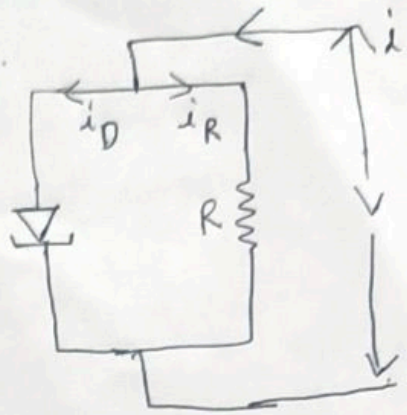
$$I = \frac{25-12}{600} = 0.02167\,A \text{ (or) } 21.67\,mA,$$

Hence the maximum and minimum values of input currents are 21.67 mA & 5 mA.

3) A resistor 'R' is placed parallel to a Ge tunnel diode. The tunnel diode has, $\left|\frac{di_d}{dv}\right|_{max} = \frac{1}{10}\,\Omega$.

Find the value of R, so that the combination does not exhibit negative resistance region in its volt-ampere characteristics.

Sol: The combination is called as tunnel resistor.



If the V-I characteristics were to exhibit no negative resistance region, the slope of the curve. $\left|\frac{di}{dv}\right| \geq 0$, for all 'V'.

$$(i \text{ (or) } I) = i_D + i_R$$

$$(i \text{ (or) } I = i_D + \frac{V}{R}$$

$$\frac{di}{dv} = \frac{di_D}{dv} + \frac{1}{R} \geq 0$$

$$\therefore \frac{1}{R} \geq \left|\frac{di_D}{dv}\right|$$

But it is given that $\left|\frac{di_D}{dv}\right|_{max} = \frac{1}{10}$ mhos

$\therefore$ 'R' should be atleast 10 Ω, so that there is no negative resistance region in the characteristics.

4) The transition capacitance of an abrupt junction diode is 20PF. at 5V. Compute the value of decrease in capacitance for a 1.0 Volt increase in the bias.

Sol: $C_T \propto \frac{1}{\sqrt{V}}$; $C_T = 20$ PF ; when $V = 5$ V

$$20 = \frac{k}{\sqrt{5}} \text{ ; } k \text{ is constant.}$$

$$k = 20\sqrt{5}$$

When $V = 6$ v, $C_T = ?$

$$C_T = \frac{20\sqrt{5}}{\sqrt{6}} = 18.25 \text{ PF.}$$

$\therefore$ decrease in the value of capacitance is $20 - 18.25 = 1.75$ PF