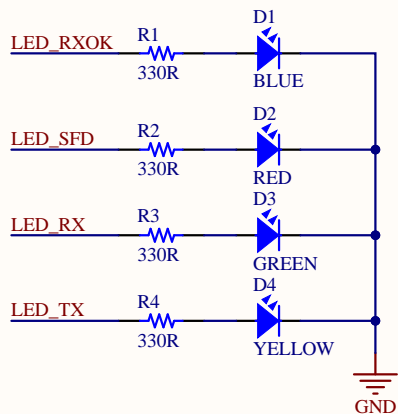
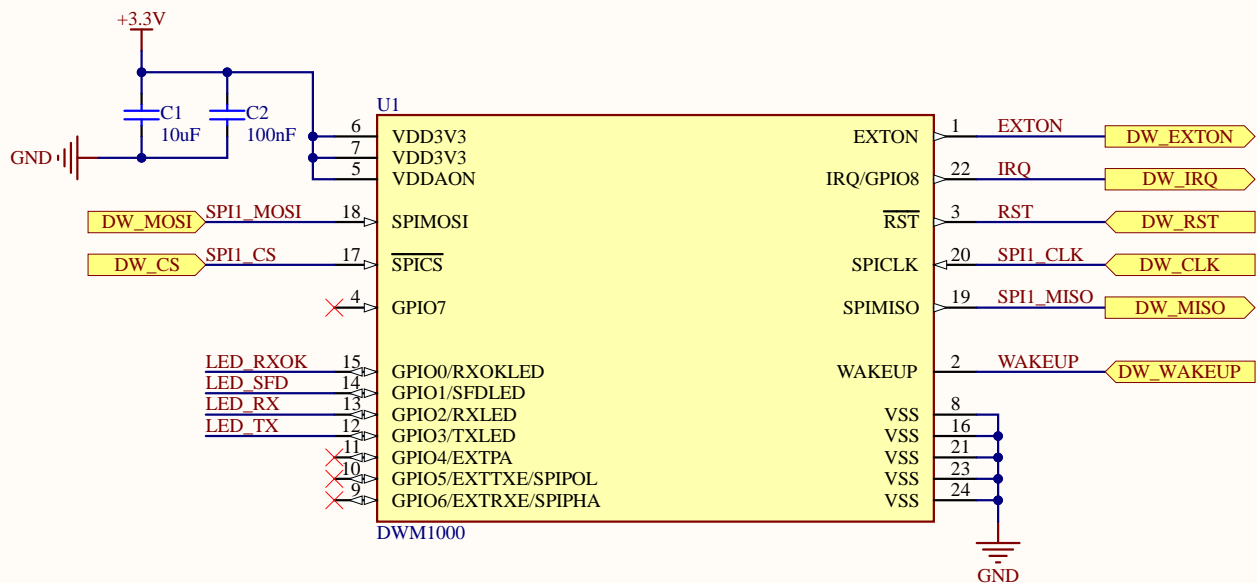


A

B

C

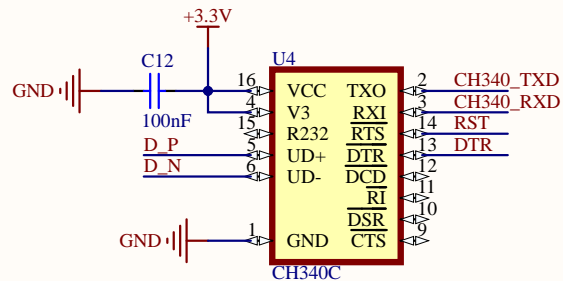
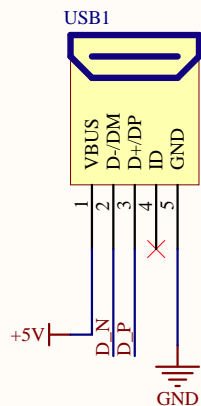
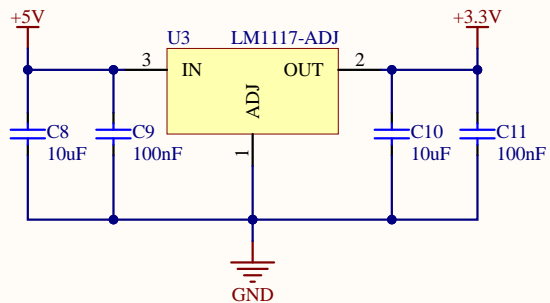
D



Title		
Size	Number	Revision
A		
Date:	4/05/2023	Sheet of
File:	D:\Final-Project\...\DW1000.SchDoc	Drawn By:

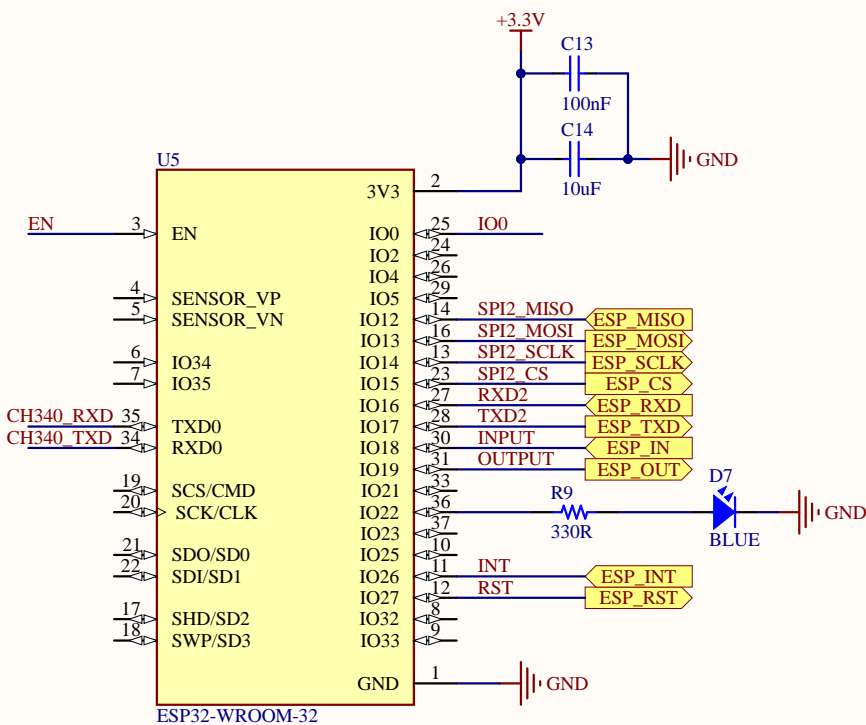
A

A



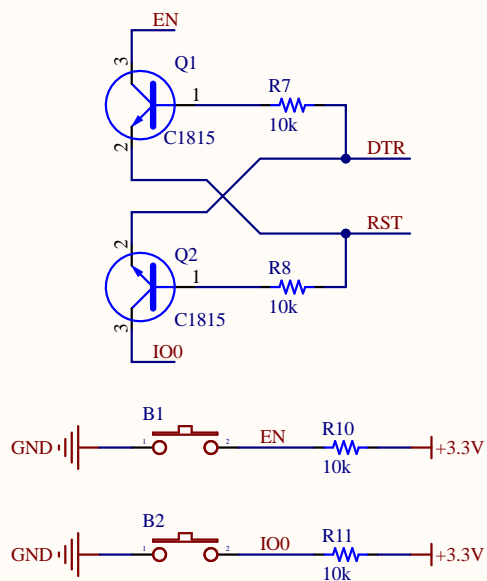
B

B



C

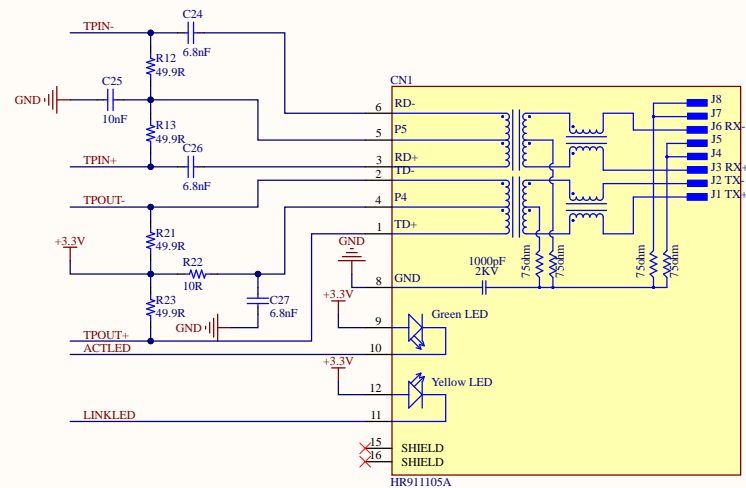
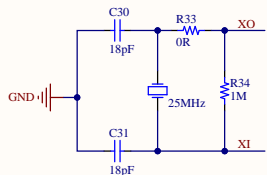
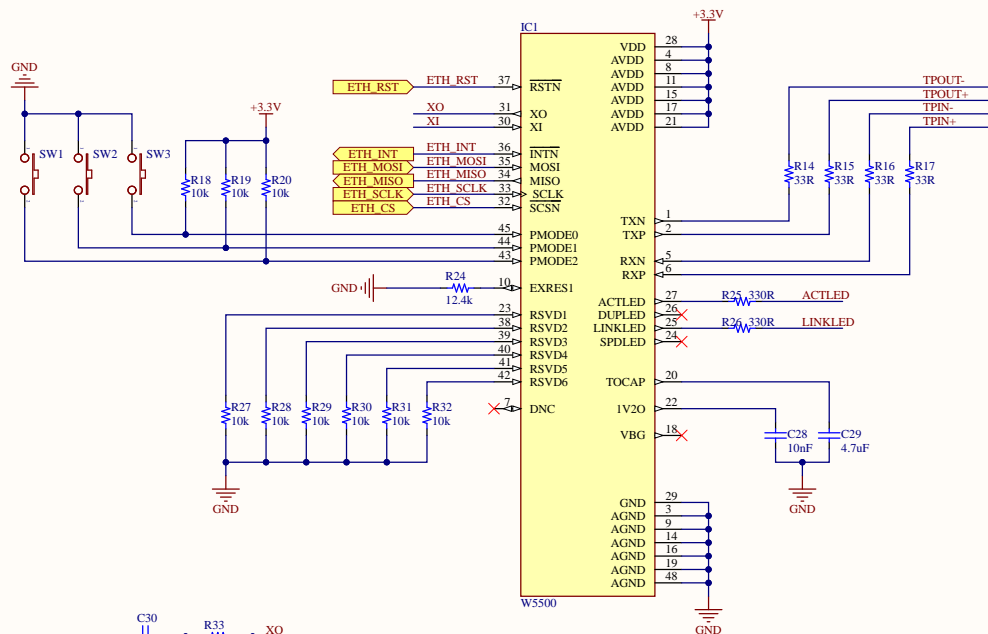
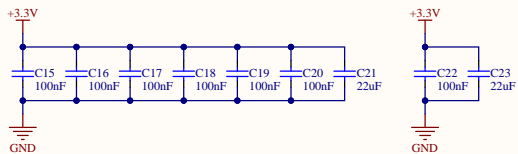
C



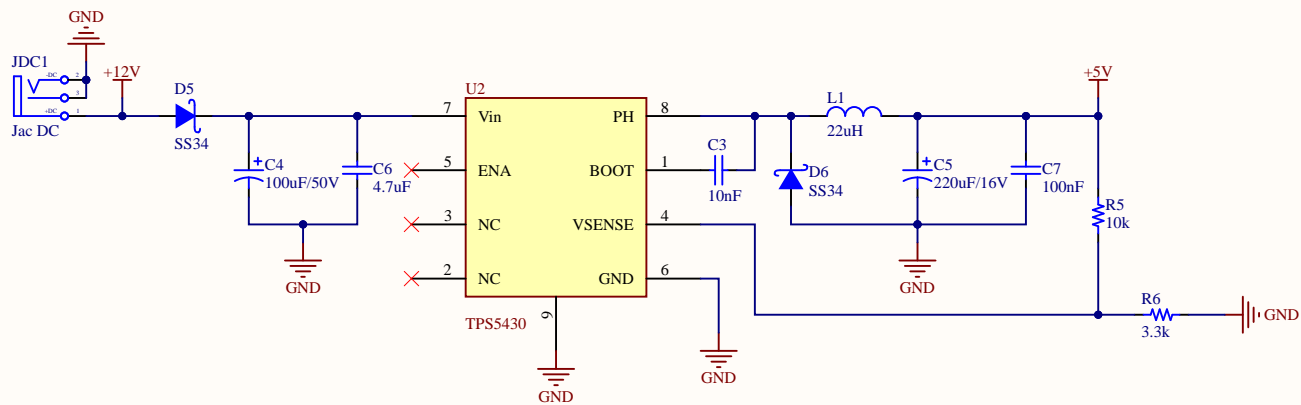
D

D

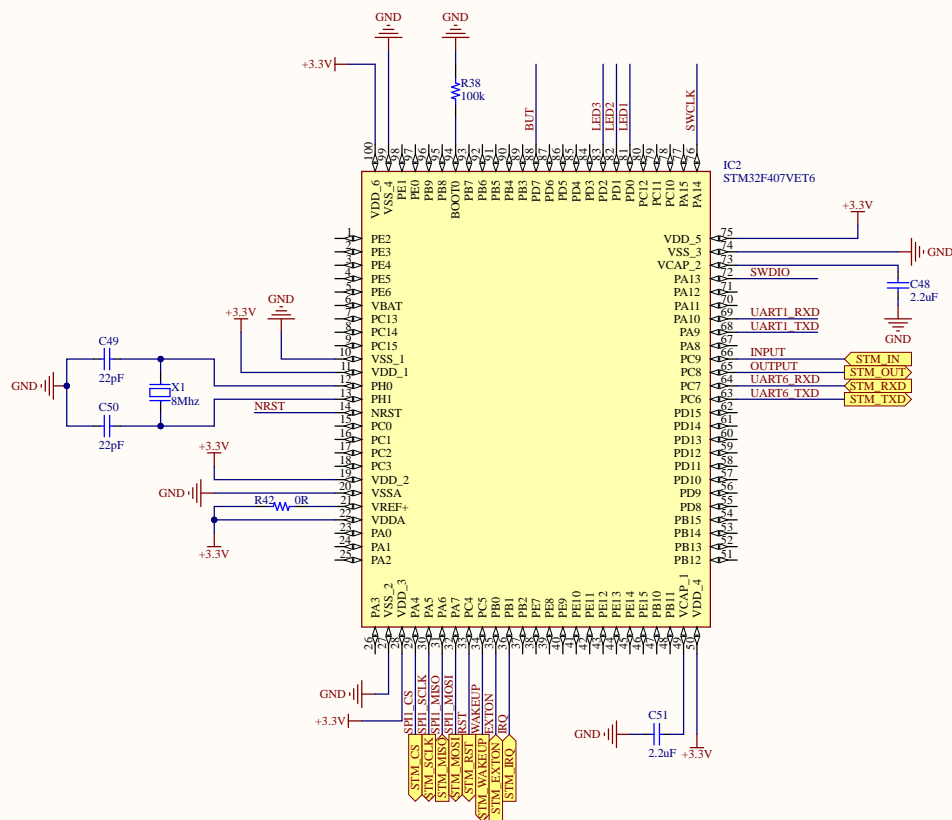
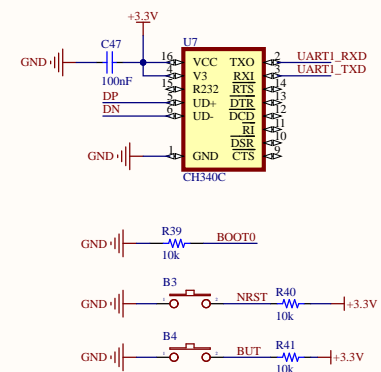
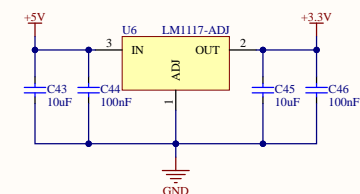
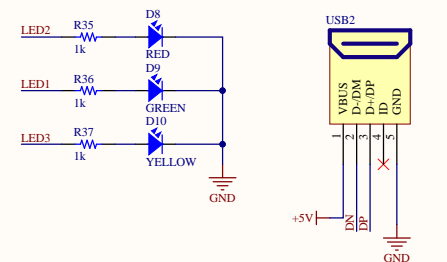
Title		
Size	Number	Revision
A		
Date:	4/05/2023	Sheet of
File:	D:\Final-Project\...\ESP32.SchDoc	Drawn By:



Title		
Size	Number	Revision
A3		
Date:	4/05/2023	Sheet of
File:	D:\Final-Project\ETHERNET.SchDoc	Drawn By:



Title		
Size A4	Number	Revision
Date:	4/05/2023	Sheet of
File:	D:\Final-Project\...\POWER.SchDoc	Drawn By:



Title		
Size A3	Number	Revision
Date:	4/05/2023	Sheet of
File:	D:\Final-Project\STM32_SchDoc	Drawn By: