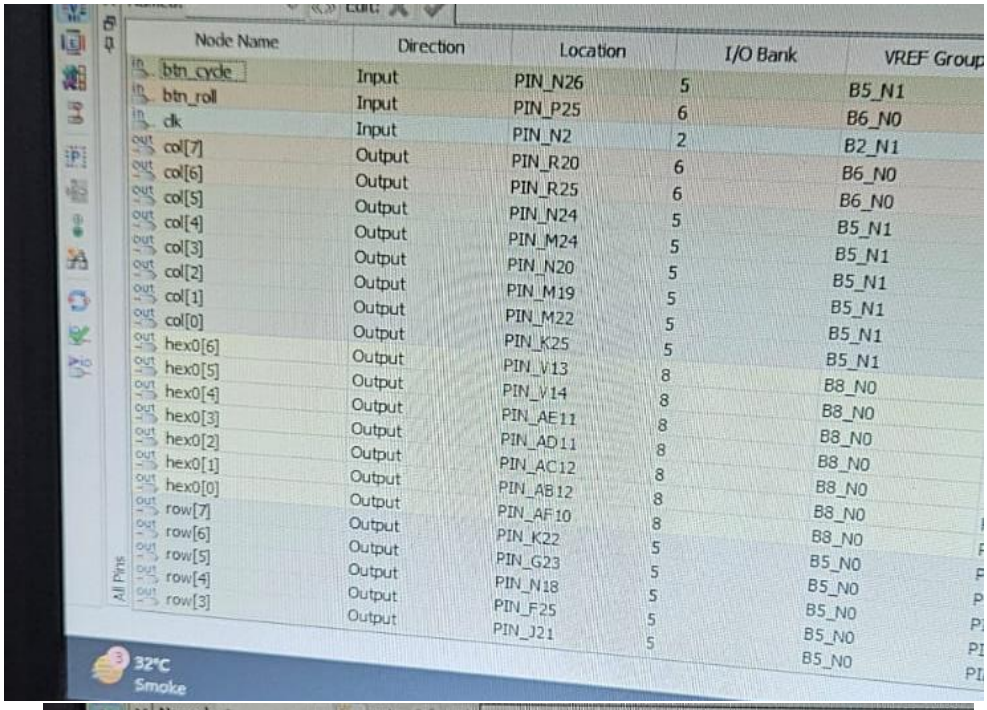
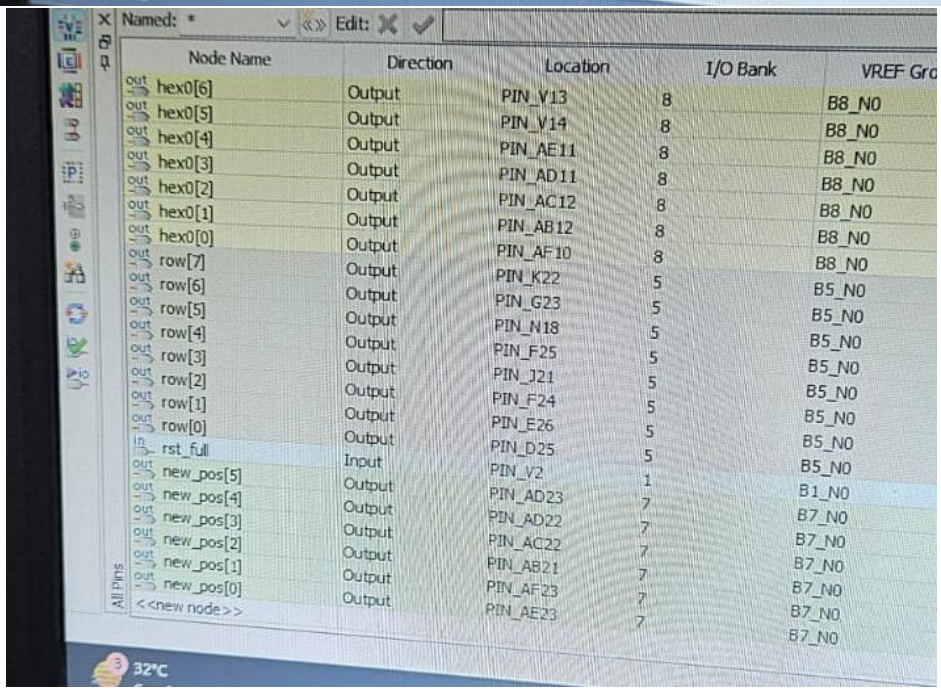
Images and Pin Assignments for Impelemtion in Altera IDE

Pin Assignment:



Node Name	Direction	Location	I/O Bank	VREF Group
btn_cycle	Input	PIN_N26	5	B5_N1
btn_roll	Input	PIN_P25	6	B6_N0
clk	Input	PIN_N2	2	B2_N1
col[7]	Output	PIN_R20	6	B6_N0
col[6]	Output	PIN_R25	6	B6_N0
col[5]	Output	PIN_N24	5	B5_N1
col[4]	Output	PIN_M24	5	B5_N1
col[3]	Output	PIN_N20	5	B5_N1
col[2]	Output	PIN_M19	5	B5_N1
col[1]	Output	PIN_M22	5	B5_N1
col[0]	Output	PIN_K25	5	B5_N1
hex0[6]	Output	PIN_V13	8	B8_N0
hex0[5]	Output	PIN_V14	8	B8_N0
hex0[4]	Output	PIN_AE11	8	B8_N0
hex0[3]	Output	PIN_AD11	8	B8_N0
hex0[2]	Output	PIN_AC12	8	B8_N0
hex0[1]	Output	PIN_AB12	8	B8_N0
hex0[0]	Output	PIN_AF10	8	B8_N0
row[7]	Output	PIN_K22	5	B5_N0
row[6]	Output	PIN_G23	5	B5_N0
row[5]	Output	PIN_N18	5	B5_N0
row[4]	Output	PIN_F25	5	B5_N0
row[3]	Output	PIN_J21	5	B5_N0



Node Name	Direction	Location	I/O Bank	VREF Gro
hex0[6]	Output	PIN_V13	8	B8_N0
hex0[5]	Output	PIN_V14	8	B8_N0
hex0[4]	Output	PIN_AE11	8	B8_N0
hex0[3]	Output	PIN_AD11	8	B8_N0
hex0[2]	Output	PIN_AC12	8	B8_N0
hex0[1]	Output	PIN_AB12	8	B8_N0
hex0[0]	Output	PIN_AF10	8	B8_N0
row[7]	Output	PIN_K22	5	B5_N0
row[6]	Output	PIN_G23	5	B5_N0
row[5]	Output	PIN_N18	5	B5_N0
row[4]	Output	PIN_F25	5	B5_N0
row[3]	Output	PIN_J21	5	B5_N0
row[2]	Output	PIN_F24	5	B5_N0
row[1]	Output	PIN_E26	5	B5_N0
row[0]	Output	PIN_D25	5	B5_N0
rst_full	Input	PIN_V2	1	B1_N0
new_pos[5]	Output	PIN_AD23	7	B7_N0
new_pos[4]	Output	PIN_AD22	7	B7_N0
new_pos[3]	Output	PIN_AC22	7	B7_N0
new_pos[2]	Output	PIN_AB21	7	B7_N0
new_pos[1]	Output	PIN_AF23	7	B7_N0
new_pos[0]	Output	PIN_AE23	7	B7_N0

Images: