

Sessional Test I—February, 2023

Semester II

ID No:

Total No. of Pages: 02

Time: 90 minutes

Max. Marks: 40

Title of the Course: Computer System Architecture

Course Code: CS118

Instructions:

For Section A

- There is one question having five parts. Each part is having four distinct options out of which only one choice will be correct.
- There is no negative marking for incorrect answers.

For Section B

- There are 6 Questions of 2 marks each. There is a choice to attempt 5 questions out of 6.

For Section C

- There are 4 Questions of 5 marks each. There is a choice to attempt 3 questions out of 4.

For Section D

- There are 2 Questions of 10 marks each. There is a choice to attempt 1 question out of 2.

Section-A

(All Questions are Compulsory, Each question carries 01 mark)

1.

a) The use of which of the following components marked the starting of second-generation computer?

- | | |
|-------------------|--------------------------|
| (i) Vacuum tubes | (ii) Microprocessors |
| (iii) Transistors | (iv) Integrated circuits |

b) Register reference instruction format contain _____ in 12 to 15 bit

- | | |
|------------|-----------|
| (i) 1111 | (ii) 1100 |
| (iii) 0011 | (iv) 0111 |

c) Which of the following are Universal gates?

- | | |
|------------------|-----------------|
| (i) OR & NAND | (ii) NOT & NOR |
| (iii) NAND & NOT | (iv) NOR & NAND |

d) An Instruction cycle refers to which one of the following?

- | | |
|--|-------------------------------|
| (i) Fetching an instruction | (ii) Clock cycle time |
| Fetching, decoding and executing an instruction. | |
| (iii) | (iv) Executing an instruction |

e) The Von Neumann bottleneck can be attributed to which one of the following?

- | | |
|---|---|
| (i) Mismatch between the speeds of the secondary and the primary storages | (ii) Mismatch between the speeds of the CPU and the primary storage |
| (iii) Slow speed of input/output devices | (iv) Low clock speedss |

Section-B

(Attempt any 5 questions, each question carries 02 marks)

2. Draw the timing diagram for following instruction assuming that SC is cleared to 0(zero) at time T_3 if control signal D_7 is active.

$$D_7 T_3: SC \leftarrow 0$$

3. There are few differences which makes combinational circuits different from Sequential circuits. Write at least 4 of them.
4. Distinguish between direct addressing and indirect addressing. Show it with the help of an example.
5. A memory unit has a size of 1024×8 bits.
- Find the size of Address bus
 - Find the size of Data bus
6. Do the following conversions.
- Convert $(670.02)_{10}$ in binary
 - Convert $(9AB.60)_{16}$ in binary
7. Write the use of the following instructions.
- ADD
 - ISZ
 - CME
 - INP

Section-C

(Attempt any 3 questions, each question carries 5 marks, subparts (if any) carry equal weightage)

8. A 4-bit SISO Shift Register has 1110 as its initial data which is already stored inside each of its flip flop while 1010 is to be serially entered inside the same. What will be the status of SISO after 3rd clock pulse. Also draw the logic diagram of 4-bit SISO using D flip flops.
9. Draw the logic diagram of J-K Flip flop. Also write its truth table showing the obtained state with the help of Present ad Next States of the Flip flop.
10. Identify the following Register symbols and also write about their use.
- AR
 - DR
 - IR
 - AC
11. Show and explain the instruction code formats for the basic computer. Identify the following instruction category.
- 0111101010011011
 - 0101110101010001

Section-D

(Attempt any one question, each question carries 10 marks, subparts (if any) carry equal weightage)

12. Earlier Program was executed with an operator setting up each instruction and also initiating the execution of each instruction. But later the John Von Neumann proposed an Architecture. Draw the Organization of Von-Neumann Computer. Explain all the major components of it and also explain what makes Von Neumann Architecture different from earlier program execution.
13. The basic computer has eight registers, a memory unit and a control unit. Show the diagram representing the paths to transfer the information from one register to another and between memory and registers. Also show the specific output that is selected for the bus lines at any given time which is determined by the binary value of the selection variables S_2, S_1 and S_0 . Explain in brief about the same.

Q1 (a) (iii) Transistor Section - A

Feb 12023

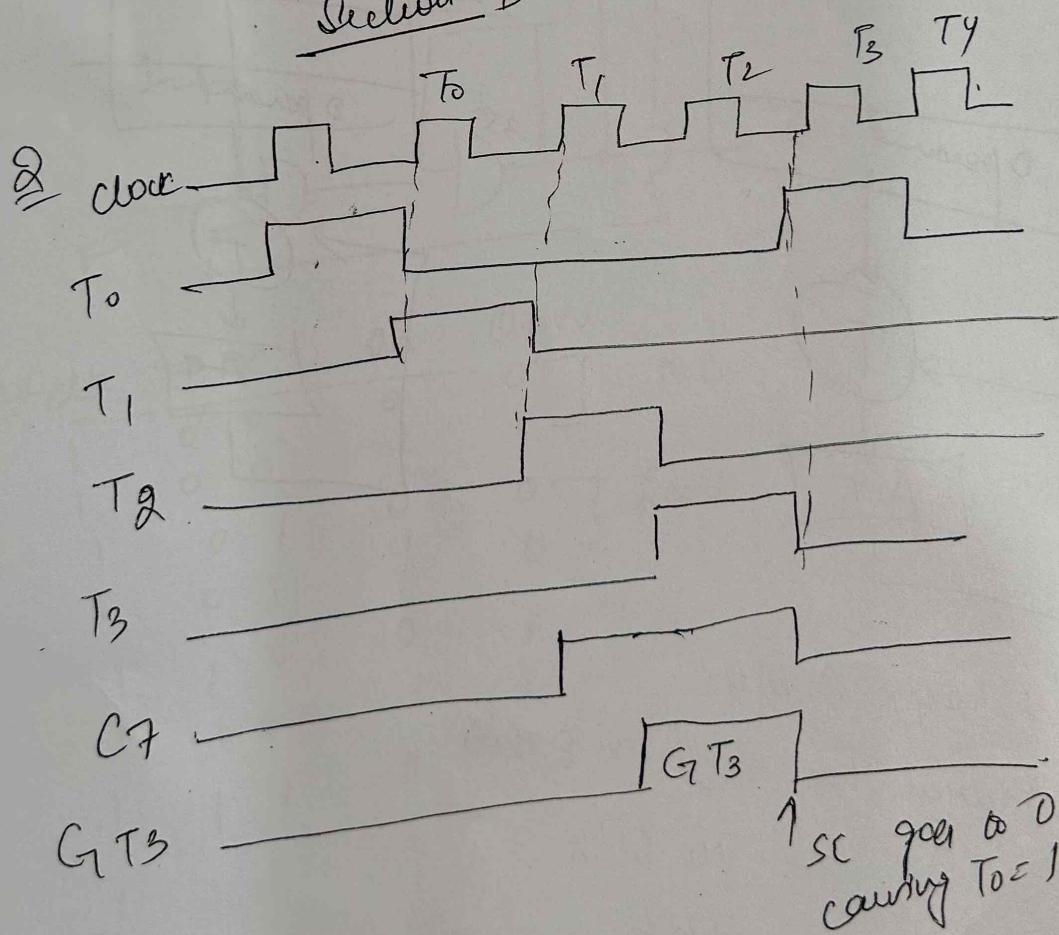
(b) (iv) 0111

(c) (v) NOR & NAND

(d) (iii) fetching, decoding and executing

(e) (ii) Mismatch b/w the speeds of the CPU & the primary storage

Section - B



3

Combinational

Output depends only on
the present IIP

fast in operation

No memory elements

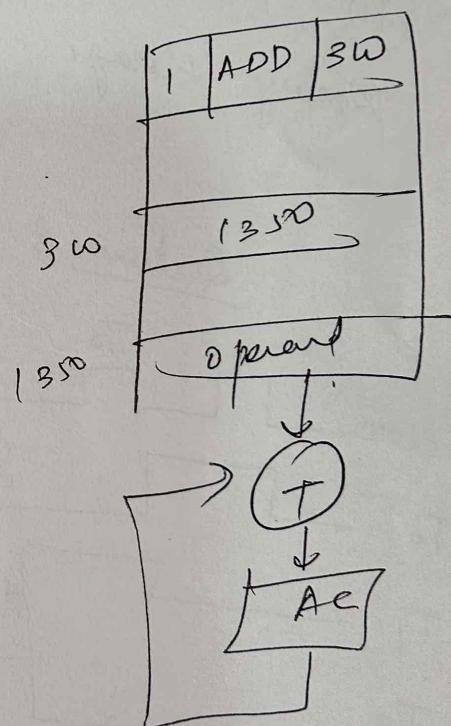
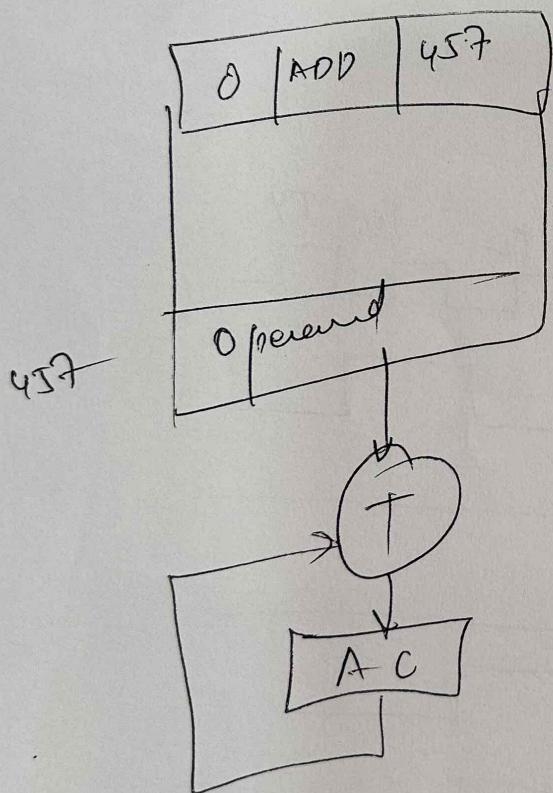
Sequential

Output depends only on
present as well as past IIP

Slow as compared to combinational
Memory element is present

4

Unit



5

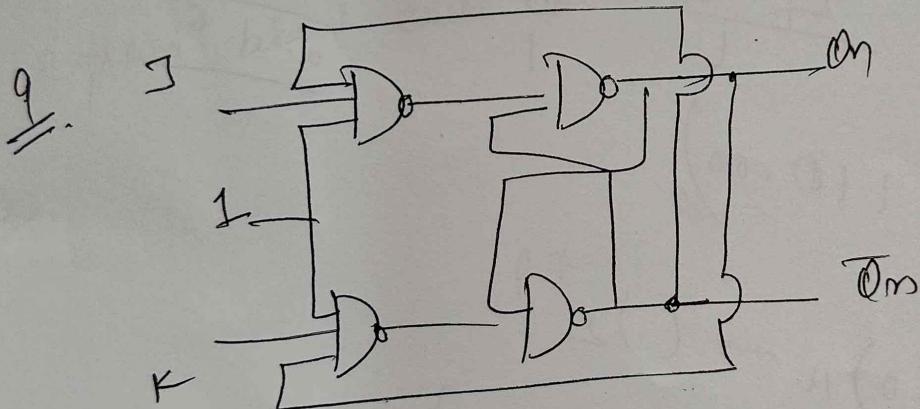
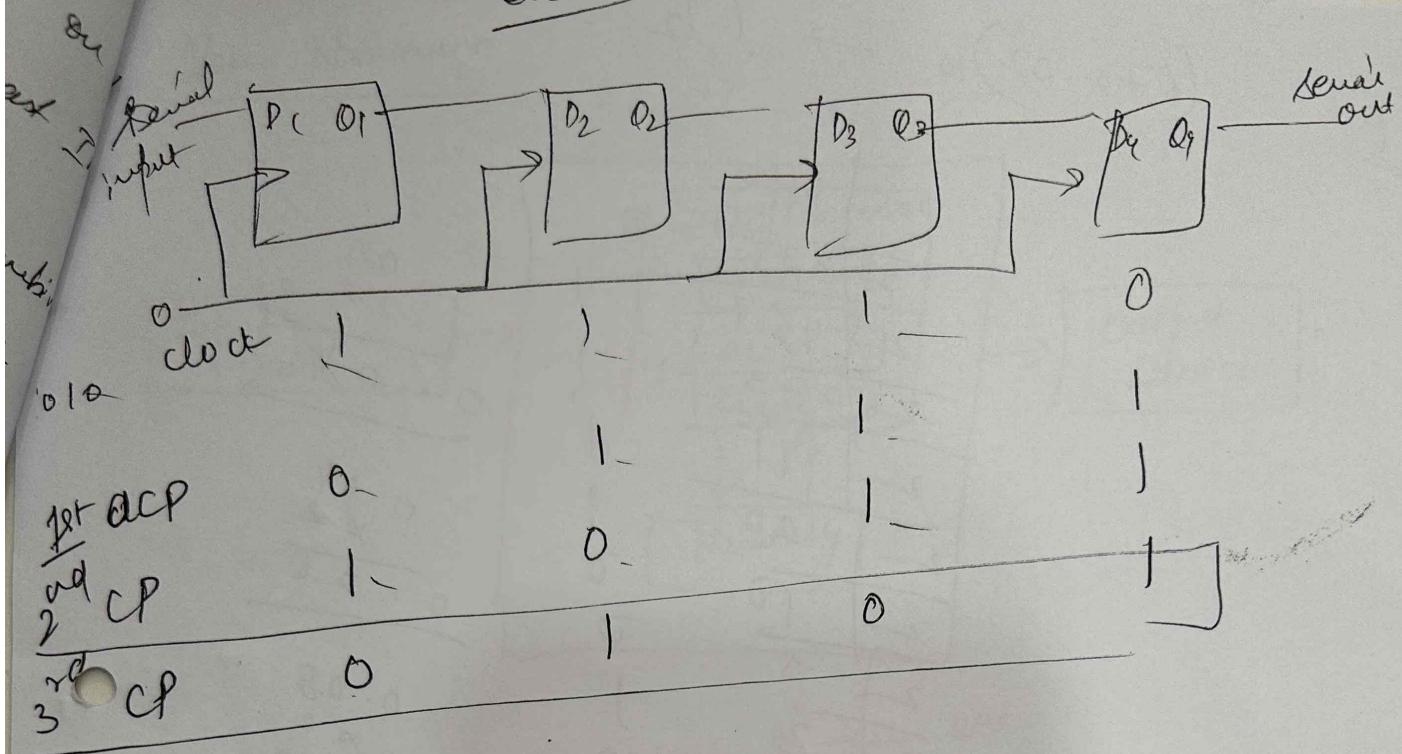
$1024 \times 8 \text{ bits}$

Address bus $2^{10} \times 8 \text{ bits}$

= 10 bits

Data bus = 8 bits

See - C



Cycle	K	Q _n	Q _{n+1}	NC
1	0 0	0 ;	0 ;	
1	0 0	0 ;	0 ;	Reset
1	0 1	0 ;	0 ;	
1	0 1	0 ;	0 ;	
1	1 0	0 ;	1 ;	Set
1	1 0	0 ;	1 ;	
1	1 1	0 ;	0 ;	Toggle
1	1 1	1 ;	0 ;	

f

$$(670.02)_{10} \rightarrow (?)_2$$

Von-

$$\begin{array}{r}
 670 \\
 \hline
 2 | 335 \\
 2 | 167 \\
 2 | 83 \\
 2 | 41 \\
 2 | 20 \\
 2 | 10 \\
 2 | 8 \\
 2 | 2 \\
 \hline
 1 & 0 & 1 & 0 & 0 & 1 & 1 & 1
 \end{array}$$

$$\begin{array}{r}
 0.02 \\
 \times 2 \\
 \hline
 0.04
 \end{array}$$

$$\begin{array}{r}
 0.09 \\
 \times 2 \\
 \hline
 0.08
 \end{array}$$

$$\begin{array}{r}
 0.08 \\
 \times 2 \\
 \hline
 0.16
 \end{array}$$

$$\begin{array}{r}
 10100111(10.00)_2
 \end{array}$$

(b) $(9AB.60)_{16} \rightarrow (?)_2$

$$\begin{array}{r}
 100110101011.01100000_2
 \end{array}$$

7

ADD - Add memory word to AC
Increment & skip if zero

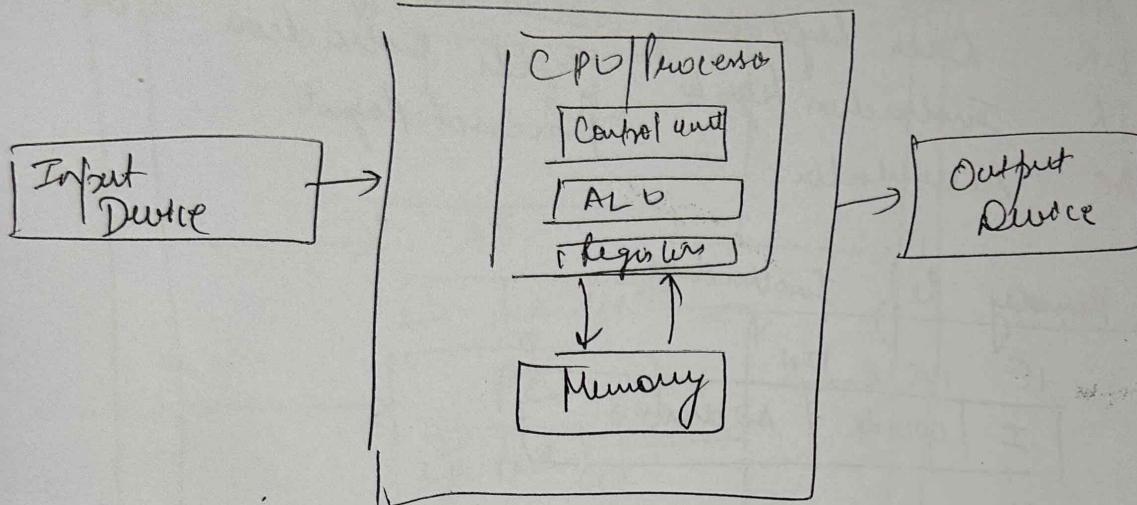
ISZ

CME

INP

Complement F
Input character to AC

Von-Neumann

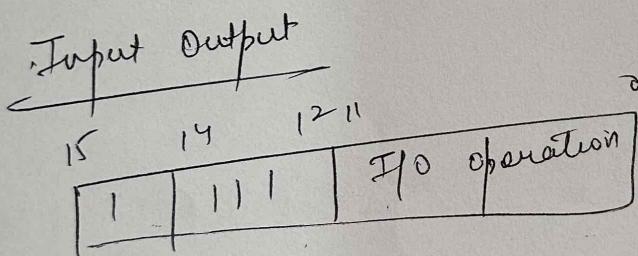
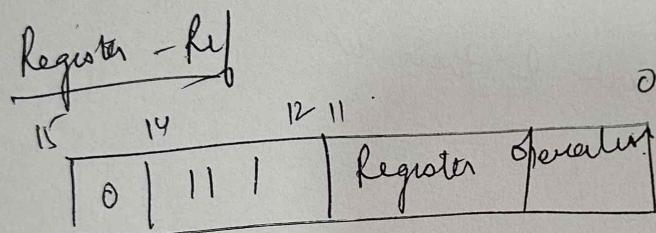
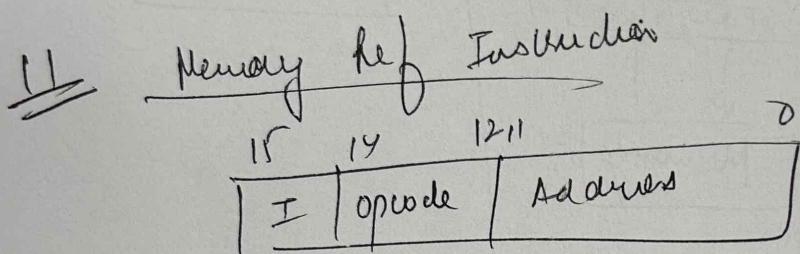


explain about each block & their use

13

P.T.O

10.	AR	Addreses Register	holds address for memory
	DR	Data Register	holds memory operand
	IR	Instruction Register	holds instruction code
	AC	Accumulator	processor register



(a) Register Reference Instruction

(b) Memory " "

