Mixed Signal Design of 8 Bit SRAM Implemented using eSIM and NgVeri

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Abstract **– The scope of this work is to present a 8-Bit Static Random Access Memory(SRAM) implemented in the Mixed Signal domain using eSim and NgVeri. Here static signifies that the memory will be retained only as long as the RAM is connected to supply. And random access means that we can read/write data from memory irrespective of which sequence the data is present in i.e it will take the same time to access/modify the data irrespective of the bit position. The main advantages of using SRAM is the high switching speed and low power consumption. The applications of this circuit can be a simple memory element, a Lookup table for an FPGA etc.**

Keywords **– 6T MEMORY CELL, STATIC RAM**

I. INTRODUCTION

In modern day computing, the memory elements play a very important role in storing large amounts of data. We all know that SRAM is much faster than DRAM (Dynamic RAM), so to utilise SRAM to the fullest we have the concept of caching the memory i.e we save the data in SRAMs on first load so that in the consecutive load time reduces drastically. This is majorly used in server based web applications because the servers are usually switched on all the time. The use of this SRAM is expected to grow further so we are going to design a 8-Bit SRAM based cache memory which is mainly used due to its High performance and Low power in comparison with the DRAM.
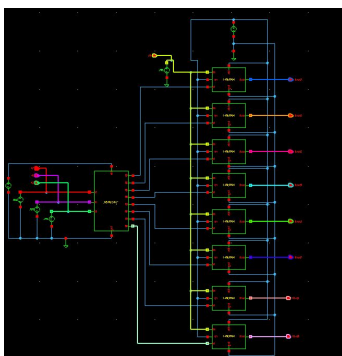

Fig. 1. 8-Bit SRAM Schematic

II. 1-BIT RAM CELL

As shown in the above figure we will have an array of 1-Bit RAM cells and the RAM cell whose bit value needs to be modified is selected through decoder circuit. The decoder circuit will be implemented in the digital domain using NgVeri and the 1-Bit RAM cell will be implemented in analog domain using eSim at transistor level. Each of the 1-Bit RAM cell will have a writer circuit, a 6T RAM cell and a sensory circuit.
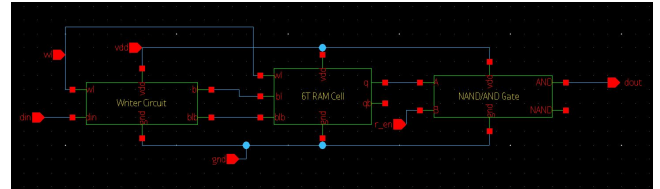

Fig. 2. 1-Bit RAM Schematic

III. 6T RAM CELL

6T SRAM is a type of transistor based memory element that uses bi-stable latching circuitry to store a single bit. As shown in the schematic when the Write Line is 1 the MOSFETs are switched on so that the value in the Bit Lines is transferred to opposite sides of the inverter network overriding the already present value. And when the MOSFETs are cut-off the value in the inverter network holds until the inverter network has power supply.
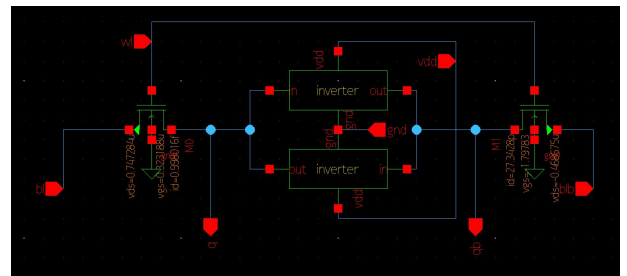

Fig. 3. 6T RAM cell Schematic

IV. Transient Analysis of the Circuit

Fig. 4. Transient Analysis of 8-Bit RAM

References

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