Four Quadrant Analog Multiplier using CMOS in 28nm technology

VANSHIKA TANWAR, Electronics and Communication Engineering,
Dronacharya Group of Institutions, Greater Noida

Abstract— **Multiplication of two analog input signals is one of the most important factors which we need while working or performing operations in Analog Signal Processing. As, the multiplier is such type of a basic circuit that is used as a subcircuit in many of the other circuits, for example, it is used in analog computers, analog signal processing, etc. Up to now there are so many analog multipliers are designed with the reduction of power supply voltages, there are many CMOS existing analog multipliers are designed but they are generally designed to be operated at higher supply voltages, which are unfortunately not suitable to be applied to battery-powered systems such as portable communications systems equipment, some radio receivers, etc.**

Therefore, in this paper, we are going to design a Low power consumption CMOS Analog Multiplier. The technique which we are going to use to make this design is a four-quadrant technique. We are going to design CMOS Analog multiplier using 28nm technology. Design and Implementation of this circuit will be done in Synopsys Custom design platform tool that is Synopsys custom design compiler tool.

Keywords—- Multiplier, Synopsys tool,28nm

I. INTRODUCTION

An analog multiplier is basically a non-linear circuit. It is a device that contains two analog input signal and gives the product of both the input signal in its output. It is a circuit that basically gives the linear product of two continuous input signals in its output. If both the input and output signals are voltages let us say "V1" and "V2" be the input signal then in the output let's say "Vout" it gives the product of both the input voltages divided by a scaling factor (say k). where k is the scaling factor that is any multiplication constant or a gain of suitable dimension.

$$Vout= (V1*V2)/k$$
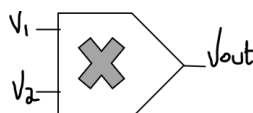
It is used widely in the field of telecommunication, analog signal processing, Instrument systems etc. Analog multiplier is categorized as single quadrant which means that when both the input is positive/negative (i.e., same unipolar), two-quadrant means when one input has a positive voltage and other input could have positive or negative voltage (i.e., x is bipolar and y is unipolar), four-quadrant multiplier means when both the input is either positive or negative (i.e., when x is bipolar and y is also bipolar).

So, in this paper, we are going to make the CMOS low power consumption four-quadrant analog multiplier. As, four-quadrant analog multiplier is a very useful basic building block in many circuits like adaptive filters, phase-frequency detection, frequency double, function generator, frequency shifters, etc. It is also used in modulation, pll (phase-locked loop), frequency mixer, frequency doubler, etc.
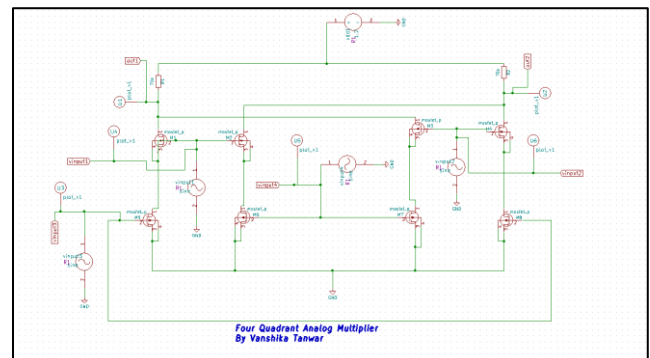
II. REFRENCE CIRCUIT DETAILE

The main purpose of designing a four-quadrant analog multiplier is to eliminate extra voltage reference to make a compact circuit design. By implementing and simulating this circuit in Synopsys Custom compiler tool using CMOS 28nm Technology, the device performance, density and low power consumption will be improved and achieved. The proposed design consists of a pair of common source amplifier with input transistors and the output that it gives is the square function of its input voltages v1 and v2. It contains a total of 8 transistors in which all 8 are PMOS including two resistors R1 and R2 to make the transistor to work in the proper region and the value of resistors has to be taken accordingly at the time of the simulation. Transistor m1 to m8 acts as a non-linear cancellation path in a square root circuit. The output which comes from transistors are directly going into the square root circuit block to produce differential output voltage or current which is just the product of the input signal v12 and v34. Here, v12 is the difference between v1 and v2 signal while v34 is the difference between v3 and v4 input signal and the resultant output signal Vout will be the differential output of vout1 and vout2.

Hence, on observing the output waveform we conclude that the given circuit become capable to operate with the input voltage and also the requirement of low power consumption for operating the circuit is also achieved. So, a new square root circuit can be used to realize a CMOS four-quadrant analog multiplier has been given. For the verification purpose of the multiplier circuit, a performance simulation result has been given.

III. REFERENCE CIRCUIT DESIGN

Four Quadrant Analog Multiplier
By Vanshika Tanwar

V. REFERENCE CIRCUIT WAVEFORMS

V. REFERENCE PAPE/JOURNALS

1. https://www.ijaiem.org/volume2issue7/IJAIEM-2013-07-16-049.pdf
2. https://aircconline.com/vlsics/V3N5/3512vlsics08.pdf
3.https://www.researchgate.net/publication/261076064_CMOS_Design_of_a_Multi-input_Analog_Multiplier_and_Divider_Circuit