Experience in Using the OpenROAD Flow Scripts tool with ASAP7 Technology by designing the 4-stage RISC V Core Design

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***Abstract*— In this paper, we are going to implement the 4-stage RISC-V core processor and also going to share our experience of using the OpenROAD Flow Scripts (ORFS) tool. In short, it is also known as the ORFS tool. Basically, ORFS is an open-source tool used for generating RTL to GDS Flow of any specific design.**

Keywords*— *Open ROAD Flow Scripts, RTL-to-GDSII flow, open-source tools, automated design, no-human-in-the-loop, riscv, Verilog code.

I. INTRODUCTION

OpenROAD Flow Scripts tool is used to generate the RTL to GDS for any digital circuit design, it uses the automated flow without the use of any inhuman in between the generation of tool flow. In this paper, we are going to describe the ORFS on a RISC V core processor design and also going to outline the benefits of different challenges which will be faced at the time of implementing this design.

Also, the experience in using the ORFS tool is pretty much good as it reduces all time and effort which is used for generating the complex or bigger digital design as this tool provides the automatic way for generating the RTL to GDSII for any easy or complex digital design.

II. DESIGN FLOW OVERVIEW

The overall flow for designing the 4-stage RISC architecture is very easy as it only needs the Verilog code for generating the digital design layout also, we have faced some issues and some challenges are faced while designing this RISC-V core processor. And, also in this paper, we are also going to focus reduce the design complexity and its simulation run time, and other parameters by doing changes in it's files, scripts or code, etc. But, by designing some of the basic existing RISC-V processors the overall experience is great and it takes less time in a generation the digital layout of any circuit design.

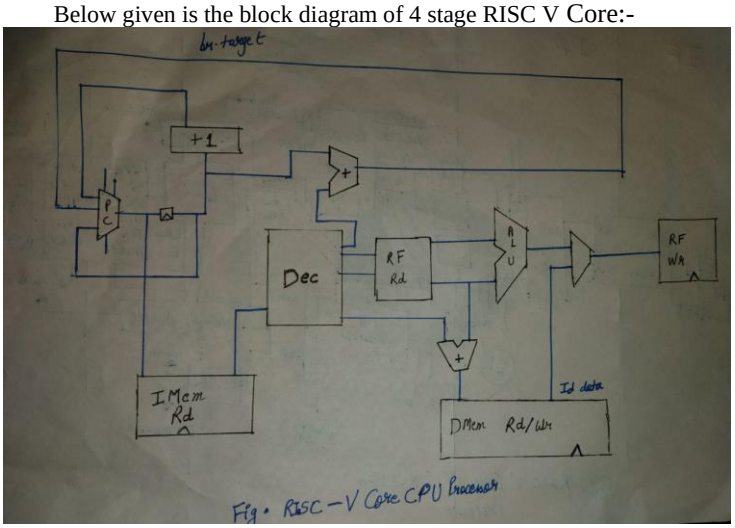
As I have designed the ibex processor using this tool so, I found the tool very much easy to use and pretty much good as first of all this tool is available for free of cost because it's an opensource tool and also this tool provides flexibility for meeting the particular design specs. And it takes less time in generating flow. But, yes as this tool generates the layout without any human intervention but it also leads to unexpected results of the final design layout so, the whole tool and the implementation of the design need to be analyzed carefully and it also needs to debug the error.

III. Experience of ORFS and Block Diagram of 4 Stage RISCV Core USING ORFS

My experience of using ORFS is pretty much good as it generates the flow in a very much less time without any human interruption in between hence, it saves time and effort for designing complex designs. Also, this provides flexibility in designing any easy to complex digital design with their particular specification. It sometimes generates the unexpected final result of our design layout so, it needs to be debugged for the error also, any new designer on this tool needs to first know about design methodologies so, there one can face the problem of first understanding and analyzing the tool.

As we are going to implement the 4-stage RISC V core Processor using ORFS Tool which is an open-source tool. 4 Stage RISC V Core processor consists of several blocks ALU, RF, DMem Rd/write, RF Wr, De (Decode), PC(program Counter), IMem Rd. We are going to design the layout using the ORFS tool using the ASAP7 technology node

Below given is the block diagram of 4 stage RISC V Core:-



IV. CONCLUSIONS AND RECOMMENDATIONS

In conclusion, Finally we are going to design the 4-stage RISCV Core Processor using this ORFS Tool using ASAP7 Technology As, this tool is going to simplify the design of use of opensource tool without any human interruption in between the generation of RTL to GDS Flow So, this tool needs to analyze carefully and all it's functioning and parameters for getting the final design result of our respected design. Hence the overall experience in using this tool is great.

We are going to recommend the use of the ORFS tool for designing any digital circuit and for generating the RTL to GDS flow for any of you designs as this tool is free of cost and it is generating the flow without any human intervention.

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