ED214:Electronics Design lab
8 Bit Computer

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8 Bit Computer Clock

-> Different modes of an 8 bit clock:

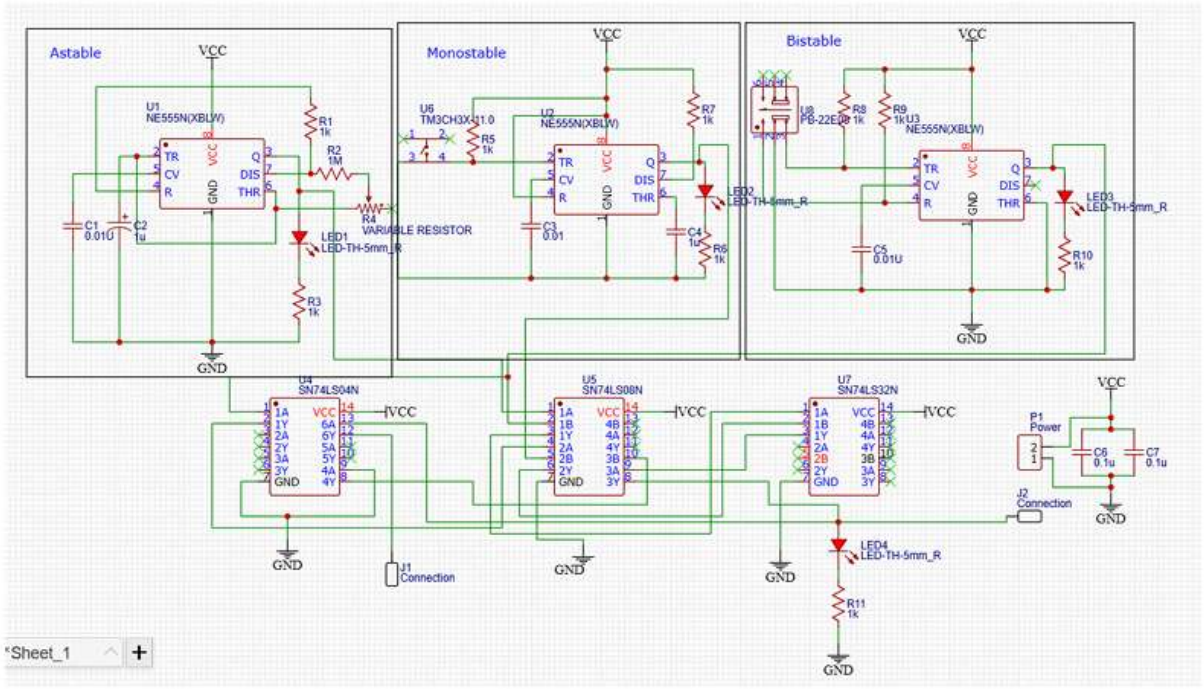
1. Astable: In astable mode, the circuit continuously switches between high and low states. If we observe the output in an oscilloscope then it will give us a square wave output of a series of high and low pulses.

2. Monostable: In monostable mode, the circuit has only one stable state when we push the switch then it will be in its unstable mode until the button is pushed.

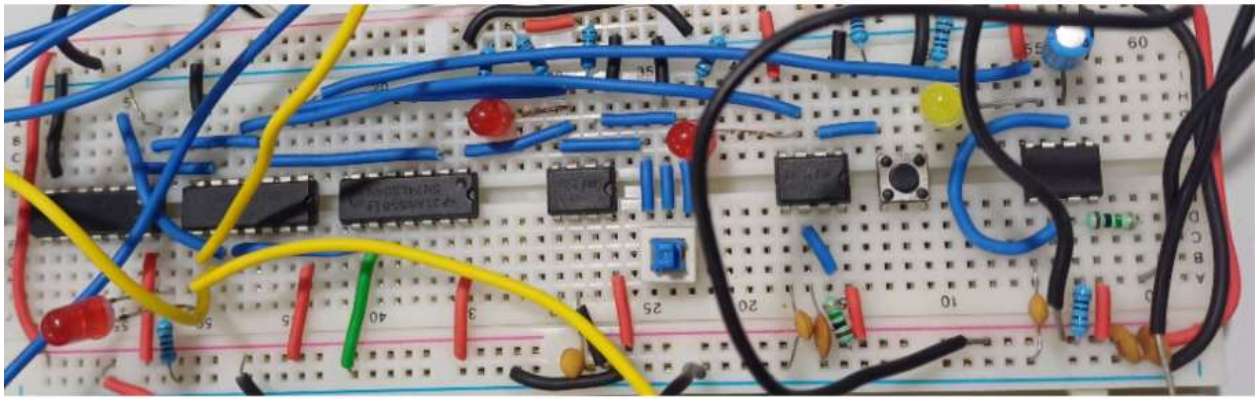
3. Bistable: In bistable mode, the circuit has two stable states, high and low, and it stays in one previous state until triggered to switch to the other.

Tool: Easy EDA

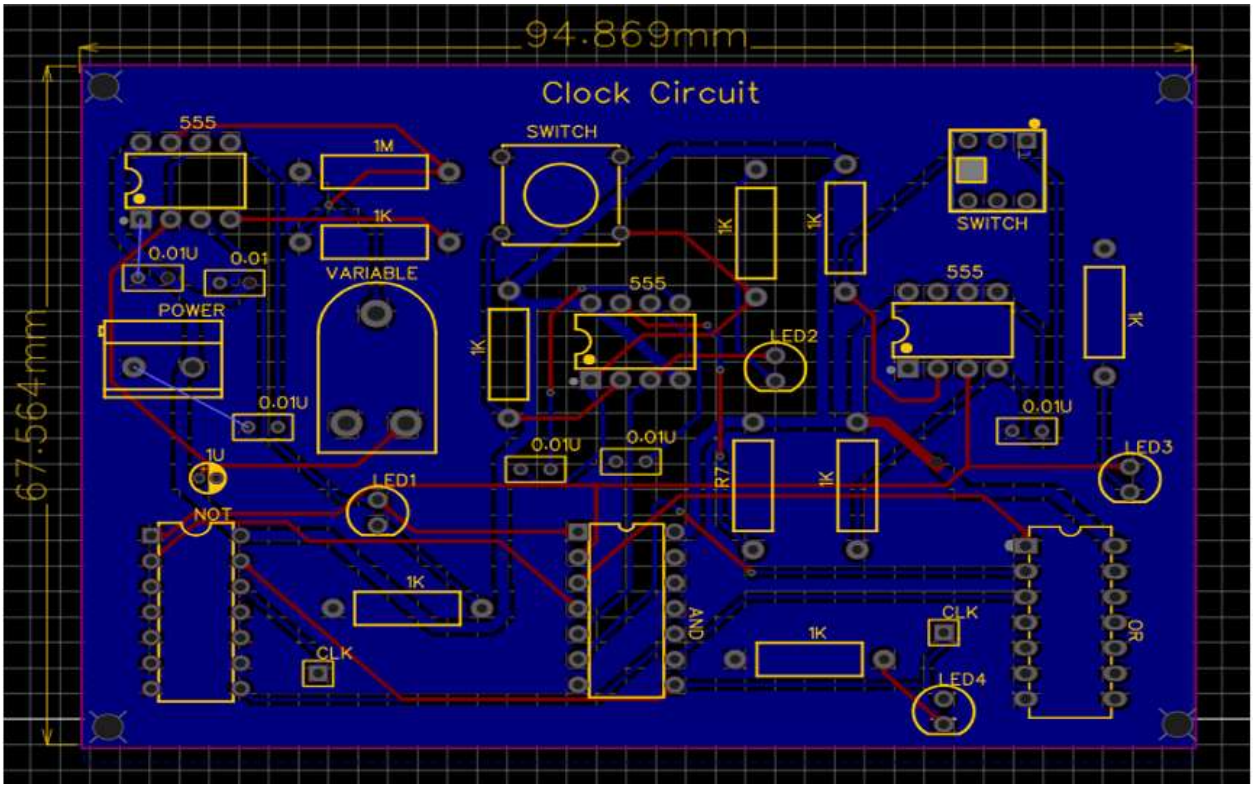
Circuit-Diagram(Schematic):-


Astable
Monostable
Bistable
VCC
GND
U1
NE555N(XBLW)
R1
1k
R2
1M
R4
VARIABLE RESISTOR
C1
0.01U
C2
1u
R3
1k
LED1
LED-TH-5mm_R
U6
TM3CH3X-11.0
R5
1k
U2
NE555N(XBLW)
R7
1k
C3
0.01
C4
1u
R6
1k
LED2
LED-TH-5mm_R
U8
PB-22E08
R8
1k
R9
1k
U3
NE555N(XBLW)
C5
0.01U
R10
1k
LED3
LED-TH-5mm_R
U4
SN74LS04N
U5
SN74LS08N
U7
SN74LS32N
P1
Power
C6
0.1u
C7
0.1u
J2
Connection
J1
Connection
LED4
LED-TH-5mm_R
R11
1k
Sheet_1

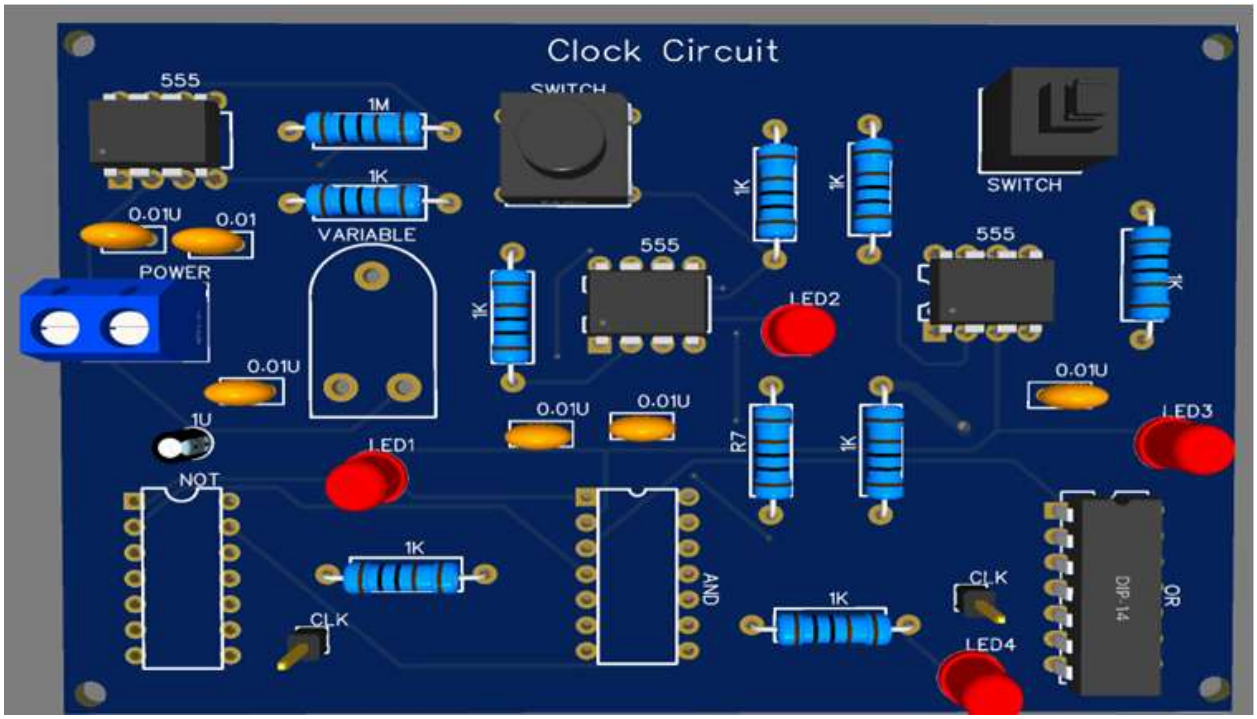
Bread-Board:-



PCB-Layout (2-Layer):-



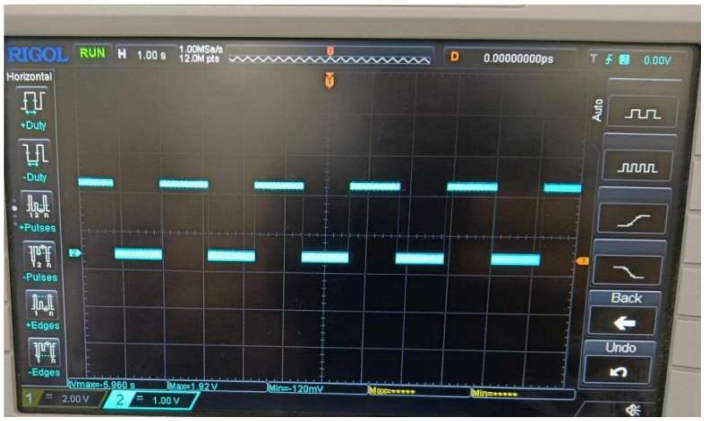
3-D:-



- HLT-Switch:-

  →The **HLT (Halt) switch** is used to **pause or stop the clock signal** in a controlled manner.
  →When activated, the clock signal is disabled, effectively freezing the operation of the computer. This is especially useful in debugging or testing situations.

Oscilloscope-output:-



IC's:

1) **NE555(555-Timer)**

Connections for Astable

Pin 1:Ground

Pin 2:Trigger

Pin 3:Output

Pin 4:Reset

Pin 5:Control

Pin 6:Threshold

Pin 7:Discharge

Pin 8:Vcc

In **Astable mode**, the 555 timer creates a continuous oscillation by charging and discharging a capacitor through resistors (R1 and R2). The connections are specifically designed to:

1. **Enable Feedback Loop**
2. **Control Timing**
3. **Ensure Stability**
4. **Provide Continuous Oscillation**:

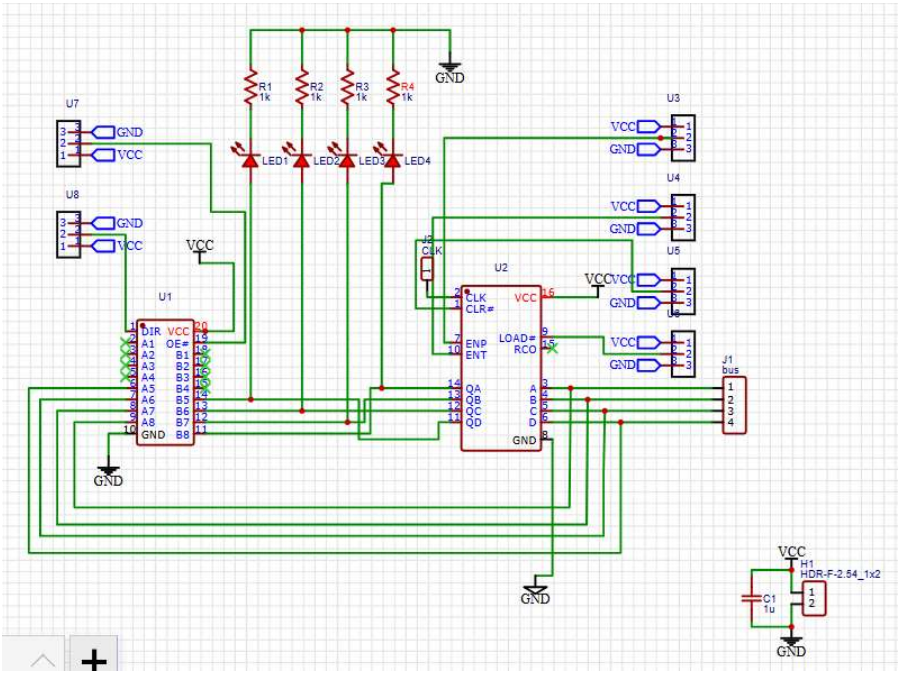
2)74LS08N(AND gate)

3) 74LS04N(NOT gate)

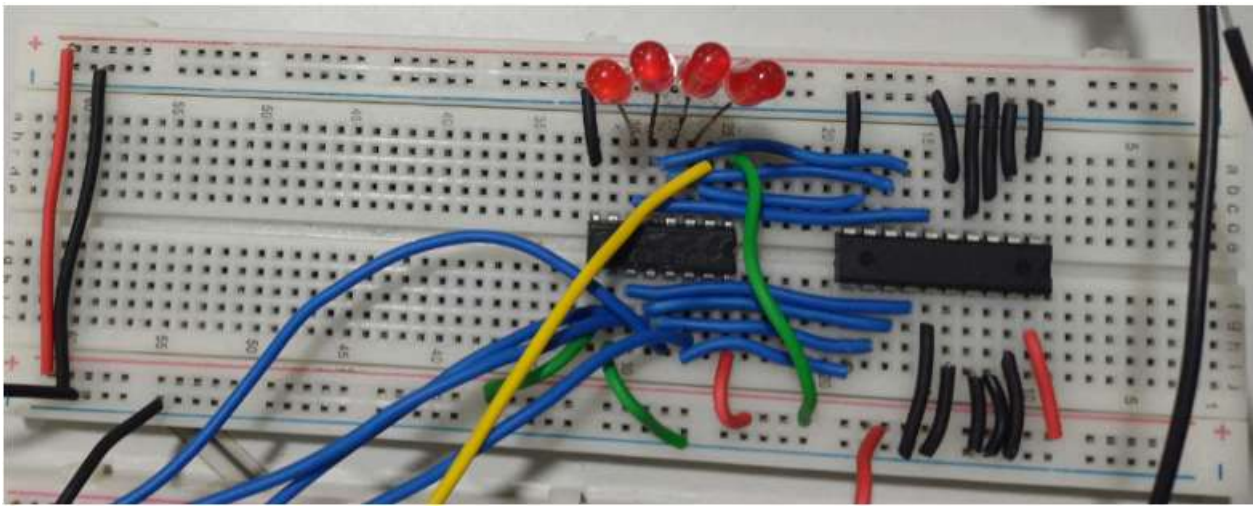
4) 74LS32N(OR gate)

B) 4-bit program counter:

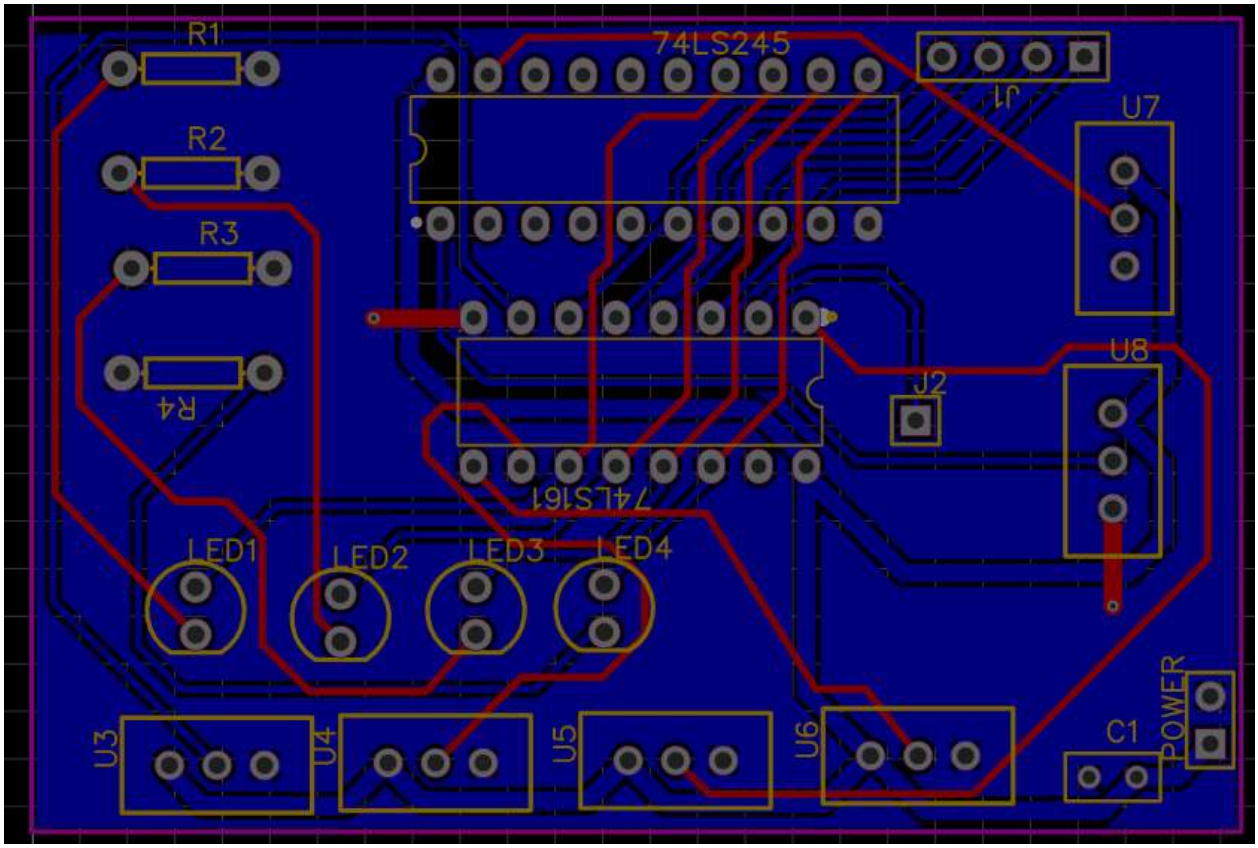
Circuit-Diagram(Schematic):-



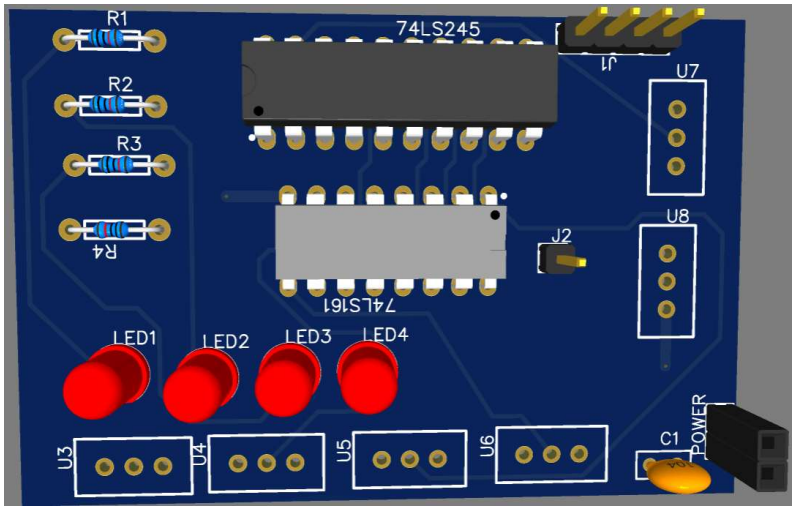
Bread Board:-



PCB-Layout (2-Layer):-



3D:-



- ICs:-

1) 74LS161(Program-Counter):-

- Purpose to include in 8-Bit Computer:-

→**Timing and control purposes**, such as sequencing operations and addressing memory.
→It generates binary counts (0–15).

- Why Synchronization?:-

Feature	Synchronous Counter (e.g., 74LS161)	Asynchronous Counter
Clocking	All flip-flops are clocked simultaneously.	Flip-flops are clocked sequentially (output of one triggers the next).
Propagation Delay	Minimal, as all stages update at the same time.	Accumulates as the signal propagates through stages.
Speed	Faster and suitable for high-speed applications.	Slower due to ripple delays.
Glitches/Errors	Less prone to glitches or timing errors.	More prone to glitches due to delayed transitions.
Design Complexity	Slightly more complex to design.	Simpler design but less efficient.

- Why Use a Positive Edge-Triggered Counter?

  →The counter updates only when the clock signal transitions from **low to high** (positive edge).

- **Pin Specifications:-**

1. **Pin 1 (GND)**: Ground connection, the 0V reference for the circuit.
2. **Pin 2 (CLR - Clear)**: Active LOW input that resets the counter to `0000` when activated.
3. **Pin 3 (CLK - Clock)**: Positive edge-triggered clock input. The counter increments on each rising edge of the clock signal.
4. **Pin 4 (ENT - Enable T)**: Count enable input (low-active); must be HIGH along with ENP to allow counting.
5. **Pin 5 (ENP - Enable P)**: Count enable input (high-active); must be HIGH along with ENT to allow counting.

6. **Pin 6 (LOAD)**: Active LOW input. When LOW, the counter loads the value from the parallel inputs (A, B, C, D) instead of counting.
7. **Pin 7 (Q1)**: First bit (LSB) of the counter's binary output.
8. **Pin 8 (Q2)**: Second bit of the counter's binary output.
9. **Pin 9 (Q3)**: Third bit of the counter's binary output.
10. **Pin 10 (Q4)**: Fourth bit (MSB) of the counter's binary output.
11. **Pin 11 (RCO - Ripple Carry Out)**: Carry output for cascading multiple counters. Goes HIGH when the counter reaches its maximum count (1111).
12. **Pin 12 (A)**: Parallel data input for the least significant bit (LSB).
13. **Pin 13 (B)**: Parallel data input for the second bit.
14. **Pin 14 (C)**: Parallel data input for the third bit.
15. **Pin 15 (D)**: Parallel data input for the most significant bit (MSB).
16. **Pin 16 (Vcc)**: Power supply, typically +5V.

Truth Table:

Q3	Q2	Q1	Q0
0	0	0	0
0	0	0	1
0	0	1	0
...	...	...	...
1	1	1	1

2) SN74LS245N(Transreciever):-

- Purpose to include in 8-Bit Computer:-

  ### → Bidirectional Communication:-

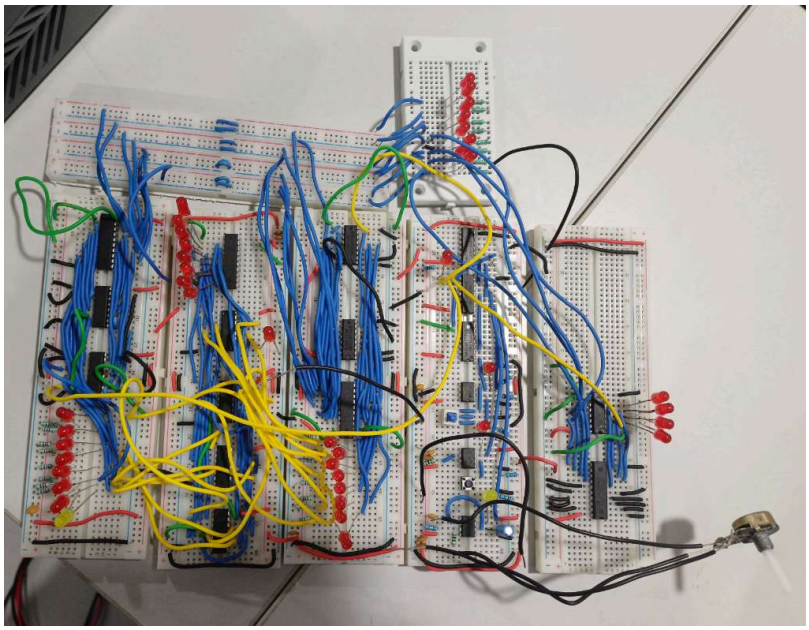
  The transceiver allows data to flow **in both directions**, enabling the counter to either send data to or receive data from other parts of the 8-bit computer, such as memory or I/O devices.

- Mechanism:-

  →A clock signal drives the 4-bit counter, which outputs a binary sequence (0-15) visible on LEDs. The transceiver (74LS245) controls data flow by sending the counter's output to an external bus(DIR=1).

C) Integration:-

Bread-Board:-



Theory: