INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, NAGPUR
B.Tech. (Electronics & Communication Engineering)
End Term Exam, III Sem (ECE), November 2022
Analog ICs (ECL 203)

Duration: 3 Hours BT21ECE045 **Marks: 50**

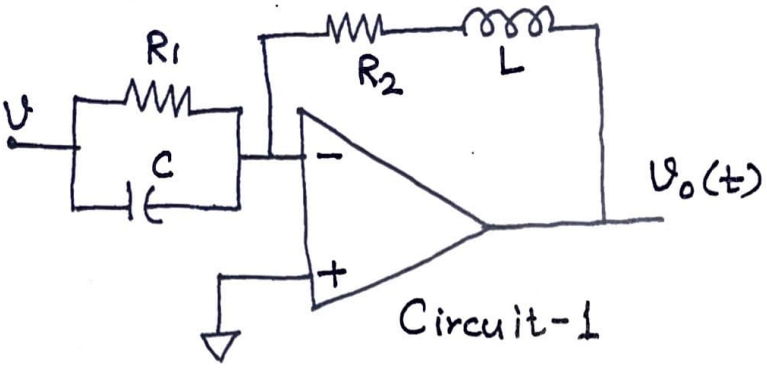
Instructions
All the questions are compulsory.
Assume suitable data, if necessary and indicate the same clearly.
Unless otherwise mentioned, symbols and notations have their usual standard meanings.
Draw suitable diagrams wherever necessary.

1. Explain the working of any five of the following circuit using Analog ICs with the help of a figure / Block diagram / Graph / Characteristics. [10 Marks, CO-3]
   (a) Positive Clamper
   (b) Half Wave Rectifier
   (c) Peak Detector
   (d) Sample and Hold Circuit
   (e) Schmitt Trigger
   (f) Instrumentation Amplifier
   (g) All pass filter
2. Consider the Analog IC - 565 (Phase Locked Loop), [2, 3, 5 Marks, CO-5]
   (a) Draw the pin diagram
   (b) Explain the working of PLL using block diagram
   (c) Design a circuit having input frequency $f_i = 1KHz$ and to generate output frequency $f_o = 2KHz$
3. Generate the sawtooth and triangular waveform using IC - 555 and IC - 741 having the $T_{ON} = 0.6$ msec and its frequency is $1KHz$, also draw the circuit. [10 Marks] [CO-4]
4. For the given circuit -1, the output voltage is

$$-v_o = a_2\frac{d^2v}{dt^2} + a_1\frac{dv}{dt} + a_0v$$

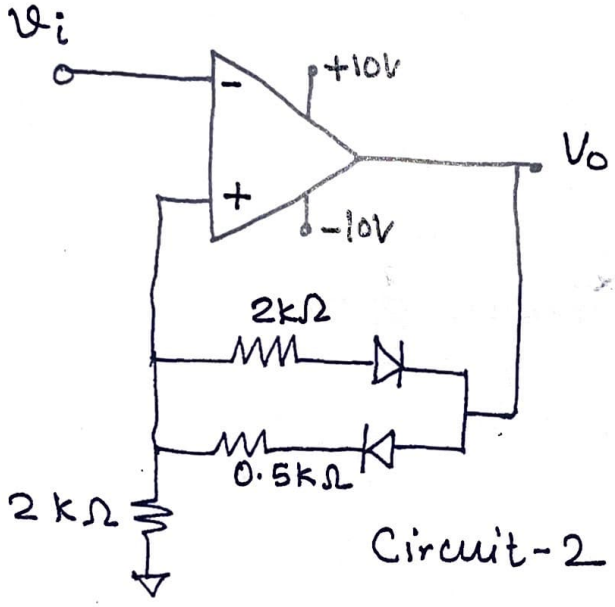
   find the values of a_2, a_1, and a_0 in terms of passive components. [5 Marks] [CO-2]
5. Use ±12V power supply and 741 IC. Design Wein-bridge Oscillator for 1000 Hz. Also derive the frequency and condition for sustained oscillation. [5 Marks] [CO-2]
6. Design 3^{rd} order butter-worth LPF having $f_c = 1KHz$, also justify the impact of order in the filter. [5 Marks][CO-3]

Analog ICs



Circuit-1

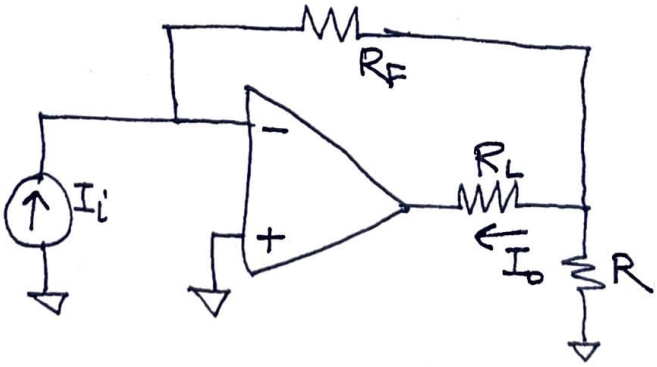
7.(a) Draw the Hysteresis plot for ckt-2 [2.5 Marks [CO-2]



Circuit-2

7(b) In the ckt-3, the expression for $\frac{I_o}{I_i}$?

[2.5 Marks]
[CO-2]



Circuit-3