

Basic Electronics

RC circuit Theory: Filters

$R \rightarrow$ resistor, $C \rightarrow$ capacitance, $L \rightarrow$ inductor, $\omega \rightarrow$ angular frequency

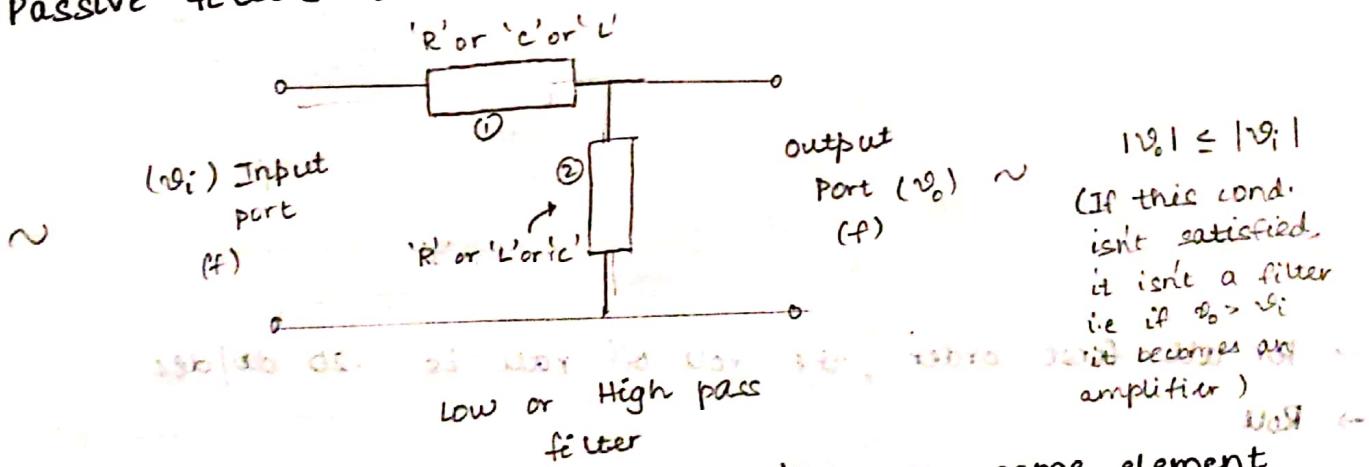
Resistance by ' R' = $X_R = R$ (reactance of R is R and it's independent of freq), $f \rightarrow$ frequency of

Resistance by ' C' = $\frac{1}{\omega C} = \frac{1}{2\pi f C}$ = X_C (capacitance of processor (clock signal))

Resistance by ' L ' = $\omega L = 2\pi f L = X_L$ filter-frequency selective circuit

Types of Filters

- Active and passive
- Low pass, high pass, all pass, band pass, band stop
- First Order, second order etc.
- Butterworth, Chebychev, Bessel etc.
- Filter are primarily freq. selective (allows/blocks signals based on their freq).
- Passive filters utilize combination of R, C, L .



- Note that, at ① and ② we shouldn't have same element (for eg, if it's R and R , it becomes a voltage divider)

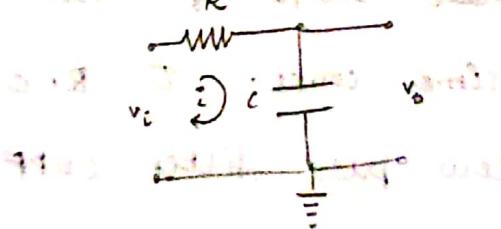
Low pass Filter

- Allows low frequency, blocks high freq. signals

$$V_o = V_i \left(\frac{Z_2}{Z_1 + Z_2} \right)$$

$$Z_1 = R, Z_2 = X_C$$

$$Z = \sqrt{R^2 + X_C^2}$$



In case of low pass filter

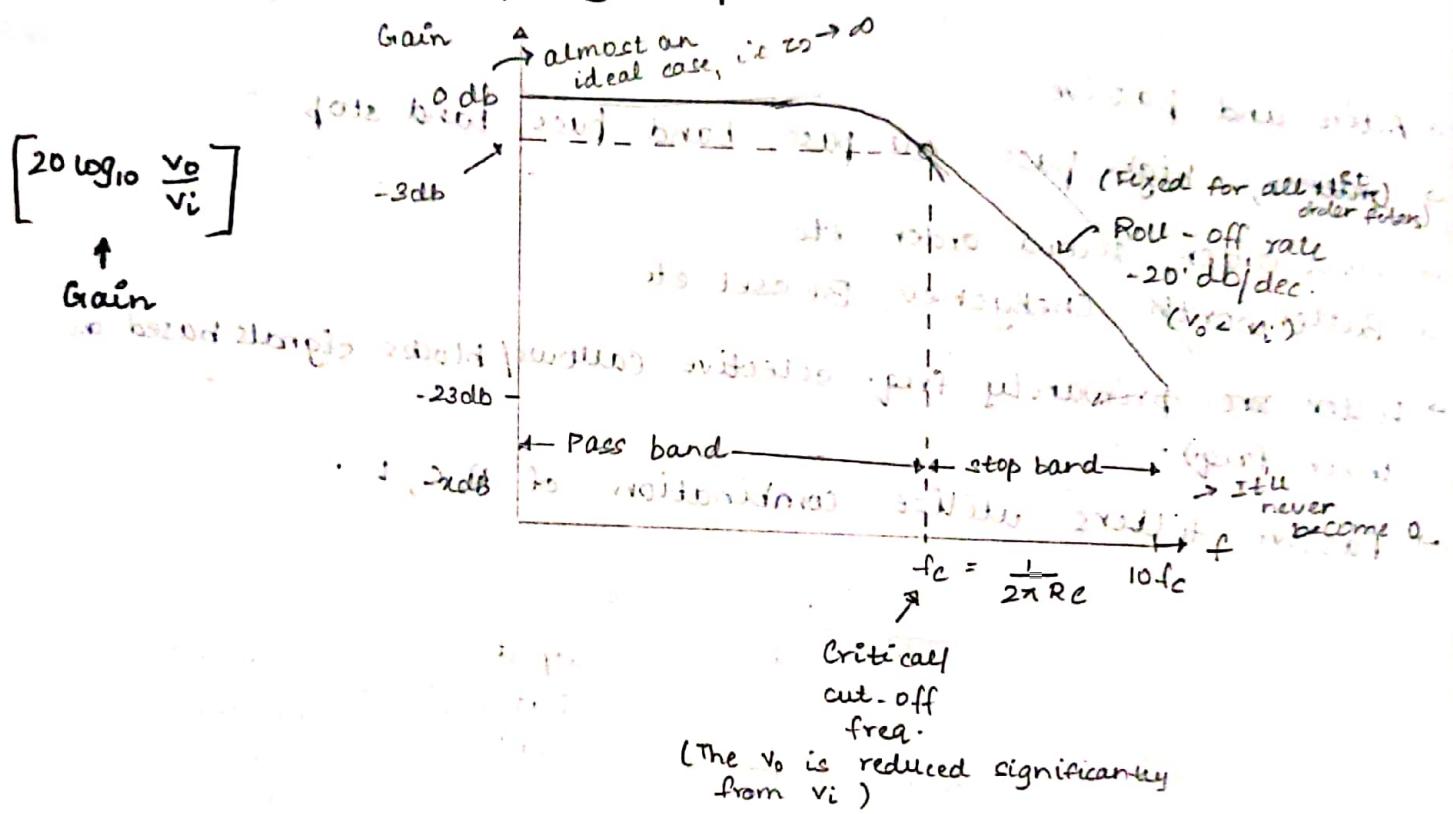
Pass band: low f signals $\frac{v_o}{v_i}$ will be $v_o \approx v_i$ in this case

Stop band: High f signals $\frac{v_o}{v_i}$ will be $v_o < v_i$ in this case

↳ when we say this, we mean that, even high freq. signals are passed, but with lower magnitude.

Hence it isn't rather it isn't possible for it to become an ideal filter.

Low pass filter's frequency response.



→ For all first order, the roll off rate is -20 dB/dec

→

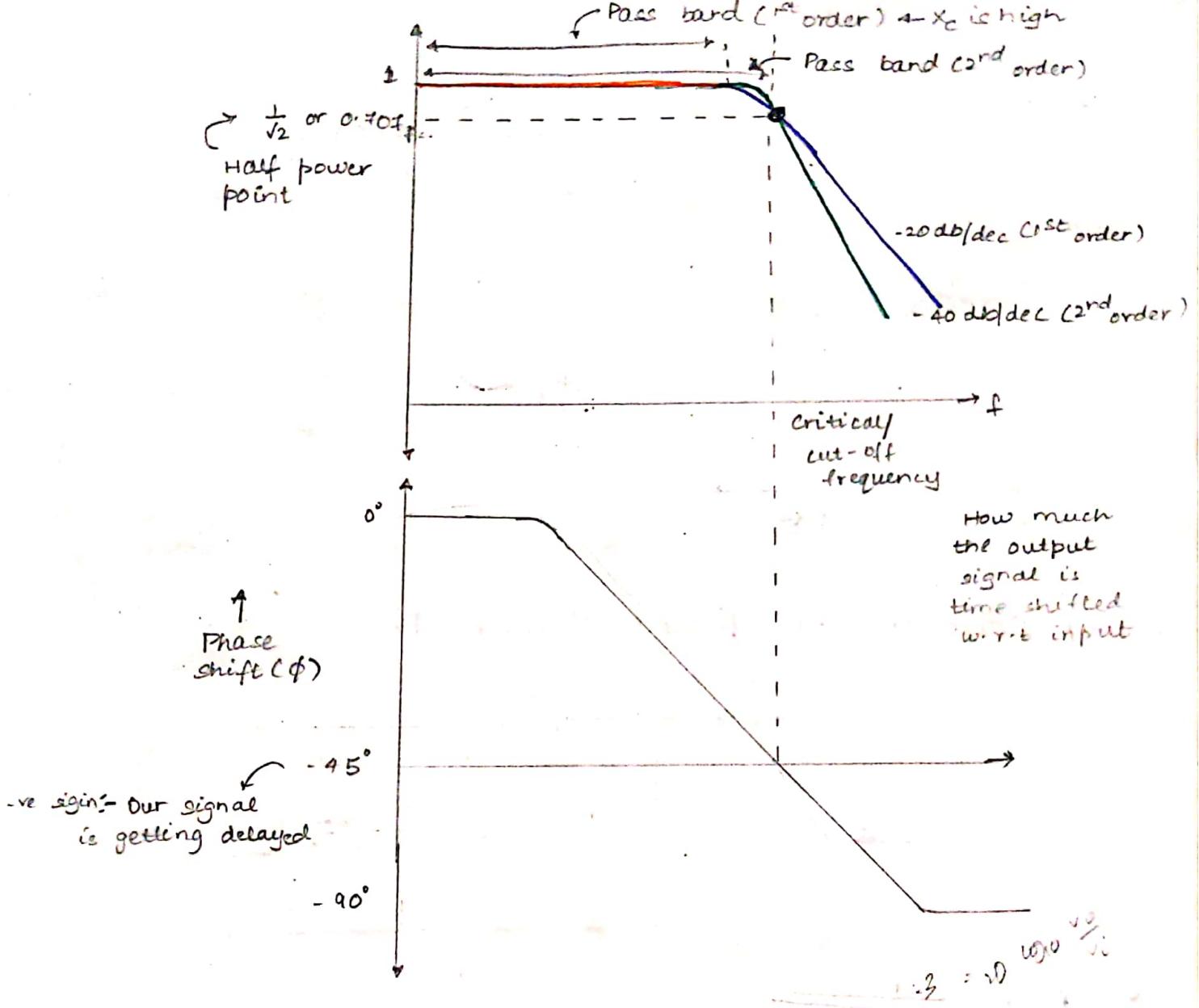
→ cut-off frequency is when v_o is reduced significantly from v_i

→ RC has affect on gain, phase-shift

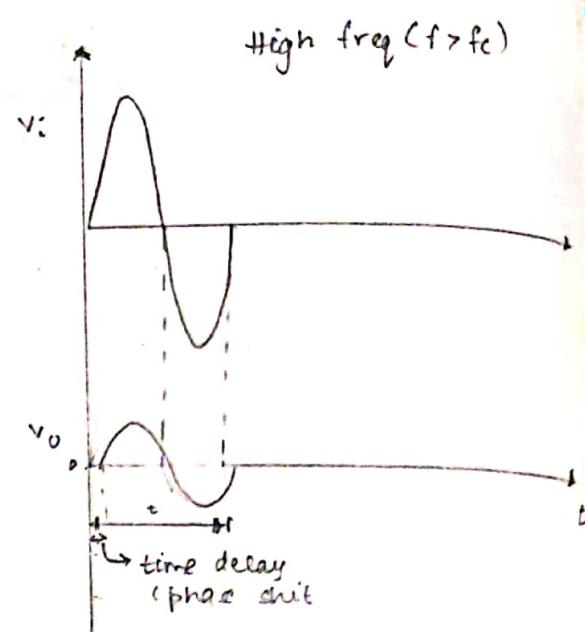
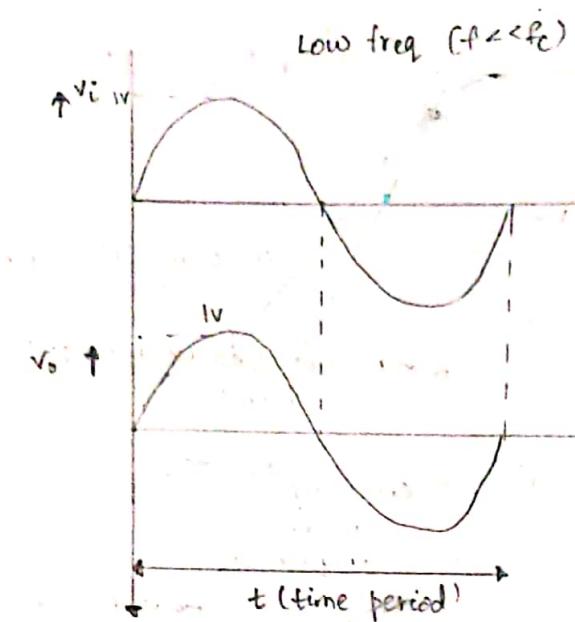
→ Phase shift $\phi = \tan^{-1}(2\pi f RC)$

→ Time const. $T = R \cdot C$

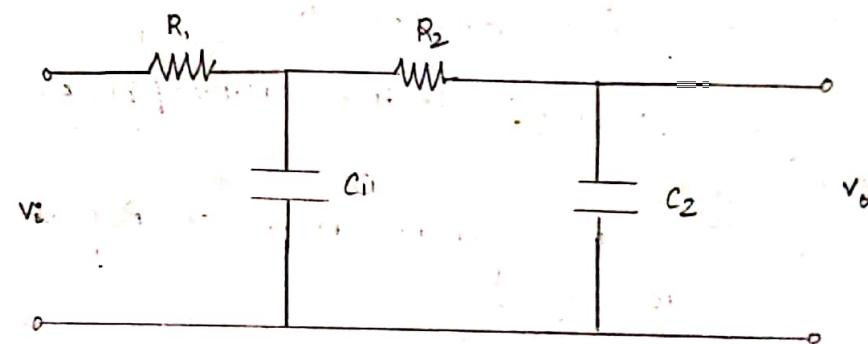
→ Low pass filter (LPF) is also known as 'integrator'



- 2nd order filter cuts the gain at a faster rate than 1st order, in [an ideal] gain \sqrt{f} freq, the gain should come to the freq. axis (\rightarrow), hence the graph for stop band must be slanted to that dotted line.
- In 2nd order filter, phase shift occurs at lower freq and thus 1st order is better.
- Even though time period changes in high freq, time period won't change



Second Order Low Pass filter (2nd order LPF)

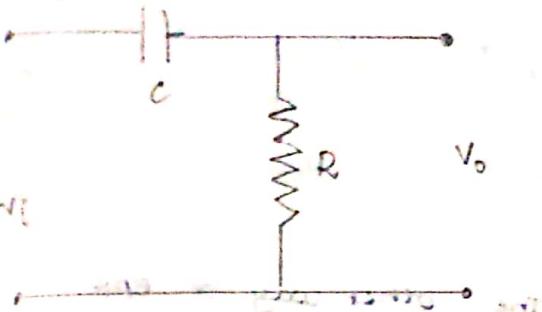


$$\rightarrow f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_2}}$$

$$\rightarrow f_{(3\text{db})} \approx f_c \sqrt{2^{(1/n)} - 1} \quad [\text{n=order}]$$

- Cascading of passive RC stages introduces attenuation. Max H/O/P can't be 0 db. It is less than 0 db in the pass band (undesired). Therefore, active filters

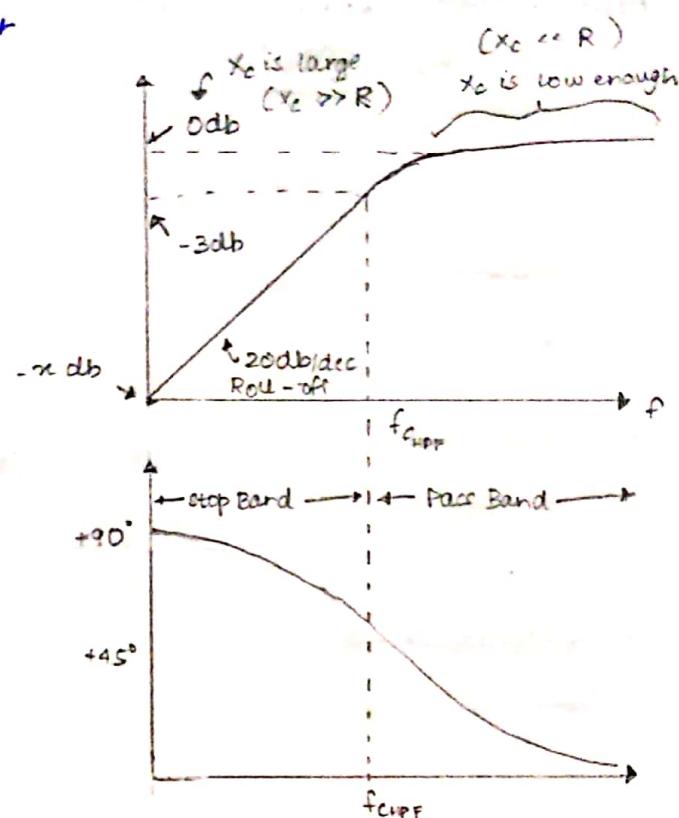
2) High Pass Filter (HPF) : 1st order



HPF \rightarrow Differentiator

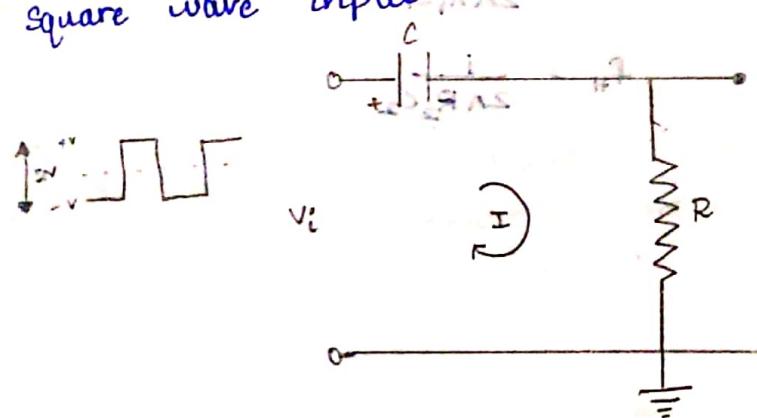
$$f_{CHPF} = \frac{1}{2\pi RC}$$

$$\phi = \tan^{-1} \left(\frac{1}{2\pi f RC} \right)$$



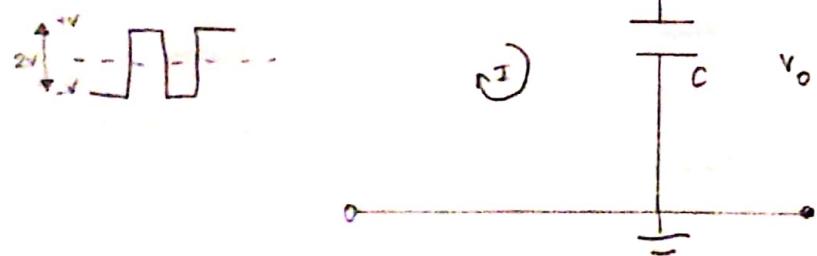
Note:-

square wave input



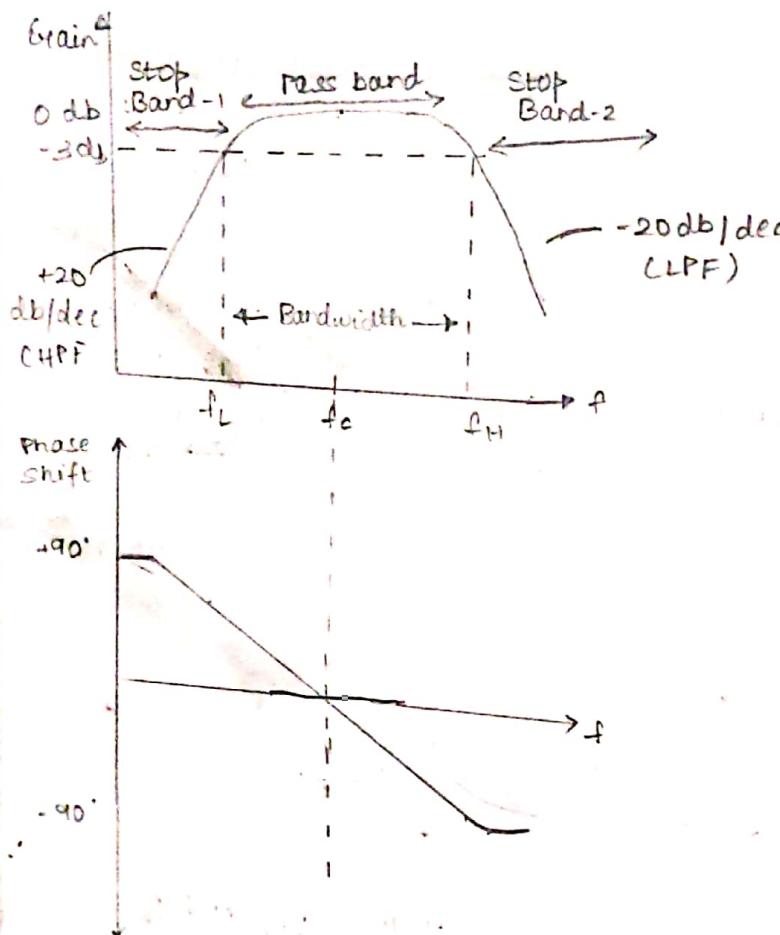
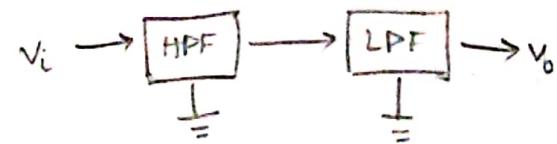
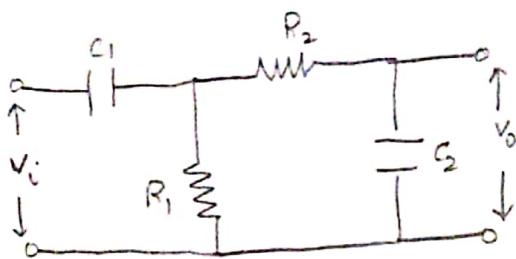
High Pass Filter

(series R, shunt C) make shunt C

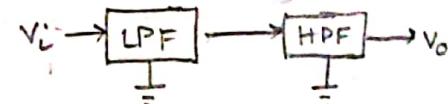
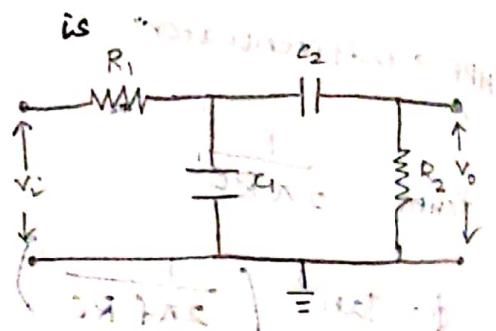


Low pass Filter

3) Band Pass Filter (BPF):



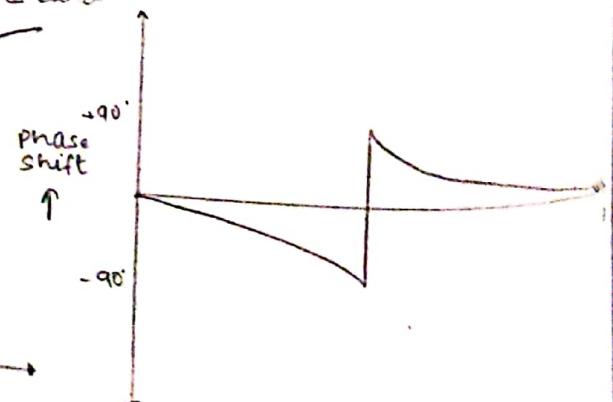
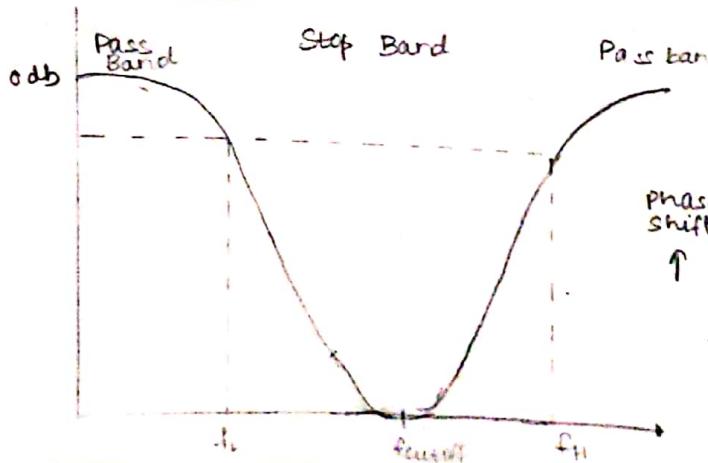
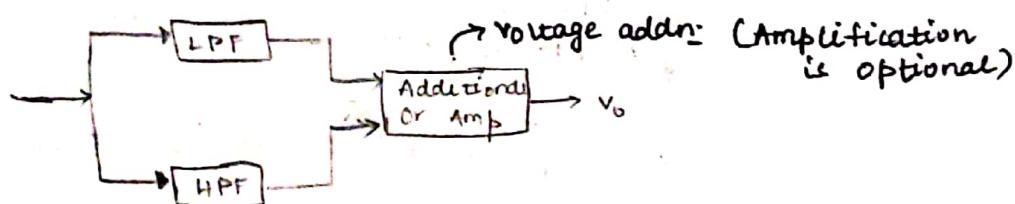
The other way of BPF



$$f_L = \frac{1}{2\pi R_1 C_1}$$

$$f_H = \frac{1}{2\pi R_2 C_2}$$

4) Band - Stop filter : (BSF)

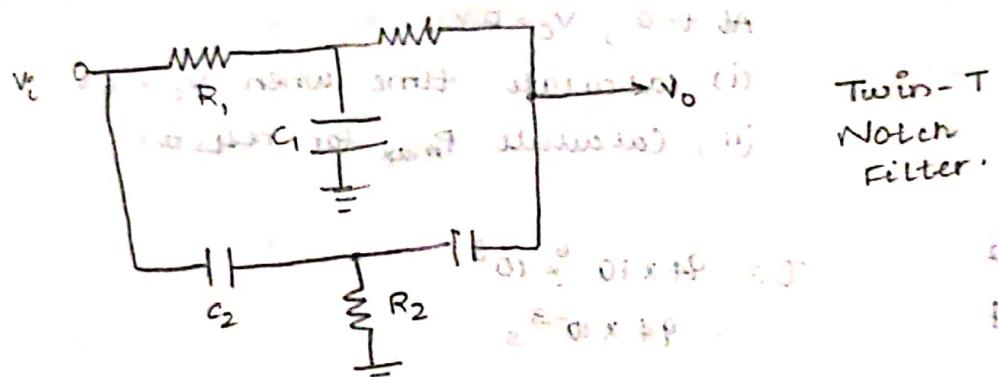


From 0 Hz, the gain of band stop filter is 0 dB and then at f_r , cut-off freq of LPF, it decreases and as we move on towards right, towards f_H , we see a rise in the gain, the middle of f_r and f_H is called a fcenter (f_c)

→ The requirement for a BSF is $f_r < f_H$

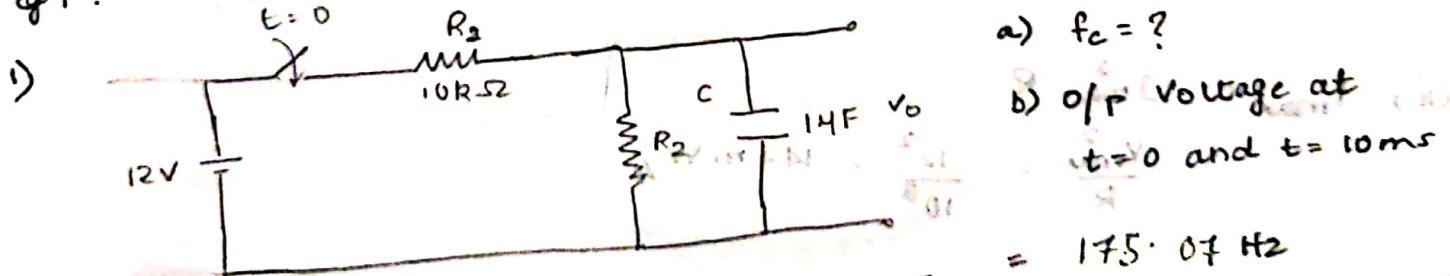
→ At about fcenter, the phase shift is drastic

→ The BSF is also called notch filters, if the diff. between f_r and f_H isn't so great (i.e. in the graph if the stop band width is narrow).



5) All pass filter: Usually active type. pass. all freq. at a const. gain changes phase shift w.r.t freq.

Eg 1:-



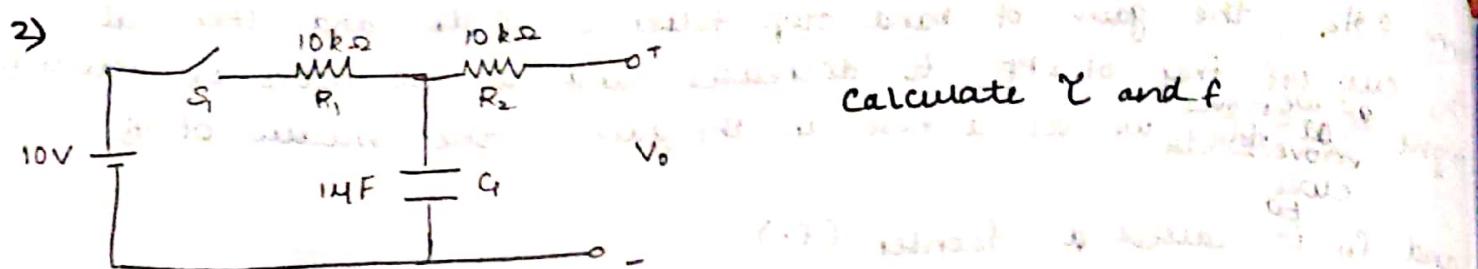
$$\text{Ans) a) } f_c = \frac{1}{2\pi(R_1||R_2)C} = \frac{1}{2\pi(10||10) \times 1 \times 10^{-6}} \text{ Hz}$$

$$\text{b) At } t=0, V_o = 0$$

$$T = (R_1||R_2)C = 909.45 \text{ ms}$$

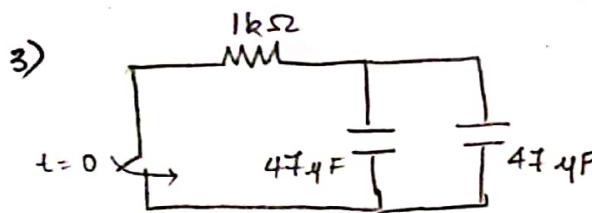
$$\text{At, } t \geq 5T, V_o \approx V_{\max}$$

$$V_{\max} = \frac{1}{1+10} \times 12 = 1.09 \text{ V} \Rightarrow \text{At } t=10 \text{ ms}, V_o = 1.09 \text{ V}$$



$$A) f_c = \frac{1}{2\pi R C} = \frac{1}{2\pi \times 10 \times 10^3 \times 10^{-6}} \text{ Hz}$$

$$\tau = R_1 C = 10^4 \times 10^{-6} \text{ s} = 10 \text{ ms},$$



$$\text{At } t=0, V_C = 12 \text{ V}$$

- (i) calculate time when $V_C = 6 \text{ V}$
- (ii), calculate P_{\max} for resistor

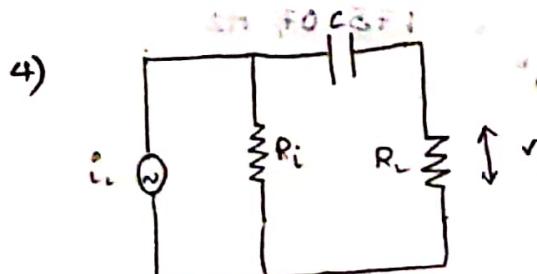
$$A) \text{eq} = C_1 + C_2 = 94.4 \text{ F}$$

$$\tau = 94 \times 10^{-6} \times 10^3 = 94 \times 10^{-3} \text{ s}$$

$$V_C = V_0 e^{-t/\tau} \Rightarrow 6 = 12 e^{-t/94 \times 10^{-3}} \Rightarrow t = 94 \times 10^{-3} \ln 2 = 65.15 \text{ ms}$$

$$B) i) P_{\max} = I_{\max}^2 R$$

$$= \frac{V_{\max}^2}{R} = \frac{12^2}{10^3} = 144 \text{ mW}$$



$$i_1 = \sin(2\pi ft)$$

$$R_i = 10 \text{ k}\Omega$$

$$f = 10 \text{ kHz}$$

$$L = 2.2 \text{ nF}$$

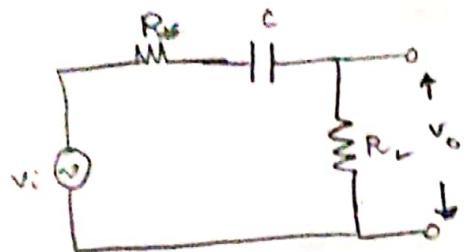
$$PR_L = 10 \text{ k}\Omega$$

calculate V_o at $t=1$

$$A) V_L = \sin(2\pi ft) \times 10 \text{ k}\Omega$$

$$= 10 \times 10^3 \sin(2\pi ft) \text{ V}$$

$$V_{FO} = 12 \text{ V}$$



$$V_b = I \times R$$

$$= \frac{V_L}{\sqrt{(R^2 + R_L^2)^2 + X_C^2}} \times R$$

$$= \frac{10 \times 10^3 \sin(2\pi ft) \times 10 \times 10^3}{\sqrt{(x+R_L)^2 + x_c^2}}$$

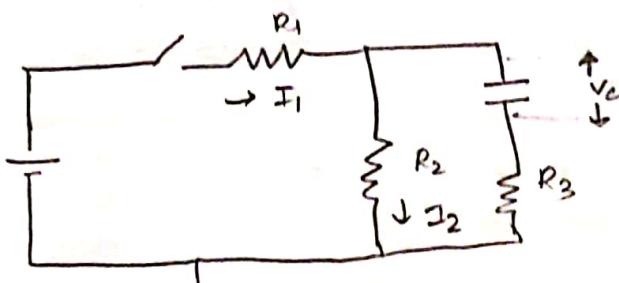
$$\left| \frac{V_o}{V_L} \right| = \frac{\omega R_L C}{\sqrt{1 + \omega^2 C^2 (R_L + R_s)^2}}$$

$$\Rightarrow \text{At } 10\text{kHz, } \left| \frac{V_O}{V_L} \right| = \frac{\omega R_L C}{\sqrt{1 + \omega^2 C^2 (R_L + R_L)^2}} = 0.47$$

$$\Rightarrow \text{At } 100 \text{ kHz} \quad \left| \frac{v_o}{v_i} \right|_{100 \text{ kHz}} = 0.499$$

$$\Rightarrow V_0|_{100\text{ kHz}} = 5 \sin(20 \times 10^6 \pi t) \text{ V}$$

5)



$$v_2 = 0 \quad \text{at} \quad t < 0$$

$$R_1 = 10 \text{ k}\Omega \quad R_3 = 1 \text{ k}\Omega$$

$$R_2 = 10 \text{ k}\Omega \quad C = 10 \mu\text{F}$$

At $t=0$, s_1 is closed (i) Find I_{s_1} and I_{s_2} at $t=0$, is

At $t=2$, s_1 is opened (D)

At $t = 0$, c is like a short

$$I_{10s} = \frac{q \times 10^{-3}}{20 + \left(\frac{10}{5}\right)} = 0.825 \text{ mA}$$

$$I_2|_{0A} = \frac{R_3 I_{1(0A)}}{R_2 + R_3} = \frac{1 \times 10^3 \times 0.825 \times 10^{-3}}{11 \times 10^3} = 75mA$$

$$T = \text{Req } c = 60 \text{ ms}$$

13 > T

At 1s, C is fully charged at 4.5V \rightarrow No 'I' through C

$$I_{1\text{(cls)}} = I_{2\text{(cls)}} = \frac{q}{R_1 + R_2} = \frac{q}{20K} = 0.45 \text{ mA}$$

: (ii) At $t=2s$, battery is disconnected

$$I_{(2s)} = 0$$

$$I_2(20\text{mA}) = \frac{4.5}{R_2 + R_3} = \frac{45}{11 \times 10^3} = 4.094A$$

$$I_2(\text{2s7min}) = 0 \text{ mA} @ 2.06^{\circ}\text{S}$$

44-0 2004-2005 2005 100 kHz 100 kHz

• (in 2010) die 3 : 344.001 N 42

$$a = 0.5 \text{ m} \quad g = 9.8 \text{ m/s}^2$$

21. 0-3. 300
22. 1. 12 days old. length 10. 432 mm. wt. 12. 0 g. JA
23. 1. 12 days old. length 10. 432 mm. wt. 12. 0 g. JA
24. 1. 12 days old. length 10. 432 mm. wt. 12. 0 g. JA

Ann Arbor MI 48106-1184

$$\Delta H_{\text{rxn}} = \frac{\text{Heat lost by water} - \text{Heat lost by calorimeter}}{\text{Mass of water}} = \frac{140.1 \text{ J/g}}{50.0 \text{ g}} = 2.802 \text{ J/g}$$

$$2\pi \times 3 = 3 \cdot \frac{\pi}{2} \approx 4.7$$

7 days old. The average in the first week is 2.5%.

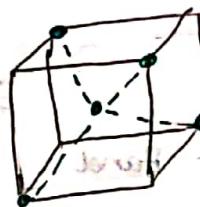
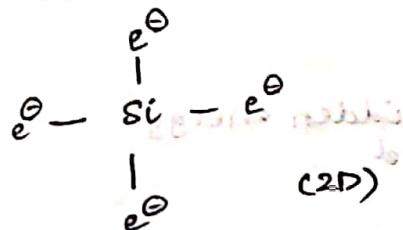
$$A = 3 \times 3 - \frac{8}{25} = \frac{8}{25} \times 3 \times 3 = \frac{8}{25} \times 9 = \frac{72}{25}$$

Semi-Conductors

Semiconductors are materials, the conductivity is between conductors and insulators

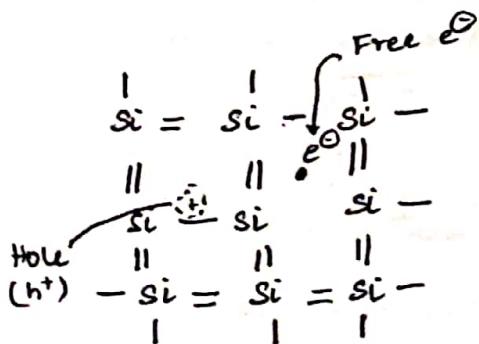
- Materials valency is 4 (four outer shell e⁻s -ve charged particles)
- Eg:- Silicon, Germanium, Carbon
- Gallium - Arsenide (GaA-As)

Silicon - Forms crystal matrix (crystalline solid structure)



(3D)

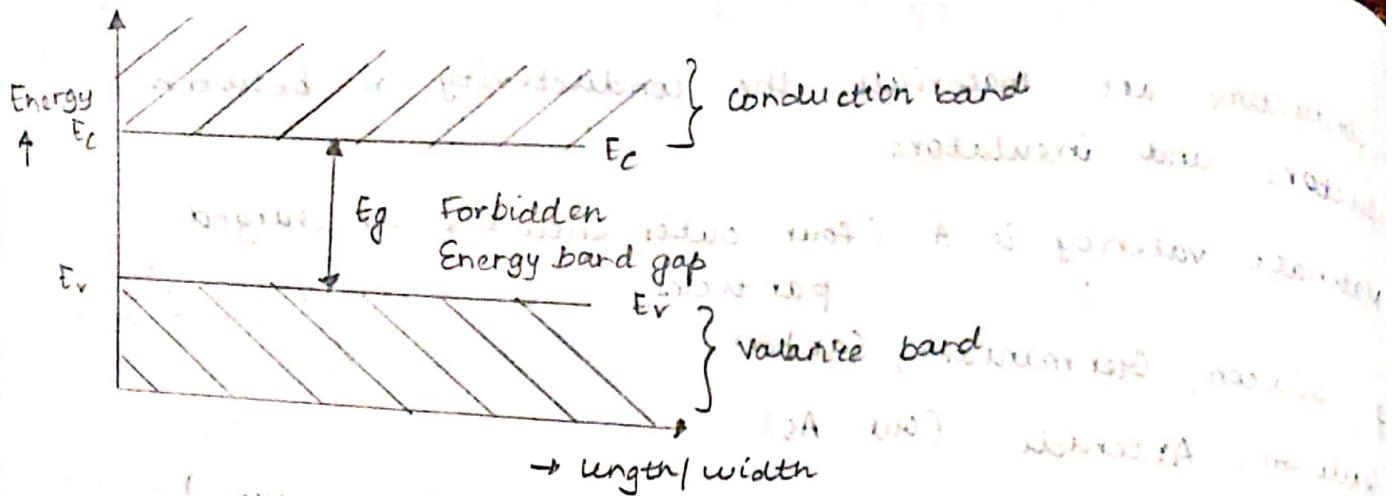
- 1 → representing one outer shell electron
- Si = Si = Si - → There is a uniformity in arrangement
 - Si = Si = Si - → Forms a covalent bond with nearby Si-atom.
 - Si = Si = Si - → This is case when $T = 0\text{ K}$ or -273°C
 - Si = Si = Si - → The e^- contributing to covalent bond are called immobile electrons
- If $T \uparrow$, then the e^- are gaining energy, which leads to breaking of covalent bonds, thus e^- moves freely (free e^-)
- In this state, we can say Si is an insulator as e^- aren't moving
- "Min. energy to gain for becoming a free e^- is E_g or band gap energy"



e^- : - very charged

h^+ : + very charged hole or absence of e^-

Now the e^- is free to move in the material, and there is a vacancy created at covalent bond site



- Energy band diagram is a plot drawn between length/width w.r.t energy
- 0 - E_v } Valence Band E_c - E_g } Forbidden energy
E_c - higher } Conduction Band band
- So as make an e^- move from valence band to conduction band, we have to supply min. amt. of energy, i.e. E_g
- When we supply an energy E_g to an e^- in valence band it becomes an free e^- as it goes to conduction band, and thus can conduct freely.
- No e^- are allowed to stay in forbidden energy gap.
- All these energies are measured in eV

Semi-Conductor

Si

largest band

1.1 eV

0.66 eV

Ge next largest band

C

5.4 eV

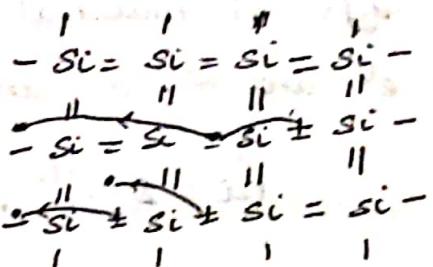
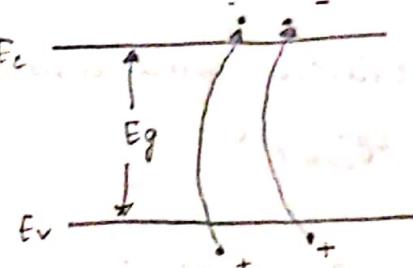
Ga-As

1.43 eV

Si is hard



Electron Transfer across energy bands



Net charge of a material is neutral. While an e^- moves away from its home position, a +vely charged hypothetical 'empty state' is created at that position. This +vely charged location moves, but in opp. direction of an e^- . A hole or n^+ (+vely charged) particle-like behaviour is true observed. It can loose energy.

true observed.
 e^2 can gain while going from $C \rightarrow V$, it can loose energy
 i.e. from $V \rightarrow C$ across junction voltage and making

while going from $\text{N} \rightarrow \text{O}$ the electrons in the valence band are the ones that are static and making covalent bonds.

Types of Semiconductor

Intrinsic	Extrinsic
<ul style="list-style-type: none"> → densities of e^- and h^+ are equal → offers low conductivity → No sub-types → Single crystal structure → Conductivity is more dependent on T → used to create extrinsic material → Rarely used directly → Pure 	<ul style="list-style-type: none"> → densities of e^- and h^+ are unequal → Higher conductivity → n and p-type → Distorted crystal structures → less dependent on T → Used to create electronic devices → Always used directly → Impure.

Intrinsic Semiconductors

- Only one type of material.
- Conc. of e^- and h^+ in an intrinsic semiconductor.

(s-c)

$$n_i = B \cdot T^{3/2} e^{-Eg/2kT}$$

B-co-eff related to specific s-c material

T - Temp in K

$$B_{Si} = 5.23 \times 10^{15} \text{ cm}^{-3} \text{ K}^{-3/2}$$

Eg - Band gap energy

$$B_{Ge} = 1.66 \times 10^{15} \text{ cm}^{-3} \text{ K}^{-3/2}$$

k - Boltzmann's const.

$$B_{Ga-As} = 2.10 \times 10^{14} \text{ cm}^{-3} \text{ K}^{-3/2}$$

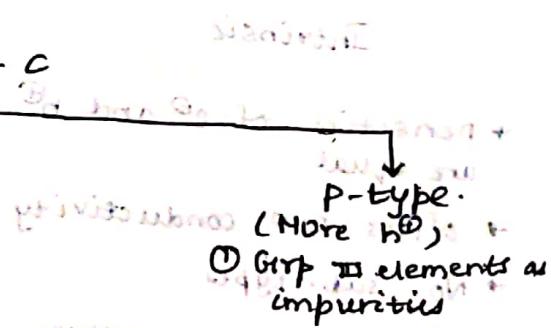
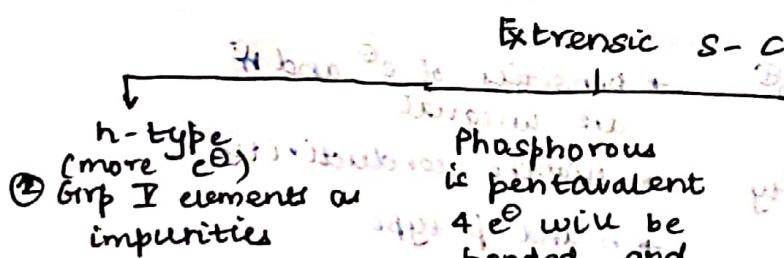
- B, Eg depends on the material

Extrinsic Semiconductors

- Made by combining intrinsic semiconductors by adding impurities (grp III / grp V)

Trivalent +
Impurities Fivalent
Impurities

- Doping is adding impurity.



② Acceptor Impurity (B)

Note :-

Relationship between e^\ominus and h^\oplus conc. in a S-C at thermal eq.

$$n_0 \cdot p_0 = n_i^2$$

$n_0 \rightarrow$ Thermal eq. conc. of e^\ominus
 $p_0 \rightarrow$ " " " of h^\oplus

$n_i \rightarrow$ Intrinsic carrier conc.

→ Extrinsic semi-conductors are dominated with holes or e^\ominus 's.

Majority and Minority carriers

- Majority carriers are the kinds of carriers inside an extrinsic semi-conductor which helps in conducting electrical current.
- Minority carriers are the again electrically conducting carrier but, it may oppose flow of majority carriers.

At $T = 300K$,

Consider we have added some pentavalent impurities to the S-C

If, donor imp. conc. (N_d) $\gg n_i \Rightarrow n_0 \approx N_d$ (majority carriers)

$$P_0 = \frac{n_i}{N_d} \approx \frac{n_i}{n_0}$$
 (minority carriers)

Consider each acceptor (Trivalent \rightarrow P-type) atom accepts a valence e^\ominus creating a hole.

Acceptor conc. $N_a \gg n_i \Rightarrow P_0 \approx N_a$ (holes) (P-type)

$$\therefore n_0 = \frac{n_i^2}{N_a}$$

Minority carriers

n-type

(Majority carriers) e^\ominus (Minority carriers) h^\oplus

Current conduction is dominated by e^\ominus flow

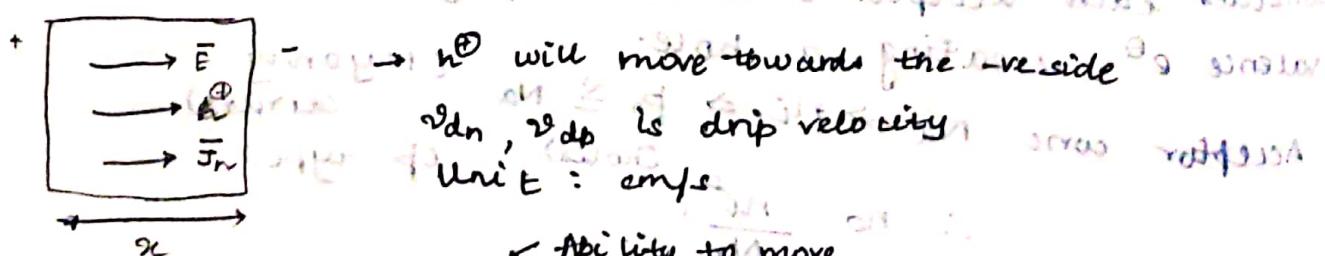
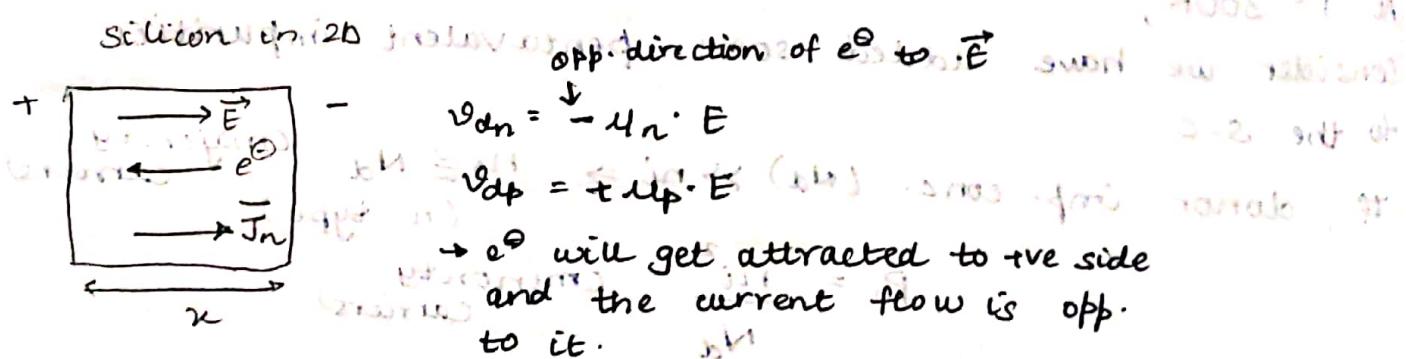
p-type

(Minority carriers) e^\ominus (Majority carriers) h^\oplus

current conduction is dominated by h^\oplus flow

Drift and Diffusion

- Basic processes that cause movement of e^- and h^+ in a semi-conductor.
- Current density is amount of current flowing per unit cross-section area of a material
Unit: A/m^2
- We talk in terms of current densities, as they help us to normalize or develop concepts which are much more fundamental and can be easily propagated to other complex phenomena.
- Diffusion current in S-C is caused by diffusion of charge carriers (e^- or h^+) or concentration gradient inside the material (e.g. Si)
- Drift current in a S-C is caused due to external force being exerted for movement of e^- or h^+



u_n : Electron mobility freely $\approx 1350 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}$
($\text{cm}^2/\text{V}\cdot\text{s}$)

u_p : Hole mobility $\approx 480 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}$

They are hypothetical carrier, rather they are passive effect observed due to absence of e^- , thus it's slower.

e[⊖] drift produces drift current density (J_n) A/cm²

$$J_n = -q n v_{dn} = +q n \mu_n E, \quad n = e^{\Theta} \text{ conc. } (\text{cm}^{-3})$$

n[⊕] drift produced drift current density (J_p) A/cm²

$$J_p = +q p v_{dp} = -q p \mu_p E \quad p = h^{\oplus} \text{ conc. } (\text{cm}^{-3})$$

conductivity (σ) [1/Ωcm] \rightarrow determines how good our s-c is conducting

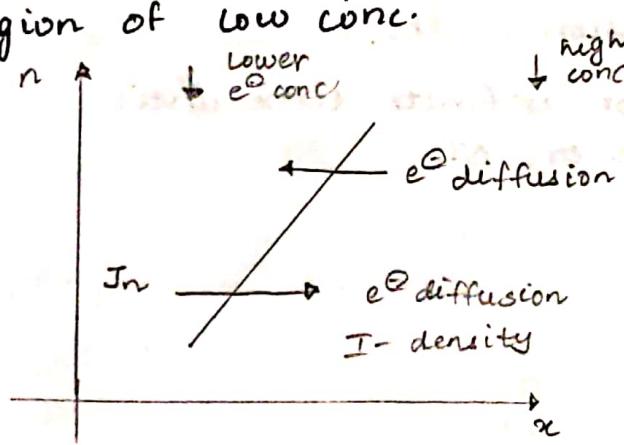
$$\sigma = q \cdot n \cdot \mu_n + q \cdot p \cdot \mu_p$$

In n-type s-c : $n \gg p$

In p-type s-c : $p \gg n$

Diffusion :

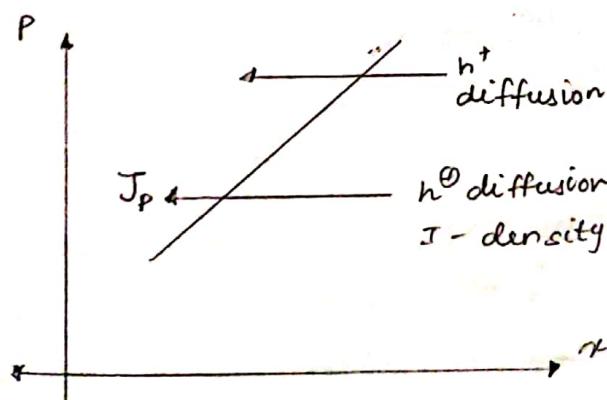
→ causes flow of particles from a region of high conc. to a region of low conc.



→ This will happen until the e[⊖] are uniformly arranged

$$J_n = q \sigma_n \frac{dn}{dx}$$

Gradient of
e[⊖] conc.
e[⊖] diff. co-eff



$$J_p = -q \sigma_p \frac{dp}{dx}$$

Gradient of
h[⊕] conc.
h[⊕] diff. co-eff

Excess carriers

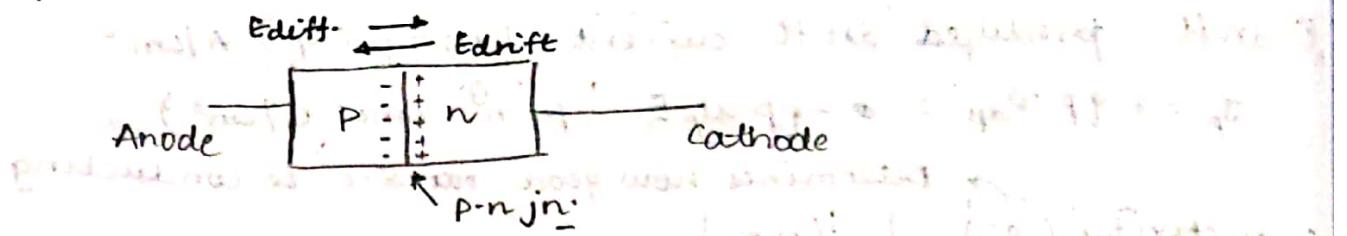
e[⊖] h[⊕] pairs are produced in a s-c while an external energy is applied

$$\therefore n = n_0 + \delta n, \quad p = p_0 + \delta p$$

excess carriers (only for a time)
At thermal eq.

Diodes

- A diode is a s-c device that is formed by using multiple extrinsic semi-conductors

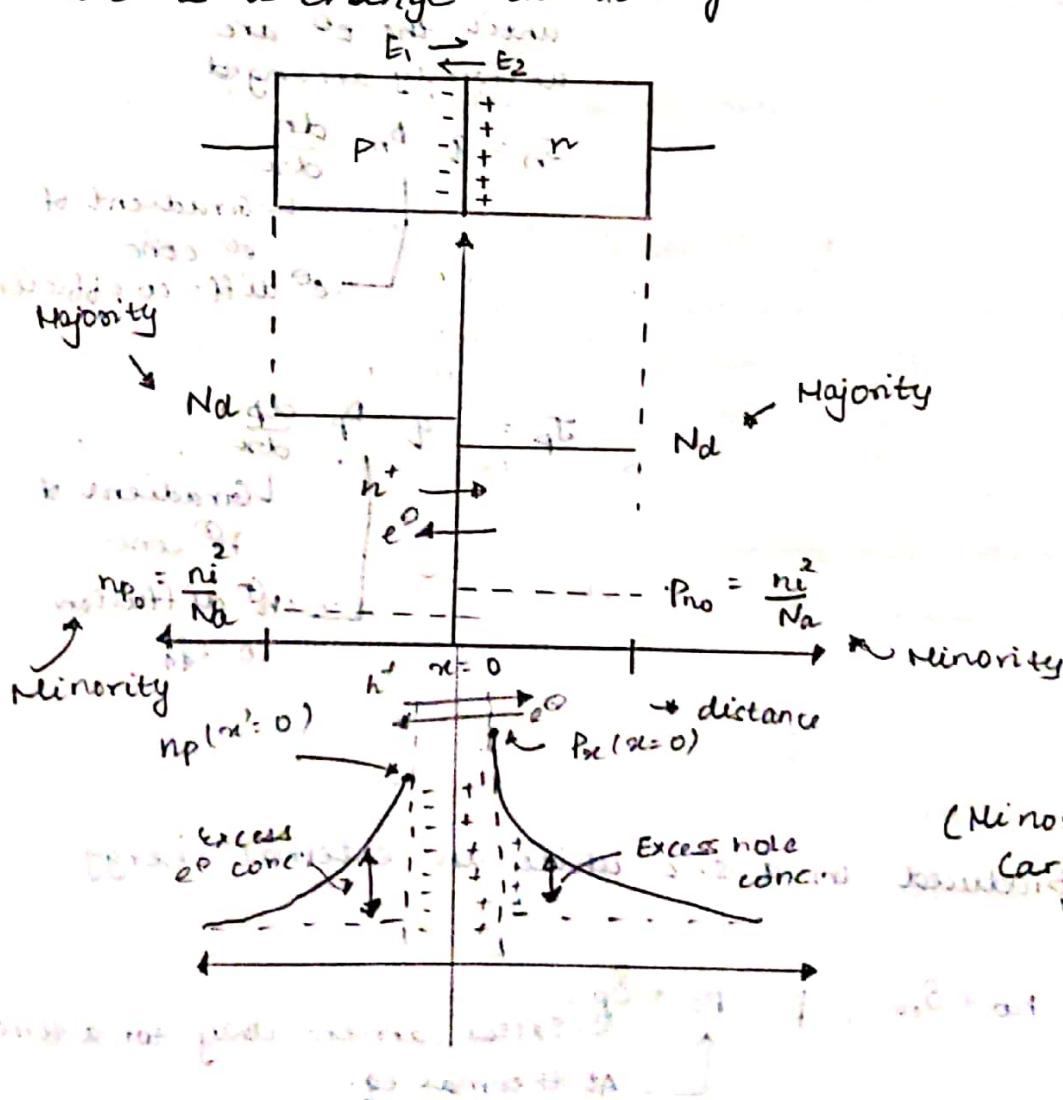


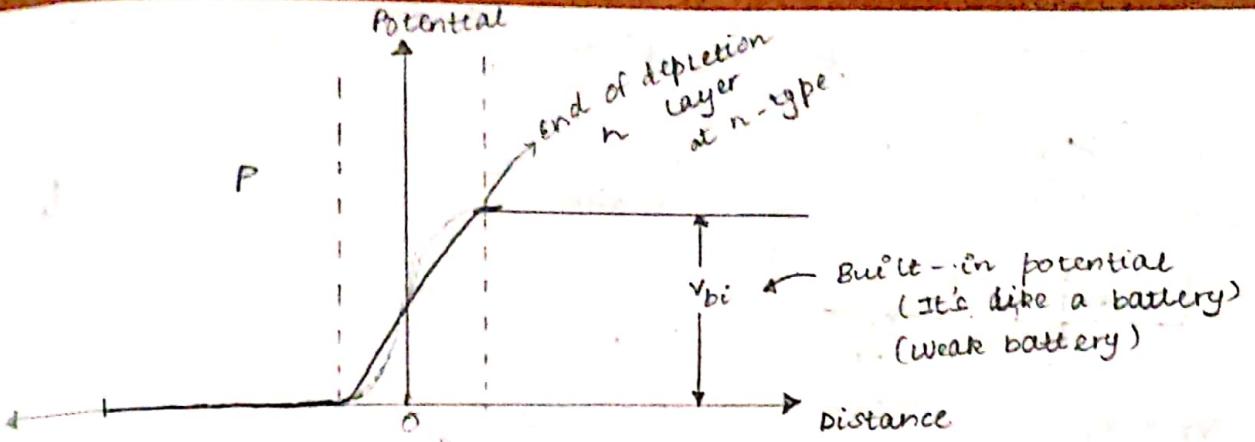
p-n junction region is also called space charge depletion region (containing immobile charge carriers) i.e they contain holes and e^- but they can't move. This happens on both sides of the junction.

This junction automatically forms when the regions are physically joined.

Electrons and holes due diffusion = drift was to merger.

And this process happens for infinite time until there is a change in voltage or AT





- At eq., $E_{\text{diff}} = E_{\text{drift}}$, thus the width of depletion layer remains same, but due to the electric field, there is movement of carriers across the jn:
- Accumulation of these charges, forms a voltage across the junction.

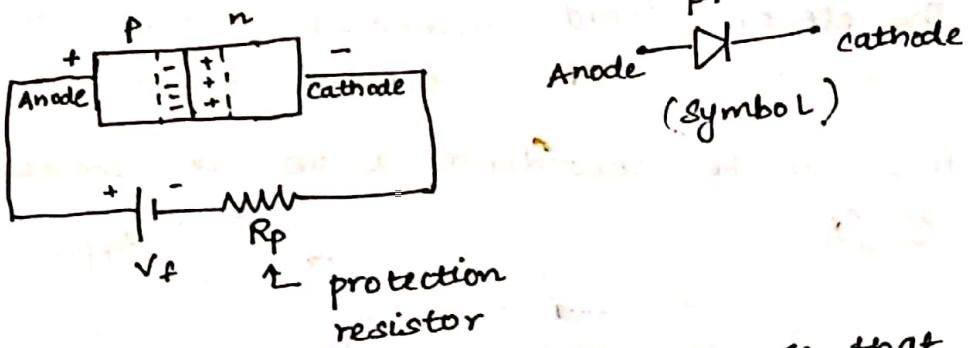
$$V_{bi} = \frac{kT}{q} \ln \left(\frac{N_A \cdot N_D}{n_i^2} \right) ; \text{ where } \frac{kT}{q} = V_T = 26 \text{ mV} \text{ (at } 27^\circ\text{C})$$

↑
Thermal v

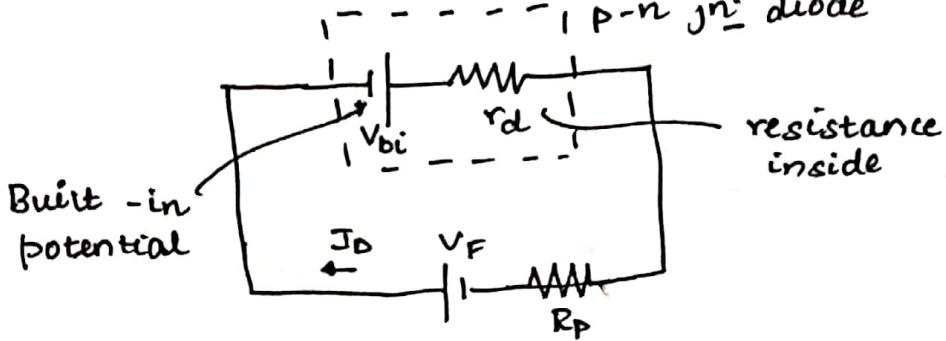
$$= V_T \ln \left(\frac{N_A \cdot N_D}{n_i^2} \right)$$

Biasing of p-n junction

① Forward biasing

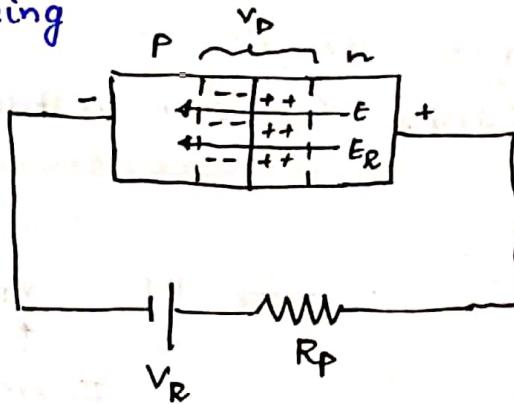


- R_p restricts the excessive flow of current so that the diode doesn't get damaged.
- Anode to +ve terminal, cathode to -ve terminal.
- Current flow from anode to cathode in the diode.
- ~~top reverse~~



$$\rightarrow I_D = \frac{V_F + V_{bi}}{R_p + r_d}$$

2) Reverse Biasing



$$\rightarrow V_D = V_R + \Delta V$$

- Wider depletion region actually shows, that if we apply a polarity such that as shown.
- The electric field increases, there is a significant increase in drift electric field.
- This can be considered as an eq. capacitor, represented by C_j

$$C_j = C_0 \left(1 + \frac{V_R}{V_{bi}} \right)^{-1/2}$$

Applied V

Built in potential

- C_j is too small in forward bias and thus neglected
- V_{bi} is same whether in forward / reverse bias

3) Diode Equation

$$i_D = I_S [e^{V_D/nV_T} - 1]$$

Diode current Reverse Bias saturation current Emission co-eff or ideality factor

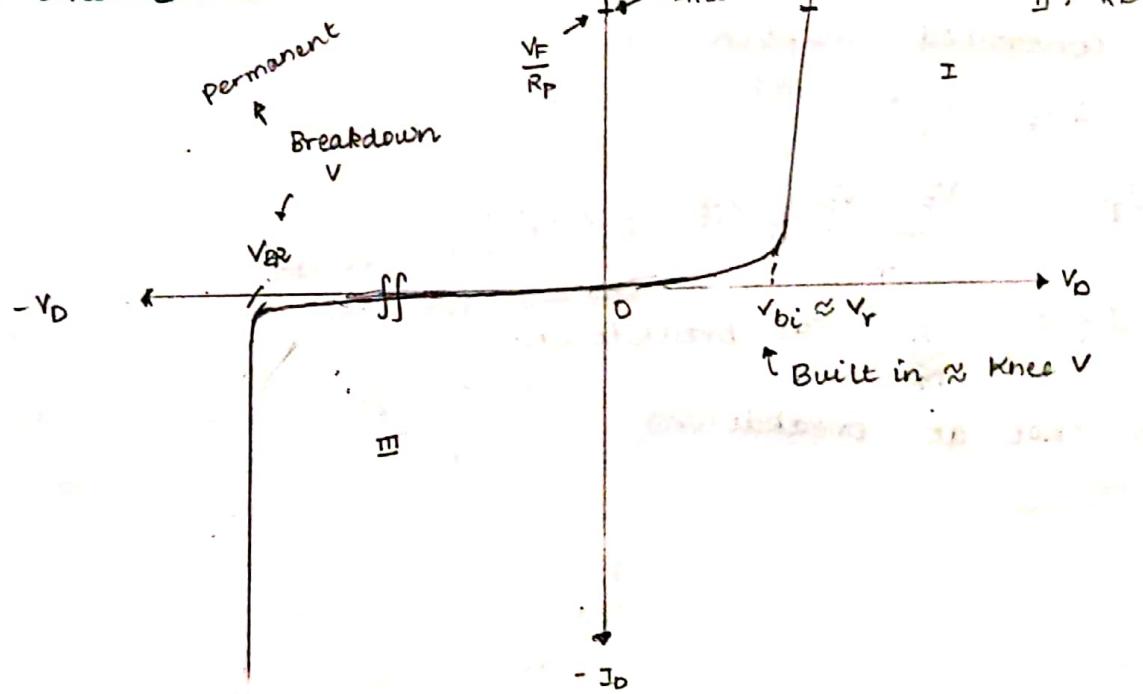
Thermal $V = \frac{kT}{q}$

$V_T \approx 26 \text{ mV} @ T = 300 \text{ K}$

$n = 1/2$

$I_S = 10^{-15} \text{ to } 10^{-13}$

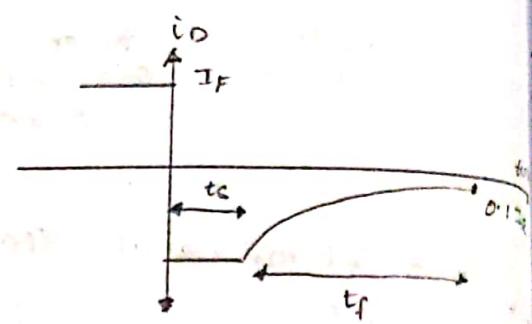
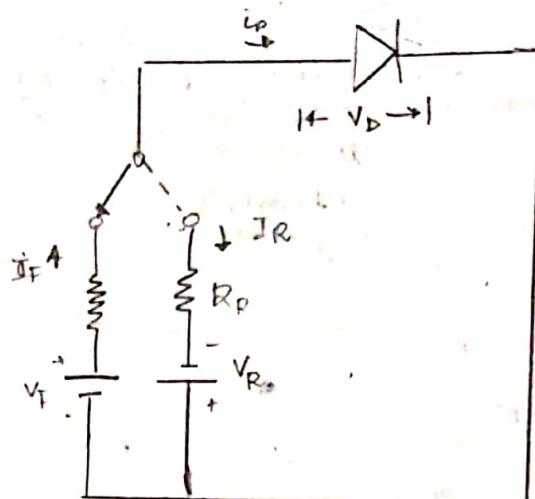
4) V-I characteristics



- **Breakdown:** Carriers collide when passing through the junction region (space charge region) and generates additional carriers, which causes larger reverse direction I (in top side), and thus damages permanently. This process is called avalanche breakdown process.

5) Diode ac switch

→ Inorder to control passage of current across the diode,



→ Voltage controlled switch

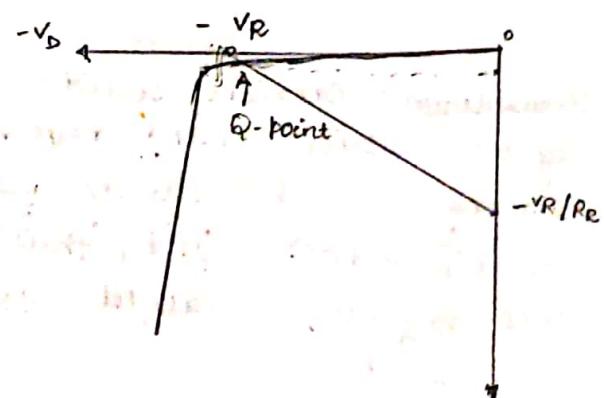
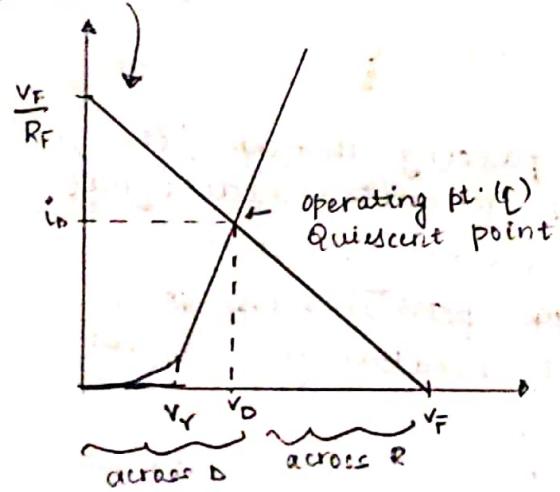
$$\rightarrow i_{DF} \approx 0 \text{ (if } V_F \leq V_r \text{)}$$

$$\rightarrow i_{DF} = I_F = \frac{V_F - V_D}{R_F} \text{ (if } V_F > V_r \text{)}$$

$$\rightarrow i_{DR} = -I_R = -\frac{V_R}{R_L} \text{ (at breakdown)}$$

$$\rightarrow i_{DR} \approx 0 \text{ (not at breakdown)}$$

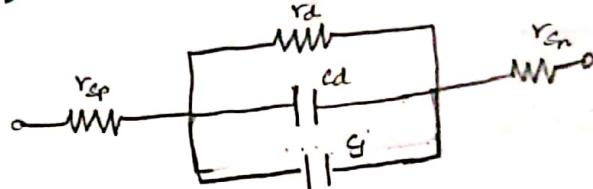
5) Load line



- That st. line is an imaginary between I_{Dmax} and V_F and it intersects with VI characteristics at some point. It is bound to intersect at some point.
- Q-point is the point that shows intersection of load line and VI characteristics.
- It shows us the actual value of diode voltage and diode current.

- When $V_r < V_D$, the q-point is towards the right of V_r
- We can't bring V_D to such a large value like V_F
- $0 \rightarrow V_D$ - voltage across diode, $V_D \rightarrow V_F$ - voltage across resistance
- $V_D = V_r + I_D r_f$
- $P_D = I_D V_D$
- Load line is an imaginary line and can change its position based on V_F and $I_{max} R_f$
- Q-points exists for both reverse and forward bias

6) Small signal Eq. Circuit



This is how a diode looks in its eq. steady state form, between its anode and cathode.

r_a, r_d : Diffusion eq. comp.

r_s : series comp. (eqv.)

Diode circuit

D) Power Supply architecture

→ consists of AC input source ($230V, 50Hz$)

→ Step down transformer is used

→ Step up transformer is used

→ Diode Rectifier (AC \rightarrow DC)

→ Pulsating DC

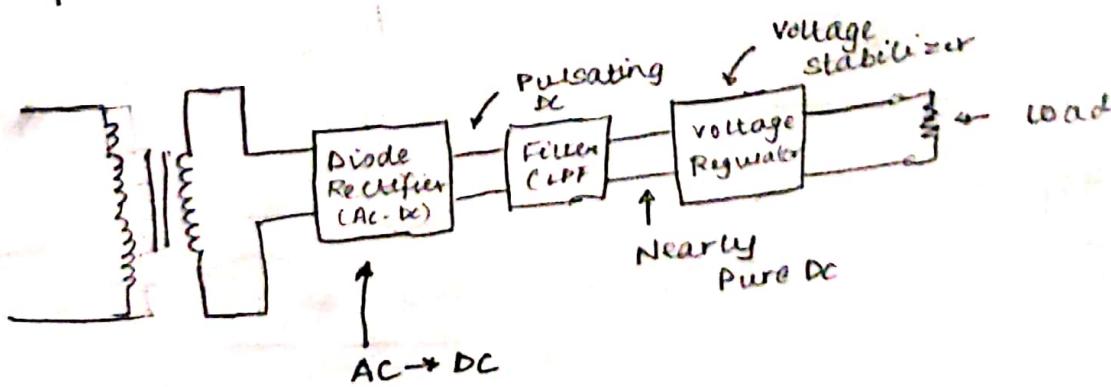
→ Filter C-LPF

→ Nearly Pure DC

→ Voltage Regulator

→ Voltage Stabilizer

→ Load

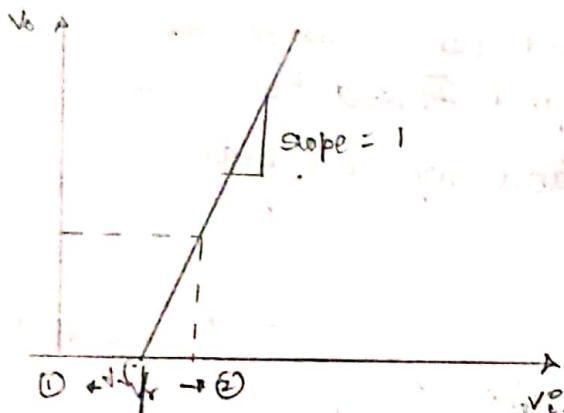
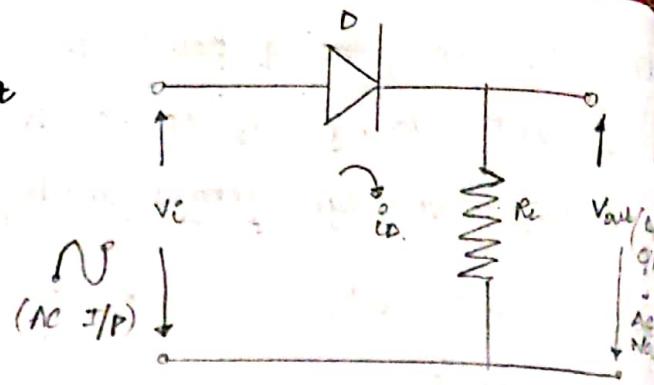


- Power transformer has low f, high M
- If the AC input change is small, then only we can expect a nearly pure DC output.
- Voltage regulator maintains a const. voltage output

2) Half-Wave Rectifier:

Rectifier is an electrical circuit that converts AC signal to DC signal

→ Only act on 50% of input signal



$$i_D = \frac{V_i - V_r}{R_L}$$

$$V_o = V_i - V_r = i_D R_L$$

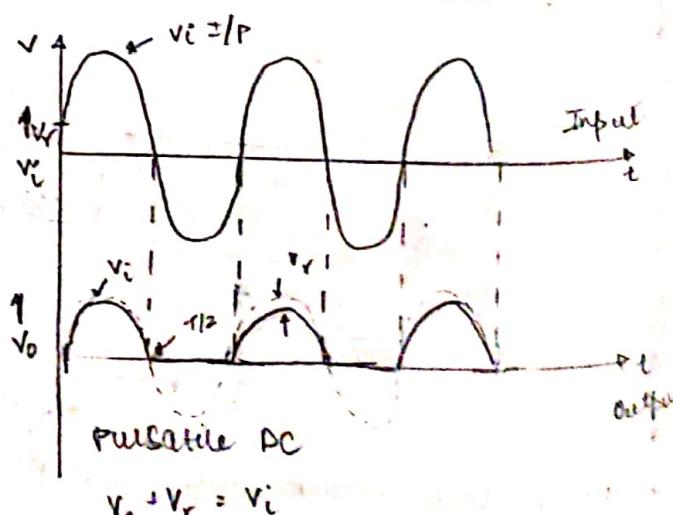
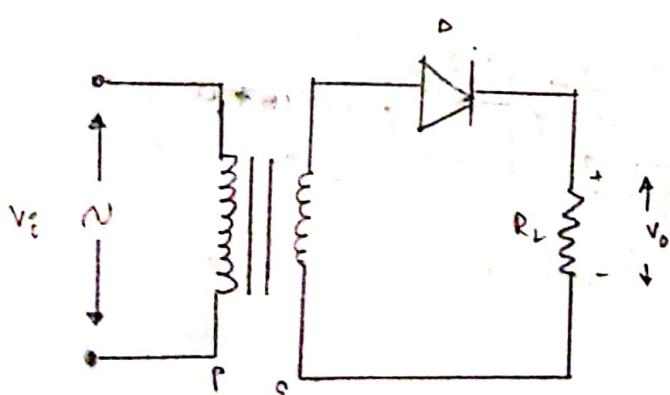
V_r - cut-in voltage (or knee voltage)

v-transfer characteristics

when voltage is -ve, it is on side ① and when +ve voltage is +ve, it is on side ②, so for some time our circuit is off.

For input voltage V_i , the output voltage V_o is less than V_i

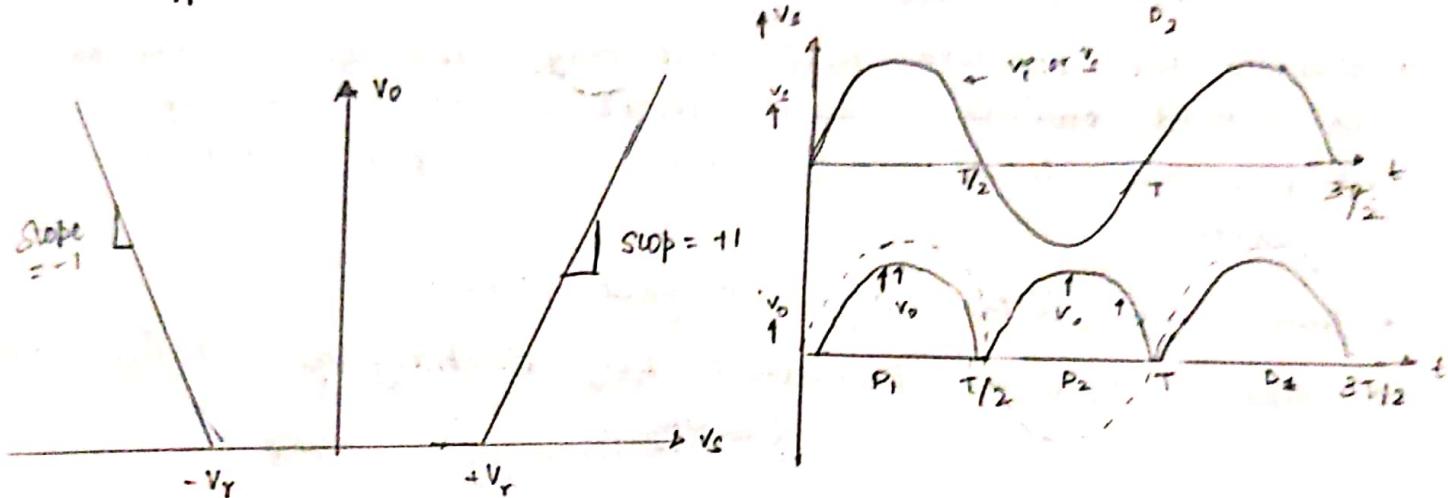
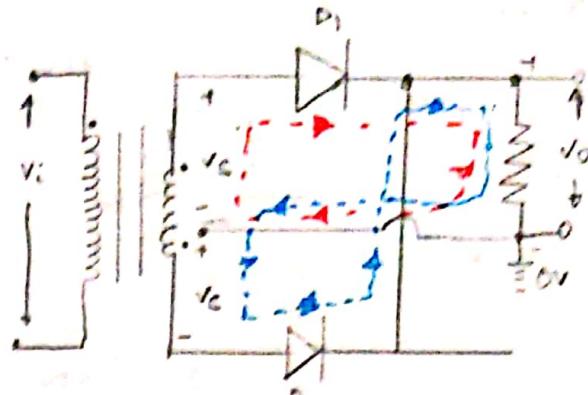
so During the positive half cycle of an AC input, we can see pulsating output, but during the negative half cycle, the circuit is in an off-cond. as diode is in reverse bias.



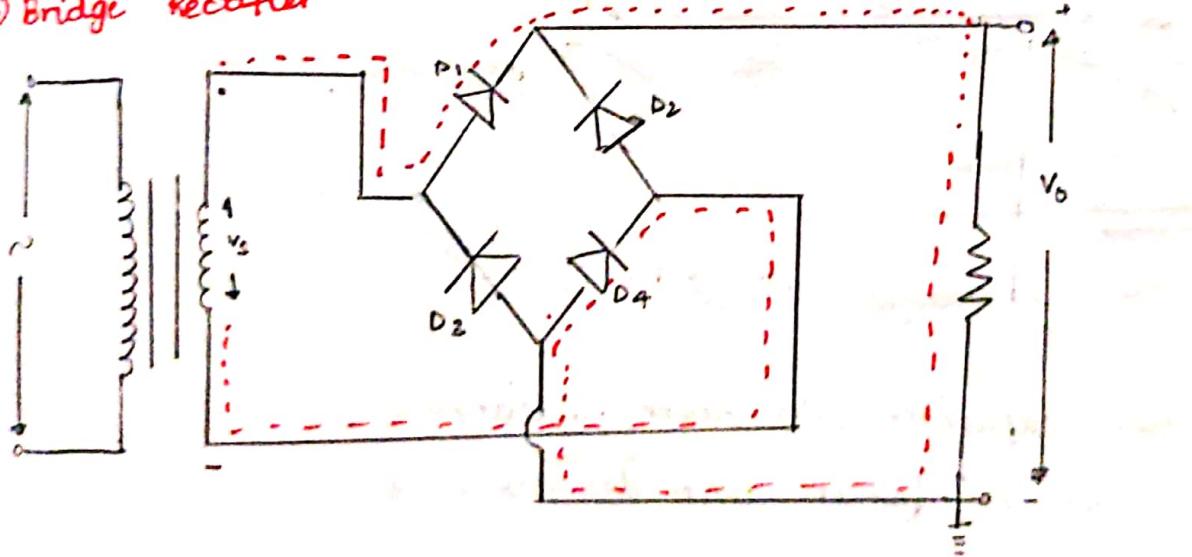
→ Inst. q-pt. isn't const, as input is time-varying voltage

2) Full Wave Rectifier

- operate on both +ve and -ve half cycles
- For +ve half cycle, the output is due to D_1 , and for the -ve half of the cycle, the current flow is due to the diode D_2 and D_1 is in off-cond in this cycle

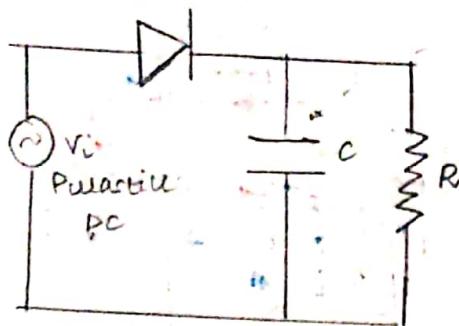


3) Bridge Rectifier

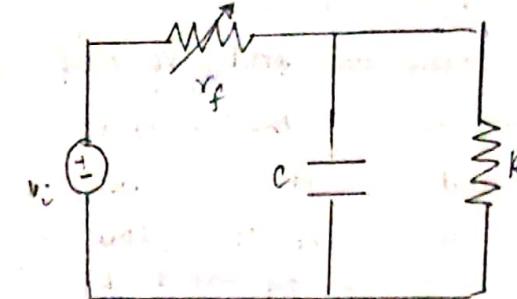


- During positive half cycle, it goes from $D_1 \rightarrow D_3$, while D_2 is in reverse bias
- And at node 0, in positive half cycle, it goes through D_4 and not D_3 , as already there was voltage drop while it came till node 0 and now there is -ve at the point through which D_3 should go.

4) Filters

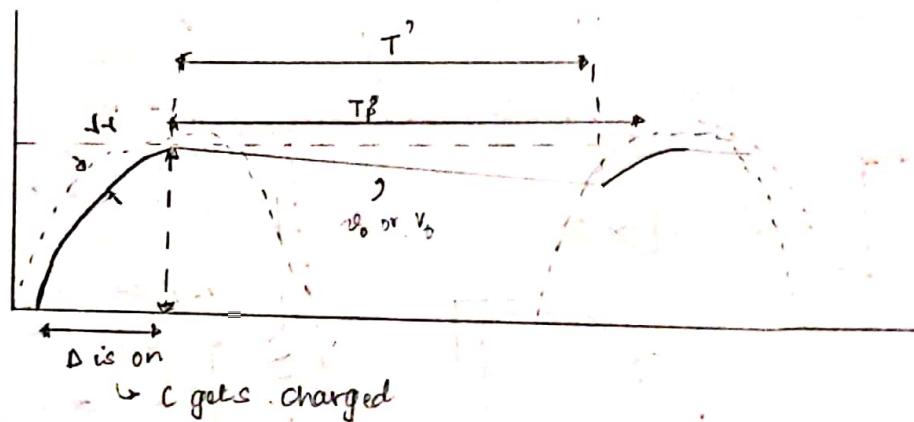


Filter capacitor



$r_p \approx 0$
(FB)
 $r_f \approx \infty$
(FP)

- During the positive half cycle only, the diode will be in closed switch, thus there is some voltage drop across diode and hence we replace by a resistor
- Thus, the filter is a low pass filter.
- charging through pulsatile DC, discharging through load R



- $R \gg r_f$, else capacitor will never discharge
- charging must be faster than discharging.
- For a bridge rectifier, it'll be same, except for a fact, that the diff will be $2V_r$.

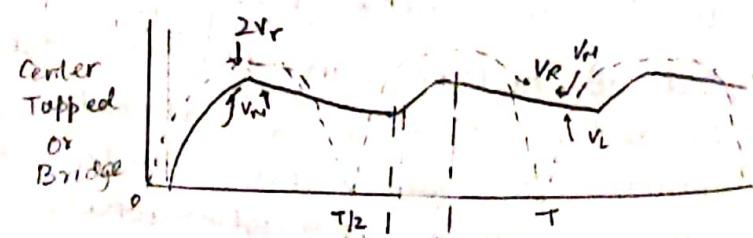
V_r : ripple voltage

$$V_r = \frac{V_H}{2fRC} = V_M - V_L$$

$$= V_M (1 - e^{-T/RC})$$

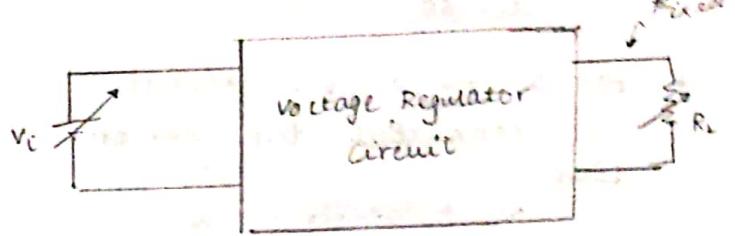
$$i_{o \text{ avg}} = \frac{1}{\pi} \sqrt{\frac{2V_r}{V_M}} \left[\frac{V_H}{R} \left(1 + \frac{\pi}{2} \sqrt{\frac{2V_H}{V_r}} \right) \right] i_{o \text{ max}}$$

$$\rightarrow T' \ll RC \quad i_{o \text{ max}} \approx i_{o \text{ peak}} = \frac{V_M}{R} \left(1 + \pi \sqrt{\frac{2V_M}{V_r}} \right)$$



5) Voltage Regulator

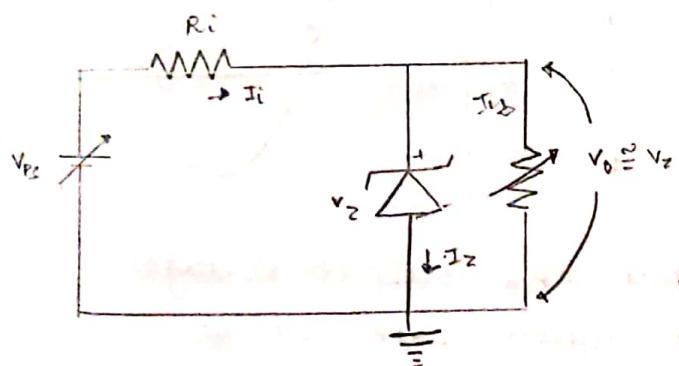
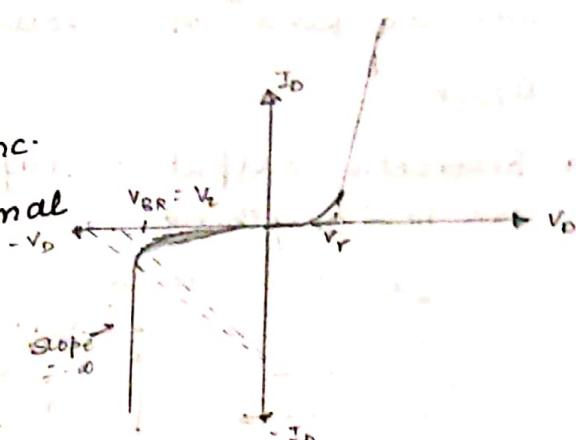
- stabilizes an o/p DC v while on I/P v is fluctuating within a range , or load R_L is changing within a range
- Filtered output is given as input to the voltage regulator , and a fixed value of voltage is the output
- Reduces the ripples



6) Zener diode as Voltage Regulator

a) z-diode characteristics (V-I)

- p-n jn⁻ diode having high doping conc.
- Breakdown voltage lesser than a normal p-n jn⁻ diode
- Thinner jn⁻ width



- Zener diode used in reverse bias only
- The voltage drop across the resistor is enough to bring the zener diode to the breakdown region

- V_z hardly changes (\because Slope $\rightarrow \infty$), thus even if voltage drop is diff, V_z doesn't change, hence V_o also remains const.

$$R_i = \frac{V_{PS} - V_z}{I_i} = \frac{V_{PS} - V_z}{I_z + I_L}$$

$$I_z = \frac{V_{PS} - V_z}{R_i} - I_L$$

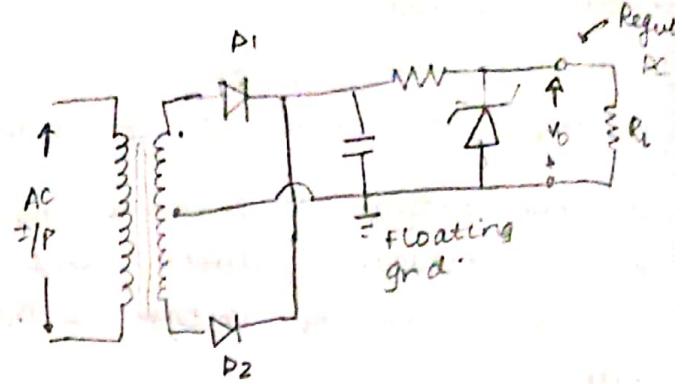
$$R_i = \frac{V_{PS\min} - V_z}{I_{z\min} + I_{L\max}} \approx \frac{V_{PS} - V_z}{I_{z\max} + I_{L\min}}$$

$$P_z = V_z I_z$$

$$I_{z\min} = \frac{V_{PS\min} - V_z}{R_i} - I_{L\max}$$

1) Linear DC power supply circuit

- Capacitive low pass filter, resistance is provided by the diode
- For a fixed DC signals we connected the zener diode.

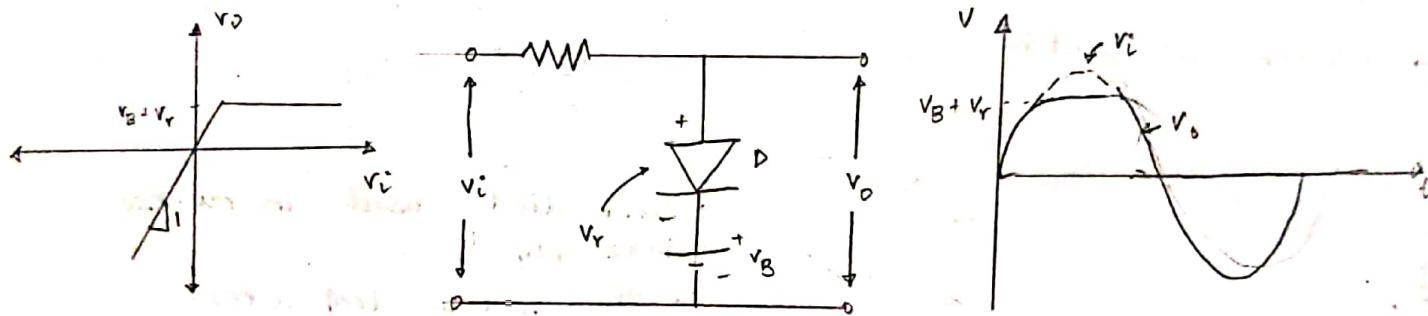


2) Clipper and Clamper (Voltage Limiter ckt.)

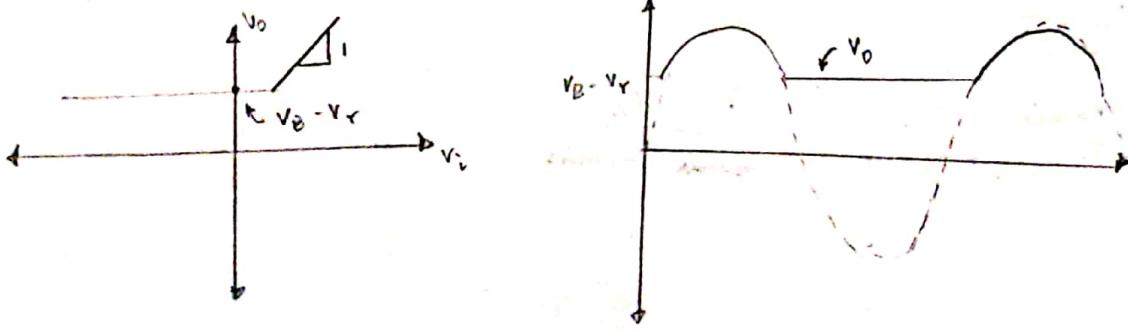
- They are kind of "voltage manipulator" circuits

a) Clipper

- Restricts output voltage beyond a voltage, while output can be anything



- Transfer char. is a plot b/w input and output voltages
- Resistor is acting like a single signal path i.e no current through resistor, since the diode is in off forward bias situation
- As voltage comes to $V_B + V_r$, the diode turns on, and there is voltage drop in the resistor.
- If we replace the polarity of the diode,

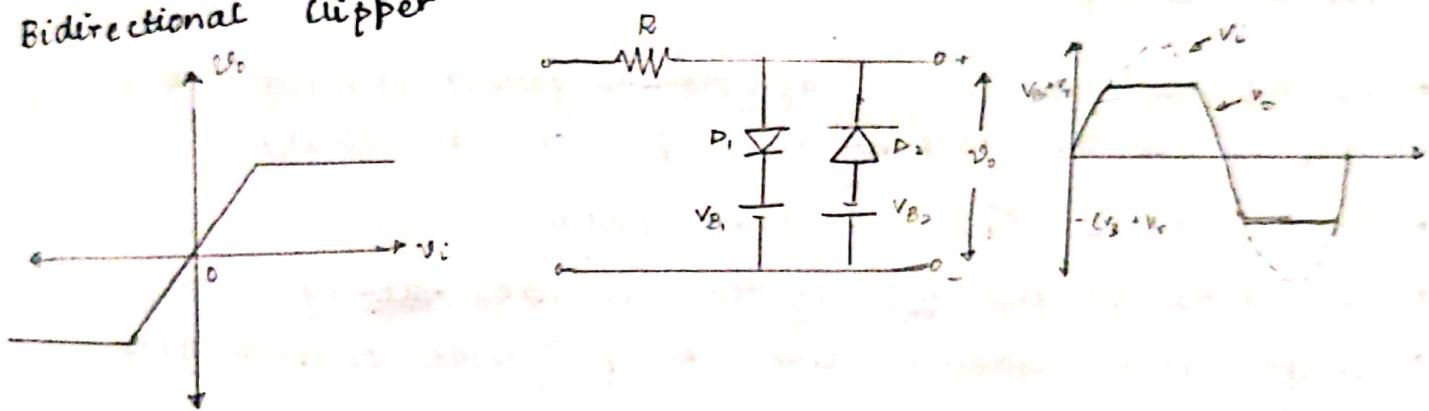


→ similarly we can make other configurations, now if we leave D the same but change the polarity of battery



→ Thus, clippers aim is to protect the other circuits, so that they don't get damaged

Bidirectional clipper



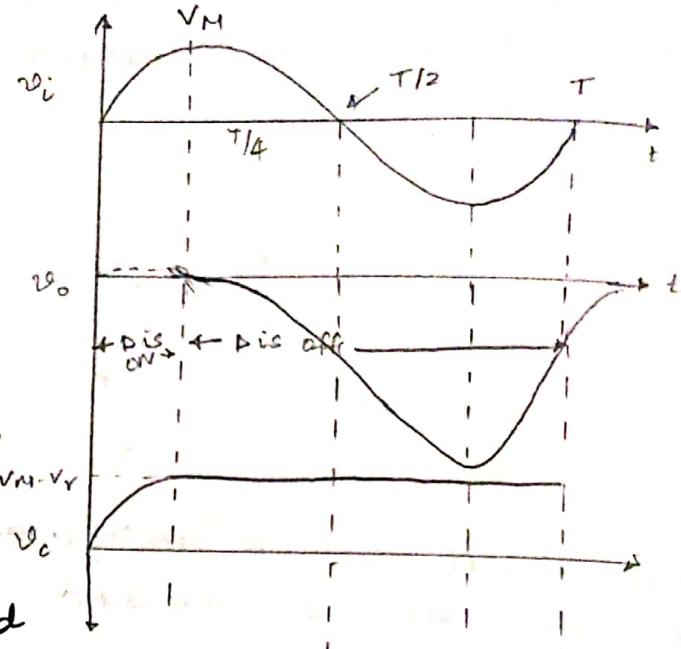
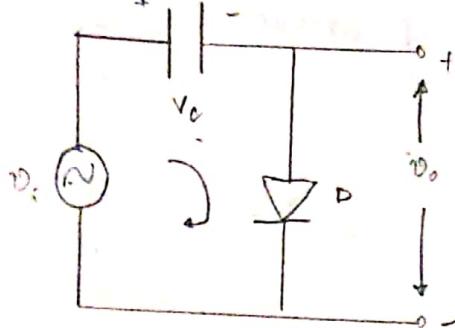
Germanium $V_T \rightarrow 0.3\text{ V}$

Silicon $V_T \rightarrow 0.74\text{ V}$

→ If we add an extra resistor in arm 1, we get a curve with lesser noise, due to the new resistor we get a rounded curve instead of a flat flat part.



b) Clamper

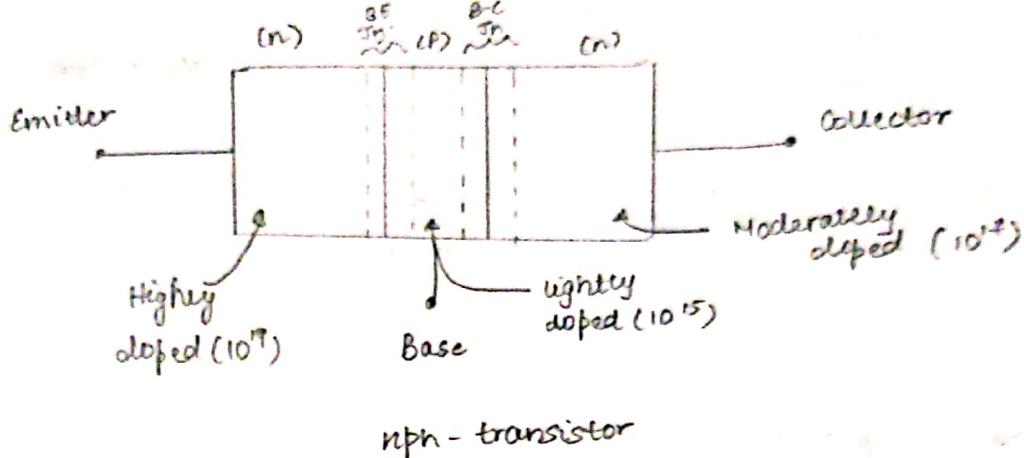


- Shows voltage shifting action, or adds a voltage, so that $V_M - V_r$ the output voltage shifts up or shifts down, and that added voltage is called off-set voltage.
- During +ve half cycle, capacitor is getting charged, and $V_M - V_r$ is the max. the capacitor can charge
- Once diode is off, C can't charge
- The diode turns off in the -ve half cycle
- Shape, freq remains same, except that output gets shifted
- If we don't want entire waveform, to shift to -ve side, we add a battery to the diode arm.

$$\begin{aligned}
 R &= 10k\Omega \\
 C &= 47 \mu F \\
 f &= 50Hz
 \end{aligned}$$

Bipolar Junction Transistors (BJT)

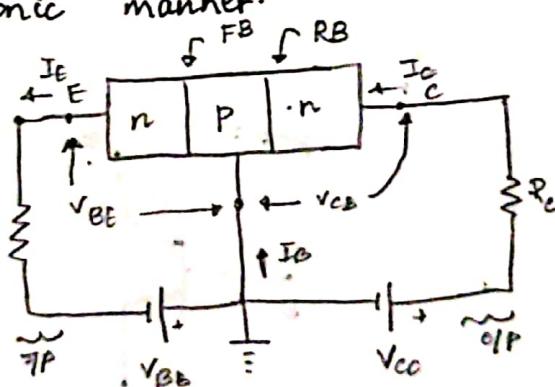
- Transistor is a three terminal device.
- Bipolar, is in the sense that there are two polarating currents, hole and e^- current. There are two p-n jn.
- Transistor means transfer of resistance



- pnp, Base acts like a cathode and other two as anode.
- npn, Base acts like anode and other two as cathode.

a) BJT Biasing

Biasing means making the transistor work in a certain electrical, electronic manner.



$$\rightarrow I_C = \alpha I_E$$

α : Common-base current gain \rightarrow const. no., $\alpha \leq 1$

$$i_B = \alpha I_E$$

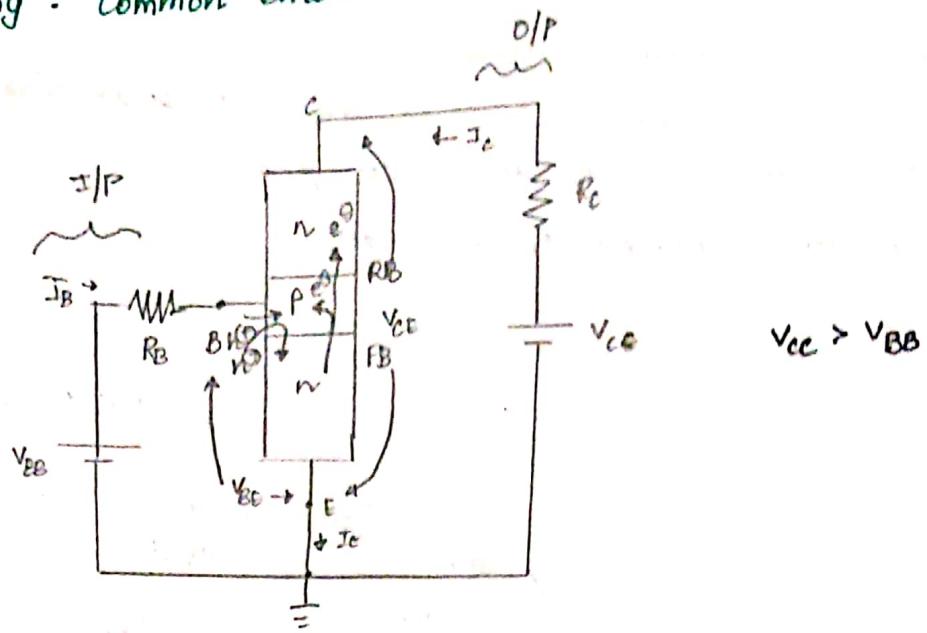
AC current

$$i_B = I_{EO} \left[e^{\frac{(V_{BE}/V_T)}{-1}} \right]$$

$$I_{EO} \rightarrow 10^{-12} \text{ to } 10^{-15} \text{ A}$$

leakage
current
if emitter
base jn is
off.

5) BJT Biasing : Common emitter (CE)



$$\rightarrow i_c = \beta i_b, \quad \beta \gg 1$$

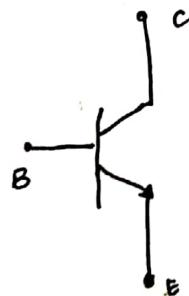
\hookrightarrow CE current gain.

$$\rightarrow i_e = i_c + i_b = (1 + \beta) i_b, \quad \alpha = \frac{\beta}{1 + \beta}, \quad \beta = \frac{\alpha}{1 - \alpha}$$

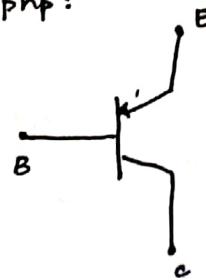
$$i_c = \left(\frac{\beta}{1 + \beta} \right) i_e$$

c) BJT Symbols

npn:



pnp:



7) a) Transistor modes of operation :

- Common base (CB)
- Common emitter (CE)
- common collector (CC)

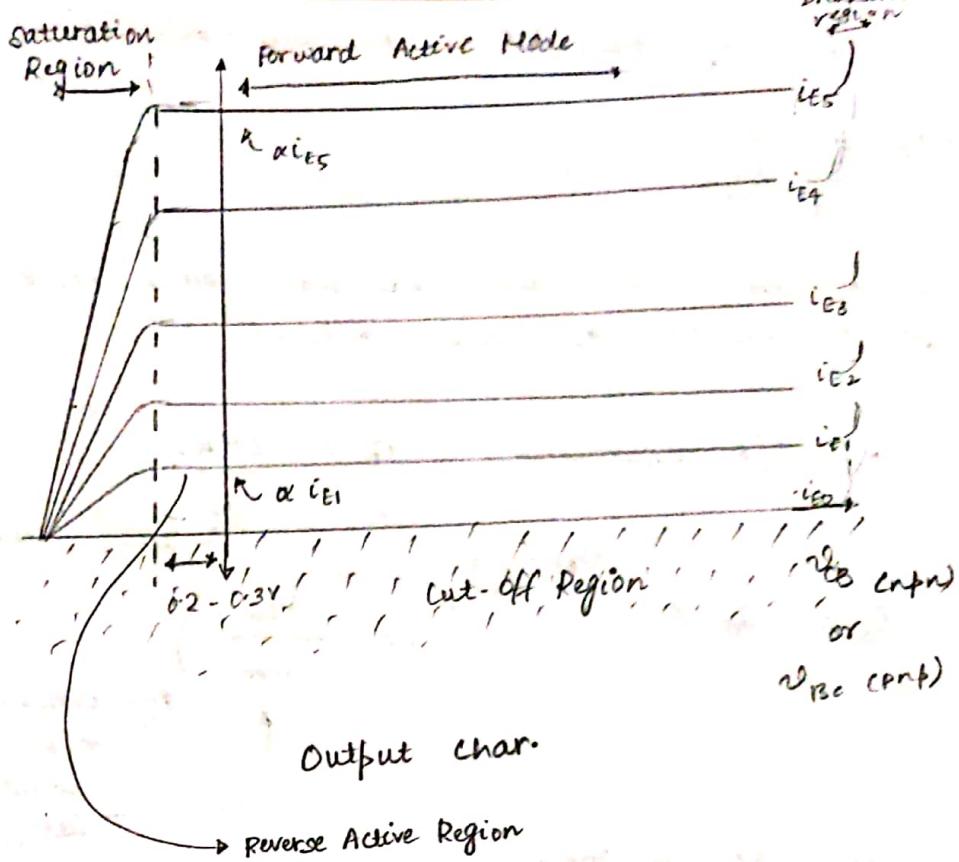
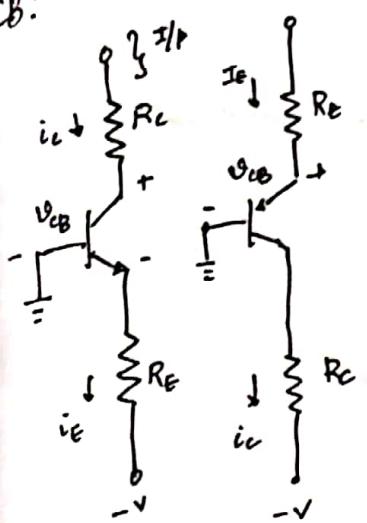
b) Transistor regions of operation

- Cut-off switch (off-switch)
- Saturation (resistor-like)
- Active → Reverse (special resistor)
- Forward ON with resistance

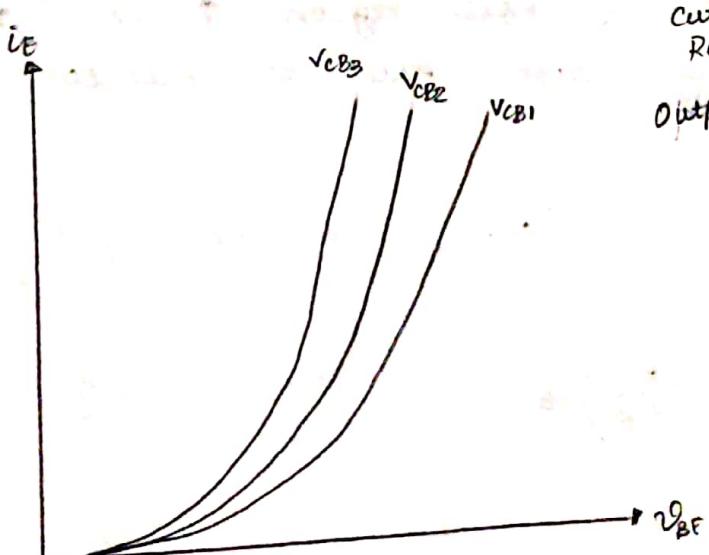
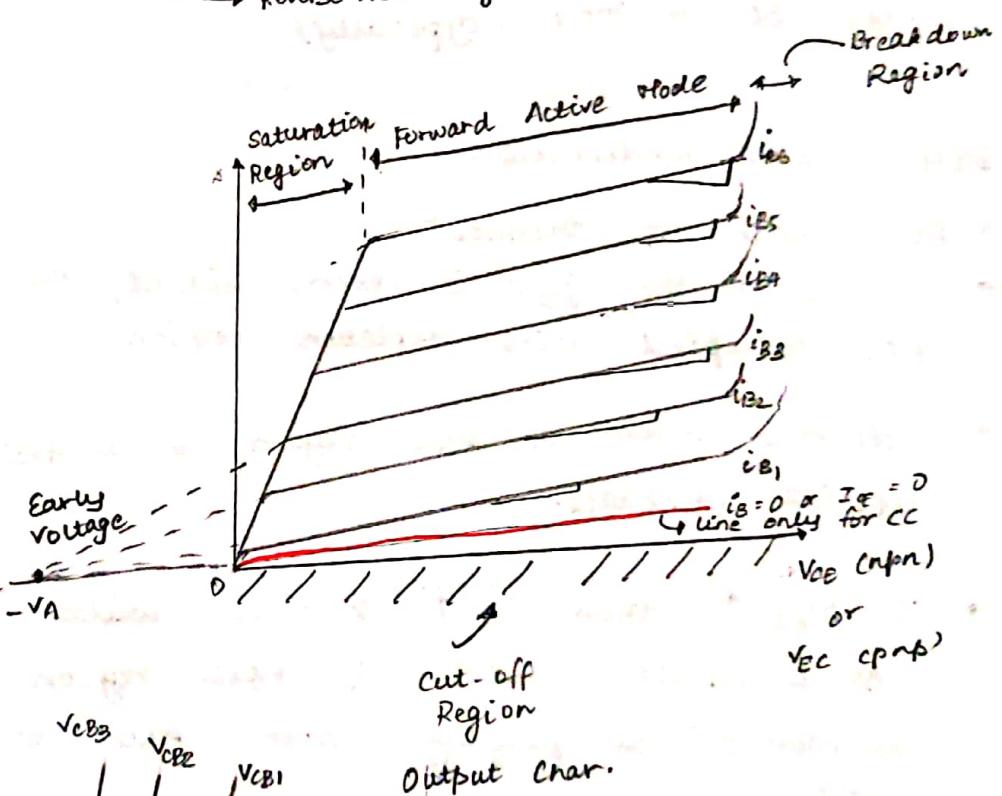
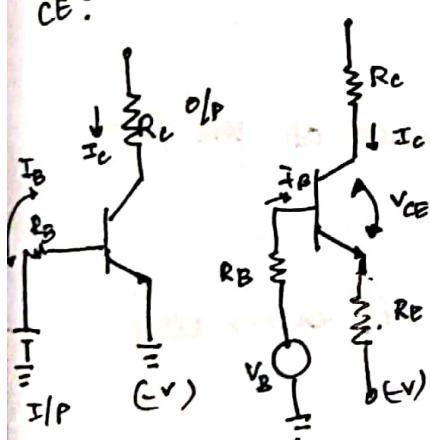
→ Breakdown region
(Permanent damage)

VI characteristics

CB:



CE:



$$V_{CB3} > V_{CB2} > V_{CB1}$$

Input Charact.

$$\text{slope} = \frac{\Delta i_c}{\Delta V_{CE}} = \frac{1}{r_o}$$

→ When the lines are extended backward, they meet at a point, known as early voltage

$$r_o : \text{o/p resistance} \quad r_o = \frac{|V_A|}{I_C} \quad |V_A| \text{ inst. current}$$

$$i_c = I_S e^{(\frac{V_{BE}}{V_T})} \left(1 + \frac{V_{CE}}{V_A} \right)$$

when early effect is considered
early voltage

$$|V_A| = 50 \text{ to } 300 \text{ v (typically)}$$

Base width modulation

- Base width is thinnest
- If one of the jn's is reverse biased, the most of the part gets occupied with depletion region.
- Effective width of base region is a fn. of externally applied voltages.
- If $V_{BE} \uparrow$, then $i_B \uparrow \Rightarrow$ Junc. width (CB) \downarrow
As a result width of base region $\uparrow \Rightarrow i_C \uparrow$
as more e^Q as passing from base to collector region.

q) I-V relationships in active region: (low to med-freq.)

$$i_E = i_C + i_B = (1 + \beta) i_B$$

$$i_C = \beta i_B = \alpha i_E = \left(\frac{\beta}{1 + \beta} \right) i_E$$

$$\alpha = \frac{\beta}{1 + \beta}$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

for npn

$$i_c = I_s e^{v_{CE}/2\theta_T}$$

$$i_E = \frac{i_c}{\alpha} = \frac{I_s e^{v_{BE}/2\theta_T}}{\alpha}$$

$$i_B = \frac{i_c}{\beta} = \frac{I_s e^{v_{BE}/2\theta_T}}{\beta}$$

for pnp

$$i_c = I_s e^{v_{CE}/2\theta_T}$$

$$i_E = \frac{i_c}{\alpha} = \frac{I_s e^{v_{CE}/2\theta_T}}{\alpha}$$

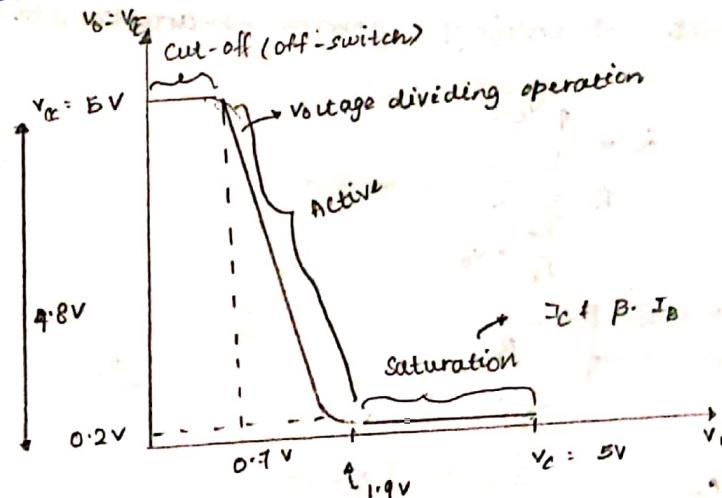
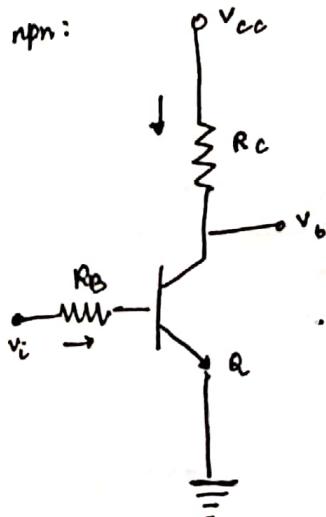
$$i_B = \frac{i_c}{\beta} = \frac{I_s e^{v_{EB}/2\theta_T}}{\beta}$$

These eqn's are without considering early effect

In load line, $I_B = \frac{V_B - V_{BE}}{R_B}$, $I_C = \frac{V_{CC} - V_{CE}}{R_C}$, $V_{CE} = V_{CC} - I_C R_C$

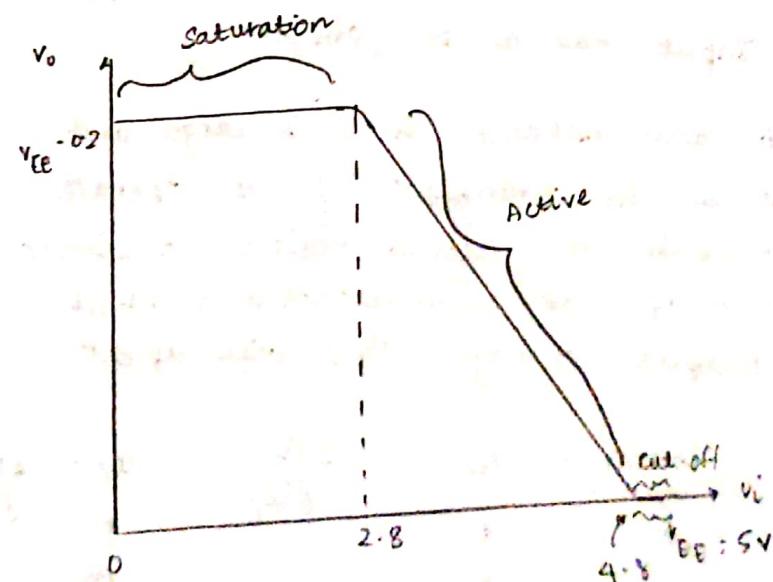
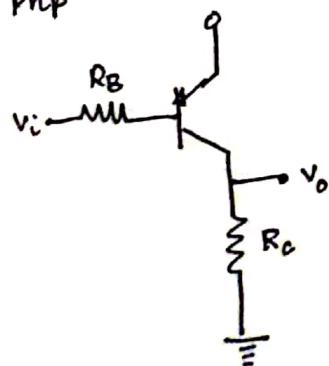
ii) Voltage Transfer Characteristics : CE

npn:



Transfer char. b/w input v and output voltage

pnp

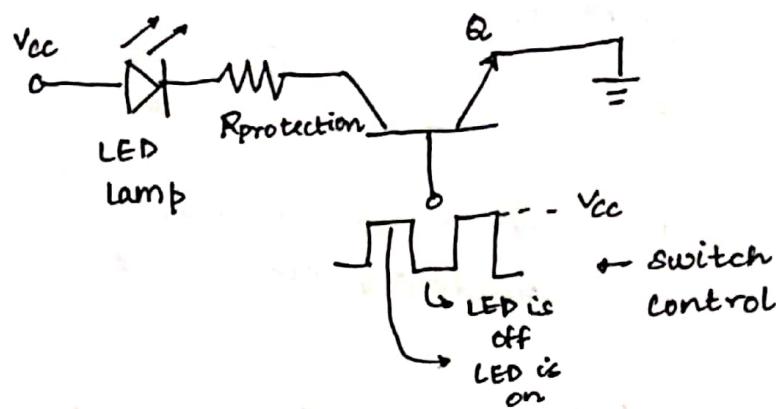


2) BJT applications:

a) Switch : 'R_e' is replaced by a load (e.g. an LED)

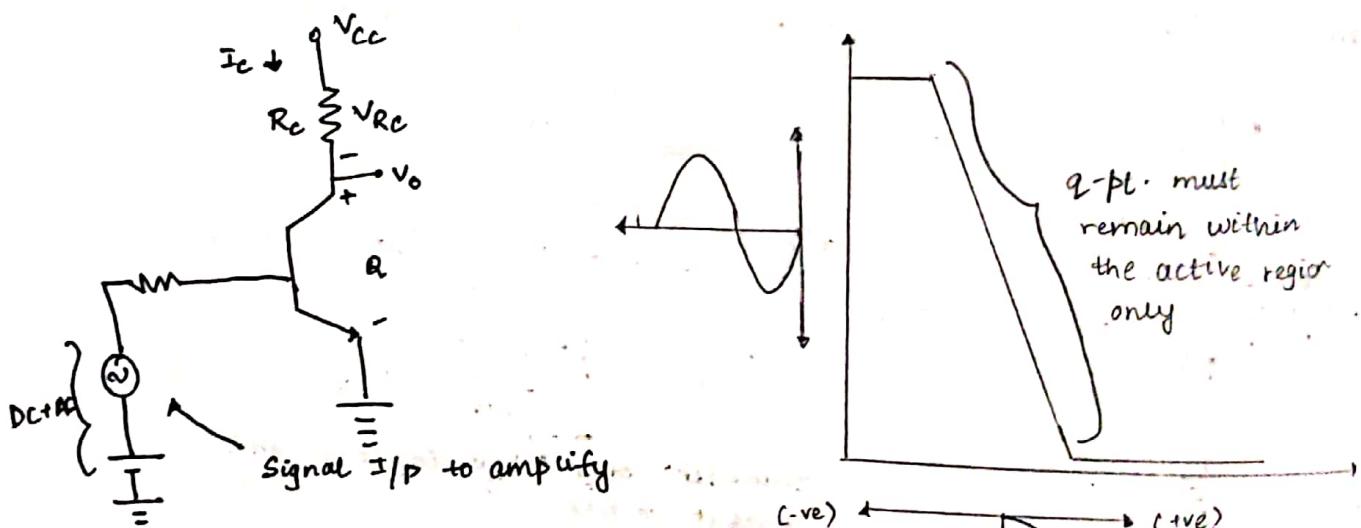
pnp/npn : 'cut-off' means OFF switch 'Q'

'saturation' means ON switch 'Q'



b) Amplifier : CE

Amplifier increases input signal to a larger output signal without changing some characteristics



Input has a DC offset

For any instance, if v_i is large and forces the transistor Q to operate outside the active region (to either cut-off or saturation) a clipped output voltage (v_o) will appear

$$\text{Gain} : \text{Av} = \frac{\Delta v_o}{\Delta v_i}$$

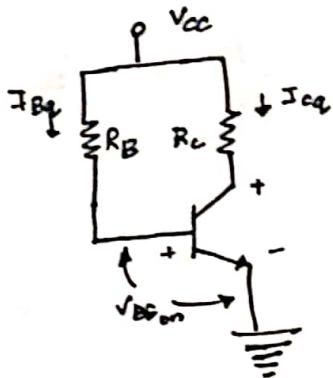
↑ DC ↑ AC

$$\text{av} = \frac{\Delta v_o}{\Delta v_i}$$

13) BJT biasing : CE as an amplifier (Amp.)

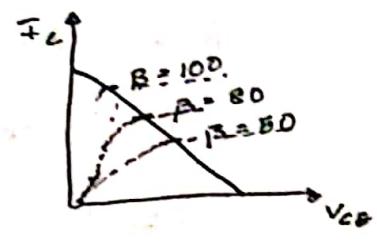
a) Single resistor biasing

→ Biasing means, selecting a q-point



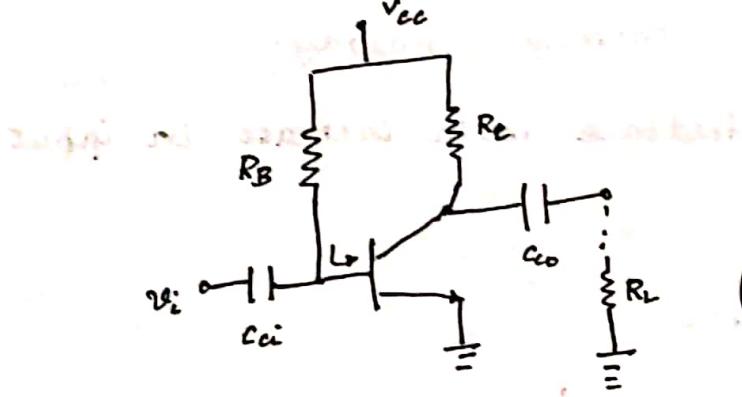
$$R_c = \frac{V_{cc} - V_{ceq}}{I_{cq}}$$

$$R_B = \frac{V_{cc} - V_{BEON}}{I_{BQ}}$$



Adjust I_{cq} and R_B such that the q-pt. is located in the forward active region (pref. at middle)

Amplifier using single resistor biasing



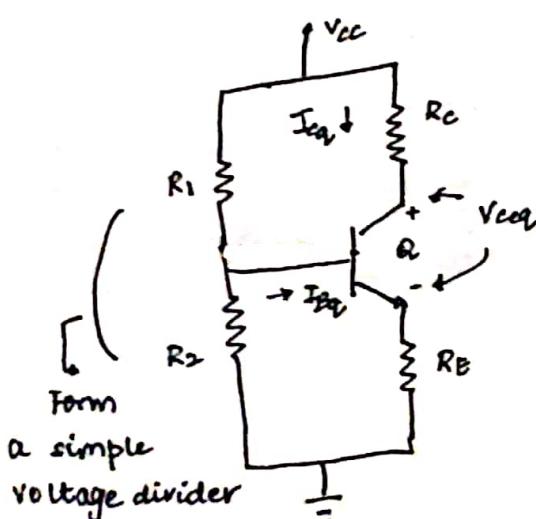
C_{ci} and C_o are I/P and O/P coupling capacitors

Coupling capacitors eliminates DC offsets at I/P and O/P

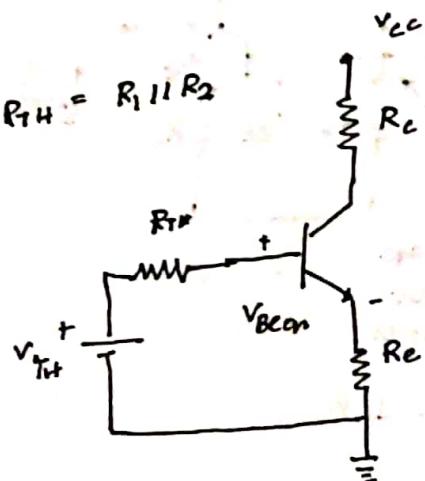
To maintain I_{cq} when no AC signal is present.

Drawback : Bias instability due to temp. change.

b) Voltage / Resistor divider biasing:



$$R_{TH} = R_1 // R_2$$



Thévenin's eq.
base driving ckt.

Improved bias stability due to temp. change. Ratiometric connection of R_1 and R_2 reduces the change in V_{TH} and R_{TH} which helps in improving bias stability with temp. variation.

$$R_{TH} = R_1 // R_2 \approx (1 + \beta) 0.1 R_E$$

$$V_{TH} = I_{BQ} \cdot R_{TH} + V_{BEon} + I_{EQ} R_E \approx \frac{R_2}{R_1 + R_2} \cdot V_{CC}$$

$$I_{EQ} = (1 + \beta) I_{BQ}$$

$$I_{CQ} = \beta I_{BQ} \approx \frac{V_{TH} - V_{BEon}}{R_E}$$

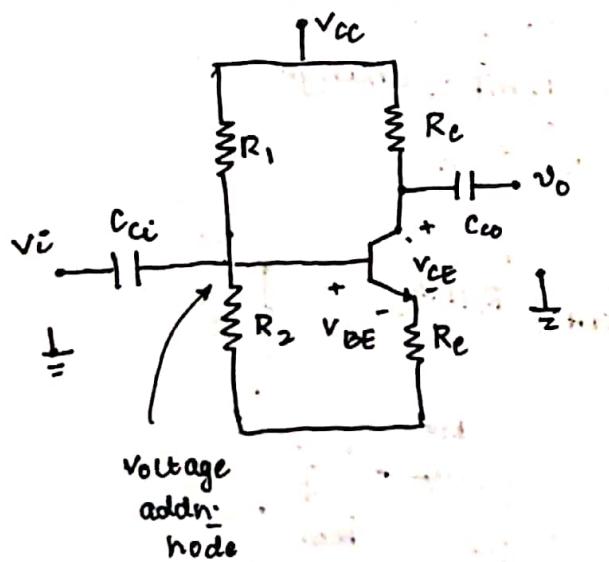
$$V_{CEQ} = V_{CC} - I_{CQ} R_C - I_{EQ} \cdot R_E$$

Adjust R_1 and R_2 and V_{CC} such that q-point lies at the middle of forward active region.

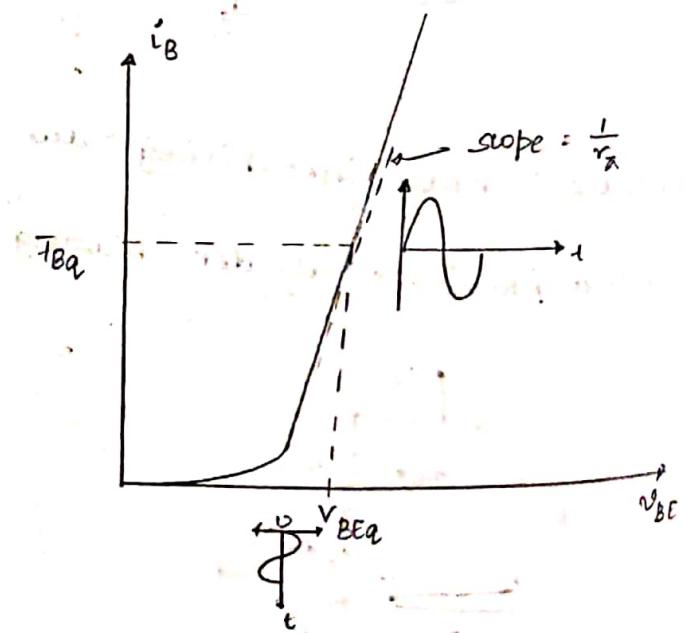
Purpose of R_E : ① V-drop additional to V_{BEon} in base ckt.
② Prevent thermal runaway.

R_E provides a negative feedback with increase in input cond. (I_B and V_{BE})

Amplifier using r-divider bias.

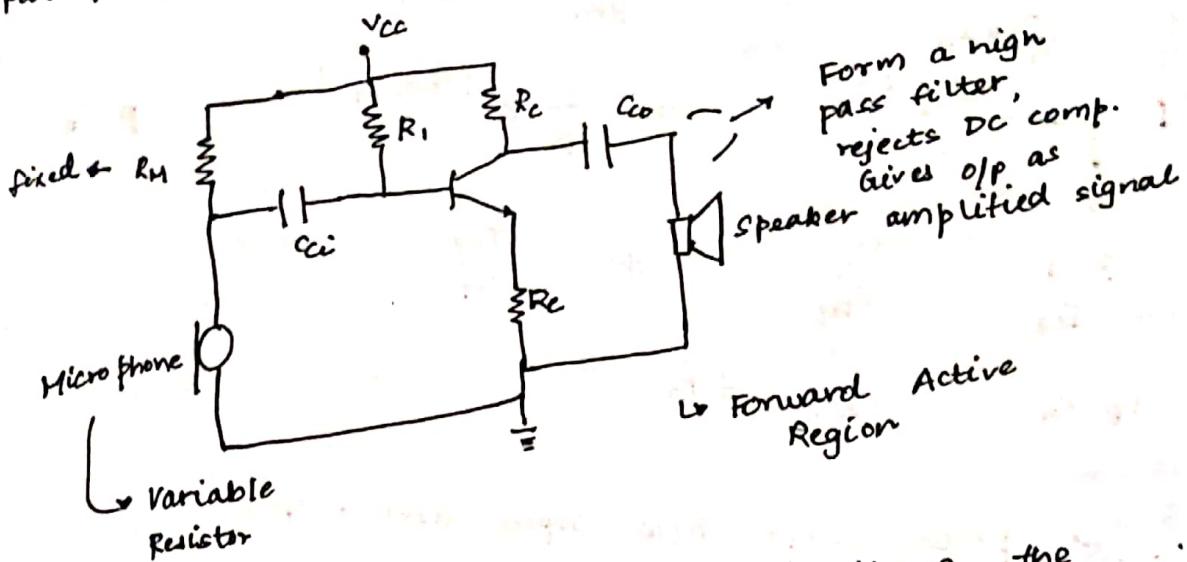


$$V_o = V_{CC} - I_C R_C$$



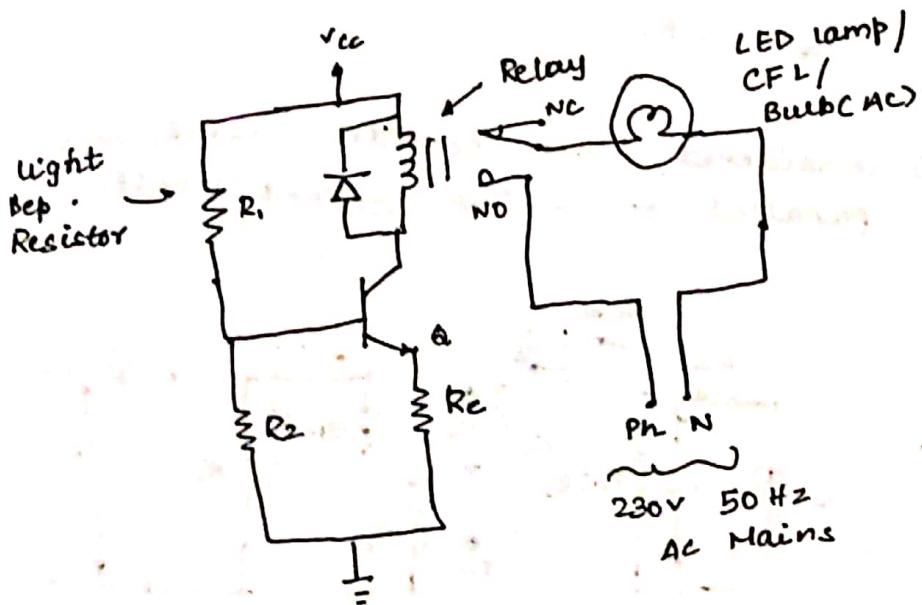
4) Applications of V-divider bias based CE Amplifier

① Microphone amplifier



Under dc cond., i.e. no sound in microphone, the C_{ci} will reject it.

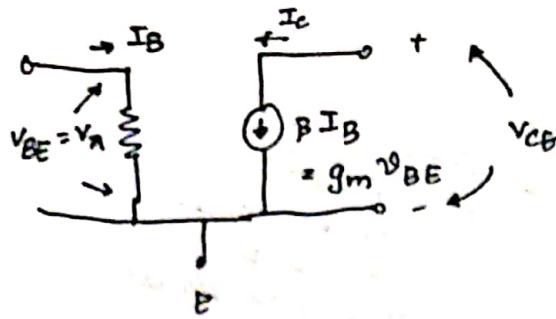
② Automatic street light controller:



NC: Normally closed
NO: Normally open
D: Free-wheeling diode

If we shine light, R_1 + when light shines on R_1 , there is reduced resistance, so now across R_2 , upper terminal of R_2 , the voltage is large enough, to turn on the transistor,

15) Small signal Hybrid π eq. circuit : CE



r_A : Diffusion resistance

g_m : Trans conductance

$$i_B = \frac{I_C}{\beta} e^{(V_{BE}/V_T)} ; i_C = \beta i_B$$

$$r_A = \frac{\beta V_T}{I_C q} = \frac{V_T}{I_{BQ}} , g_m = \frac{I_C q}{V_T}$$

$$V_{BE} = i_B r_A , r_A g_m = \beta$$

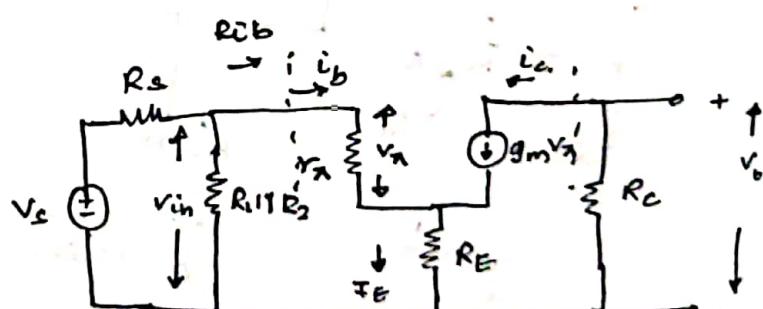
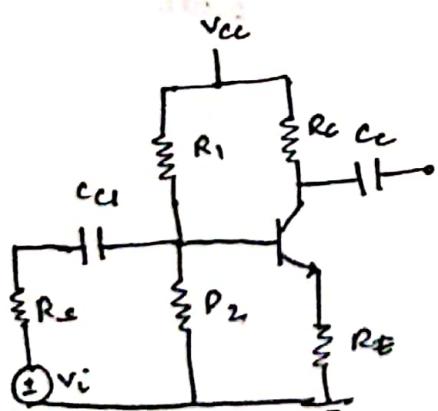
There is 180° phase shift b/w input and output

$$A_v = \frac{V_o}{V_i} = - g_m V_A R_C$$

$$V_A = \frac{r_A}{r_A + R_B} V_i \Rightarrow A_v = - \frac{\beta R_C}{r_A + R_B}$$

$$i_B = \frac{V_i}{r_A + R_B} , V_{CE} = - i_C R_C$$

If early voltage is considered, then consider ' $r_0 || R_C$ ' if r_0 is connected parallel to g_m of current source



$$V_o = - \beta I_B R_C = - I_C R_C$$

$$V_{in} = I_B r_A + (I_B + \beta I_B) R_E$$

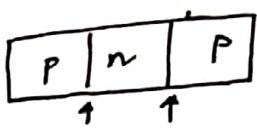
$$R_{IB} = \frac{V_{in}}{I_B} = r_A + (1+\beta) R_E$$

$$R_L = R_1 || R_2 || R_{IB}$$

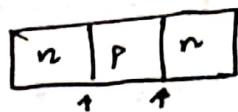
$$V_{in} = \frac{R_i}{R_i + R_S} \times V_i$$

$$\begin{aligned} A_v &= \frac{V_o}{V_i} \\ &= - \frac{\beta \cdot R_C}{r_A + (1+\beta) R_E} \left(\frac{R_i}{R_i + R_S} \right) \\ &\approx - \frac{R_C}{R_E} \end{aligned}$$

Bipolar Jn. Transistor (BJT)

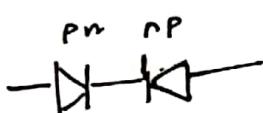


pnp bipolar
Transistor

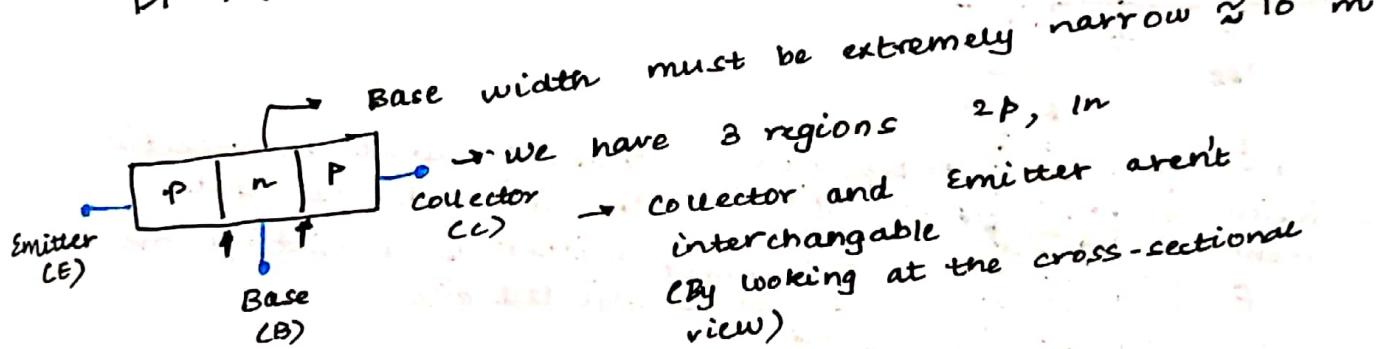


npn bipolar
Transistor

A transistor (BJT) is an semiconductor device having two P-n junctions.



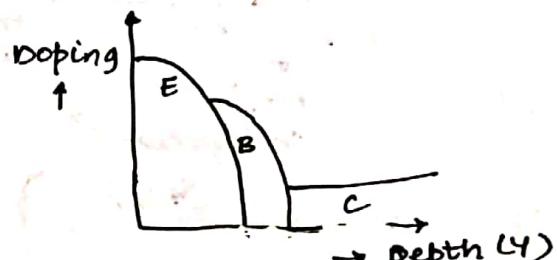
→ This won't be a transistor, as there are certain criteria for a BJT



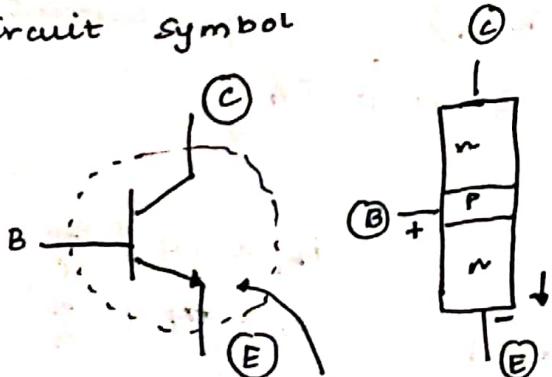
① Area of E and C

② Doping conc.

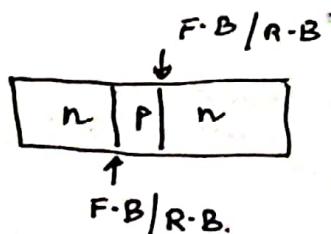
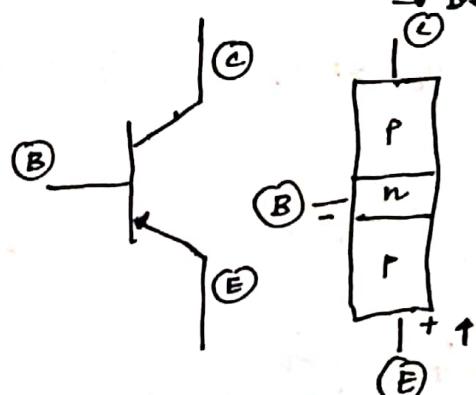
↳ Emitter region is doped heavily.



circuit symbol

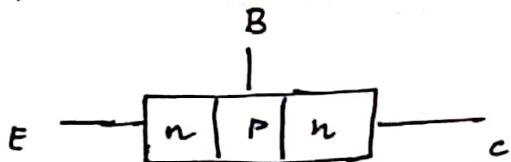


Emitter terminal has arrow
And the arrow indicates direction of flow of current.



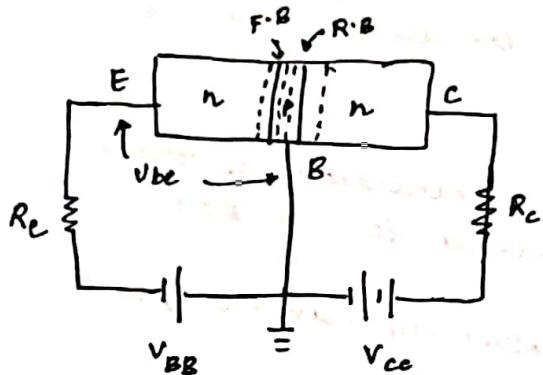
⇒ Four modes are possible

For Amplifier,

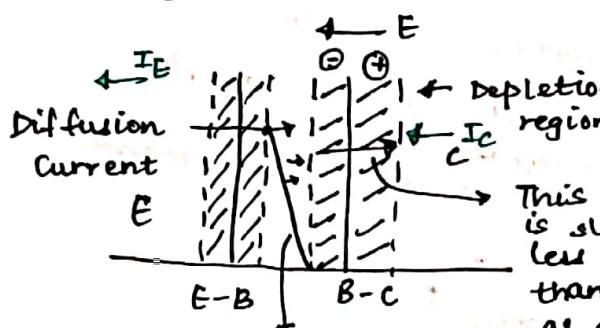


E-B \rightarrow Forward Bias

C-B \rightarrow Reverse Bias



no. of e^- s emitted from E to B is much higher than holes from p as, n of E is highly doped



Collector will be collecting the injected e^- s and.

This current is slightly injected e^- s less here than before as e^- are opp. to e^- field

$$V_{BE} > 0$$

Profile of injected e^-

$$i_E = I_{EO} \left[e^{\left(\frac{V_{BE}}{V_T} \right)} - 1 \right]$$

$$\text{If } V_{BE} \gg V_T, i_E = I_{EO} e^{\left(\frac{V_{BE}}{V_T} \right)}$$

$\hookrightarrow 10^{-12} A \text{ to } 10^{-15} A$

} Emitter current

$$i_C \propto e^{\left(\frac{V_{BE}}{V_T} \right)}, i_C \propto i_E$$

$$\therefore i_C = \alpha i_E$$

\hookrightarrow current gain

$$\kappa = \frac{i_C}{i_E}$$

common base current gain

$$i_B_1 \propto \exp\left(\frac{V_{BE}}{V_T}\right)$$

$$i_B_2 \propto \exp\left(\frac{V_{BE}}{V_T}\right)$$

$$i_B = i_B_1 + i_B_2 \propto \exp\left(\frac{V_{BE}}{V_T}\right)$$

$$i_C = \beta i_B$$

\hookrightarrow common emitter current gain

$$50 < \beta < 300$$

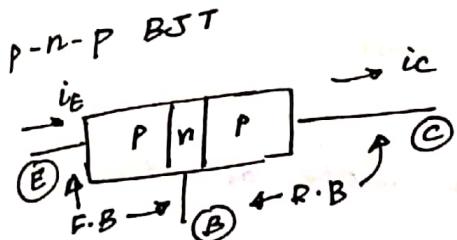
$$\begin{aligned} i_E &= i_C + i_B \\ &= \beta i_B + i_B \\ &= (1+\beta) i_B \end{aligned}$$

$$i_C = \beta i_B$$

$$i_B = \frac{i_C}{\beta} \Rightarrow i_E = \left(\frac{\beta+1}{\beta} \right) i_C$$

$$i_C = \left(\frac{\beta}{\beta+1} \right) i_E, \quad i_C = \alpha i_E$$

$$\therefore \alpha = \frac{\beta}{\beta+1}, \quad \beta = \frac{\kappa}{1-\alpha}$$



$$i_E = I_{EO} \exp \left(\frac{V_{EB}}{V_T} \right)$$

$$V_{EB} > 0$$

Imp. relations (for both n-p-n and p-n-p):

$$i_E = i_C + i_B$$

$$\beta = \frac{\kappa}{1-\alpha}$$

$$i_C = \frac{\beta}{1+\beta} i_E$$

$$i_C = \beta i_B$$

$$\kappa = \frac{\beta}{1+\beta}$$

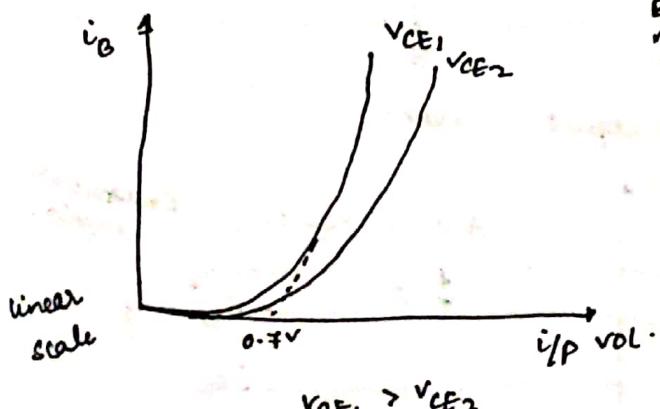
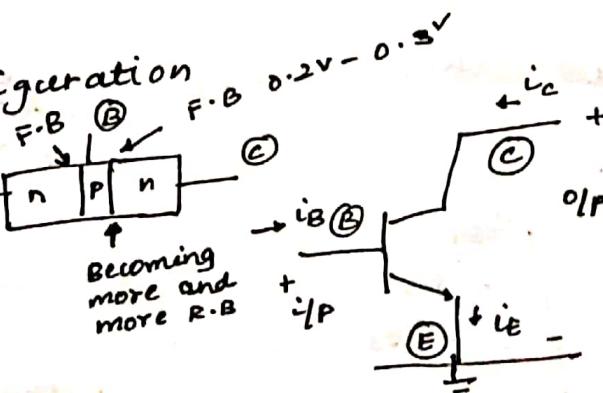
$$i_C = \alpha i_E$$

$$i_E = (1+\beta) i_B$$

only during active region

For common emitter configuration

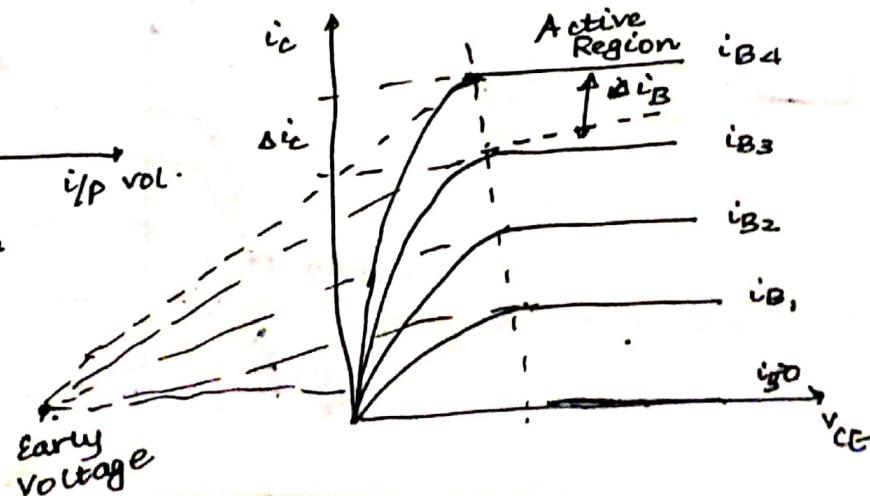
Input config. char.

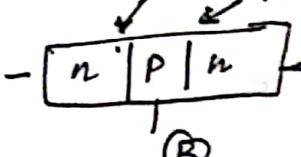


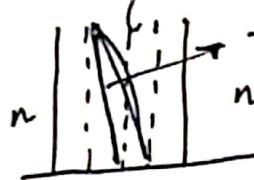
$$V_{CE1} > V_{CE2}$$

$$\beta_{ac} = \frac{\Delta i_C}{\Delta i_B}$$

$$\beta \approx \beta_{ac}$$



∴ The slope occurs as,
 As V_{CE} changes, we are changing
 R.B between p and n junction. (E) -  R.B

When V_{CE} increase
 Thus slope increases
 thereby increasing current.

Early effect

Base width modulation

$$i_c = I_s e^{(V_{BE}/V_T)} \left(1 + \frac{V_{CE}}{V_A} \right)$$

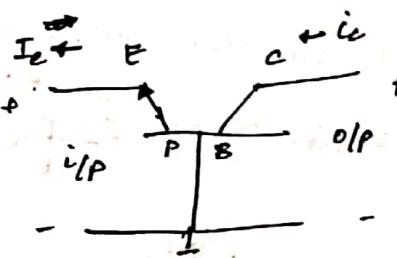
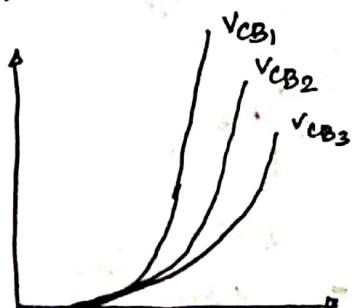
To find output resistance, we use slope of the graph.

$$\frac{di_c}{dV_{CE}} = \frac{1}{r_0} = I_s e^{(V_{BE}/V_T)} \frac{1}{V_A} = \frac{I_c}{V_A}$$

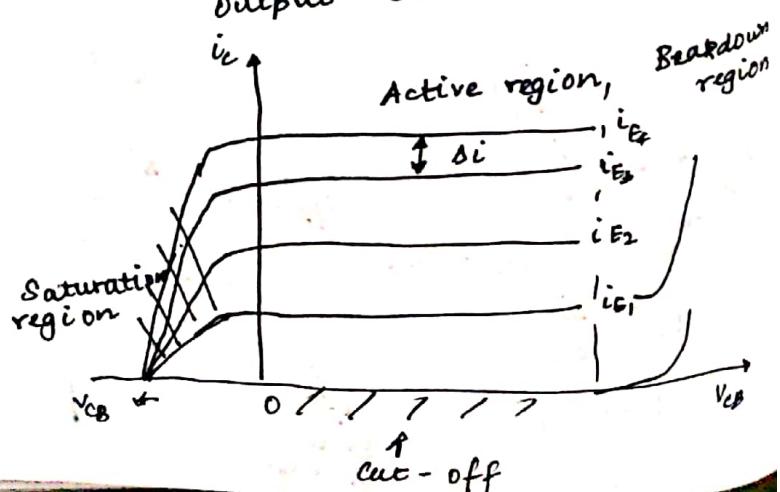
$$\therefore r_0 = \frac{V_A}{I_c}$$

Common - Base (CB)

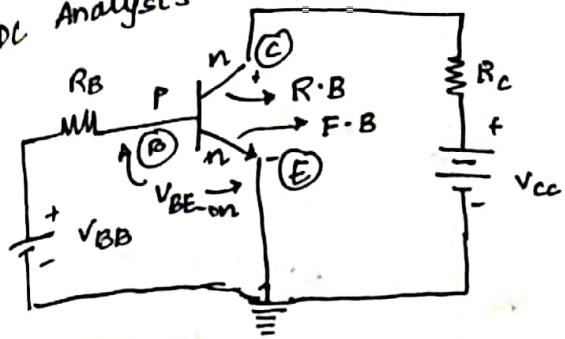
Input char.



Output char.



DC Analysis



CE circuit

$$i_B = \frac{V_{BB} - V_{BE\text{on}}}{R_B}$$

$$= \frac{V_{BB} - 0.7}{R_B}$$

(i) $V_{BB} > V_{BE\text{on}}$

Then BJT is on
⇒ i_B is finite

when the p-n junction is F-B
the voltage drop is $V_{BE\text{on}} \approx 0.7 \text{ V}$ (si)

① $V_{BB} < V_{BE\text{on}}$, BJT is off, $i_B = 0$

$$i_c = \beta i_B \text{ (Forward Active Mode)}$$

$$V_{CE} = V_{CC} - i_c R_C$$

$V_{CE} > V_{BE\text{on}}$, BC Jn. is in reverse bias

Power dissipation in BJT (P_T) = $\frac{i_B}{2} V_{BE} + \frac{i_c}{2} V_{CE}$; $\frac{i_B}{2} \ll \frac{i_c}{2}$

$$V_{CE(\text{sat})} \rightarrow 0.1 \text{ to } 0.3$$

$$B = 100, \text{ si BJT}, V_{BE\text{on}} = 0.7 \text{ V}$$

$$V_{CE(\text{sat})} = 0.2 \text{ V}$$

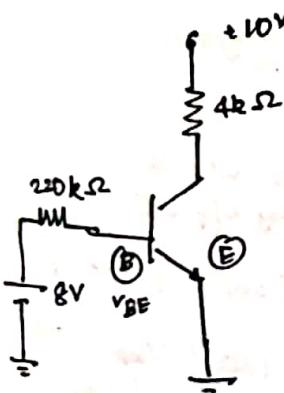
Assume, BJT is in active region

$$i_B = \frac{8 - 0.7}{220 \times 10^3} = 33.24 \mu\text{A}$$

$$i_c = B i_B = 100 \times 33.24 \mu\text{A} = 3.32 \text{ mA}$$

$$V_{CE} = V_{CC} - i_c R_C = 8 - 3.32 \times 4 = -3.28 \text{ V}$$

↳ Implies it isn't in active region.



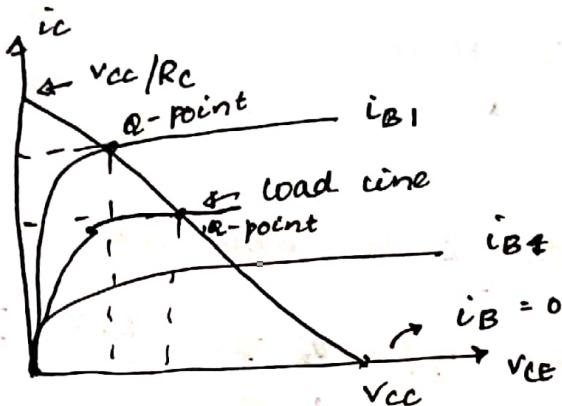
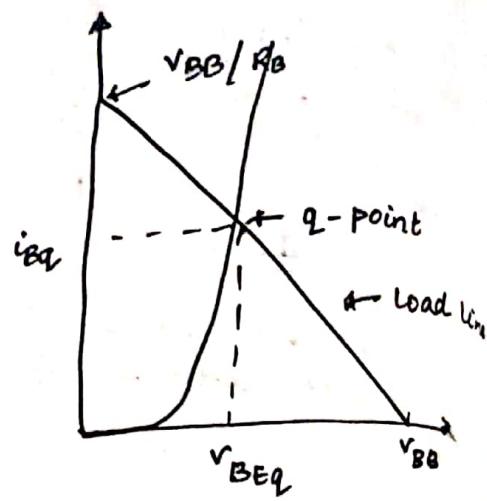
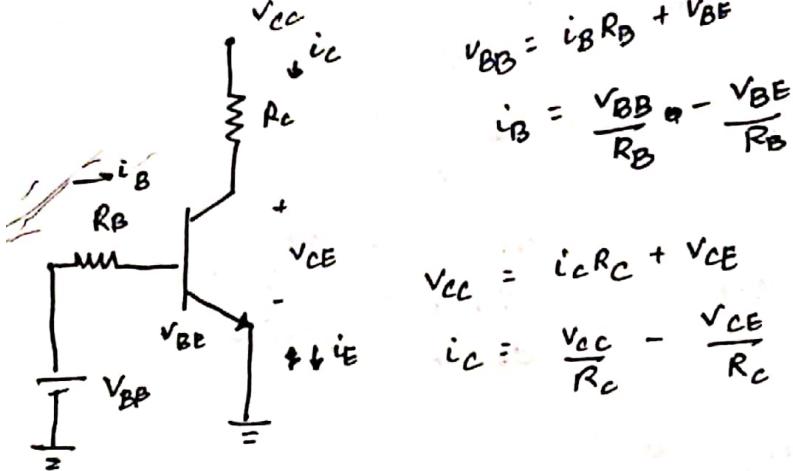
∴ It's in saturation region

It's not in cut-off region,

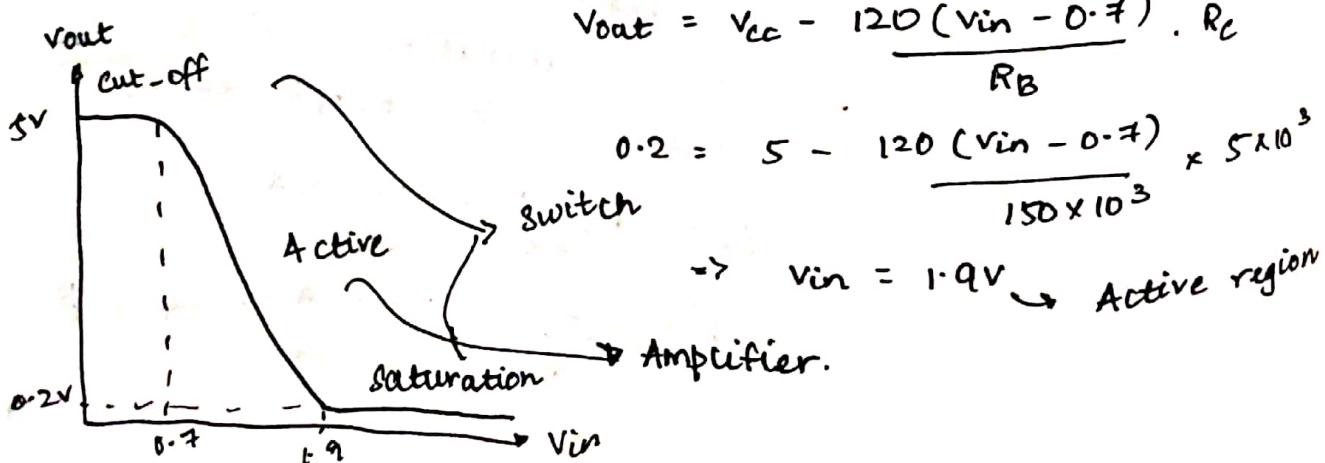
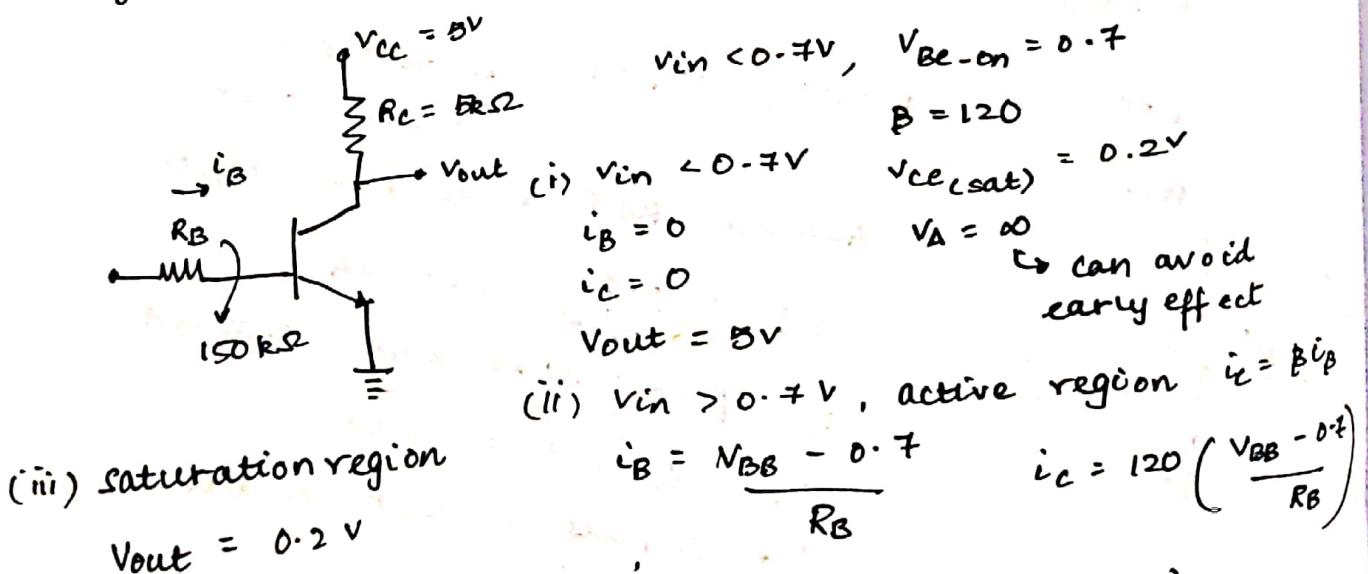
$$i_c = \frac{10 - 0.2}{4k} = 2.45 \text{ mA}$$

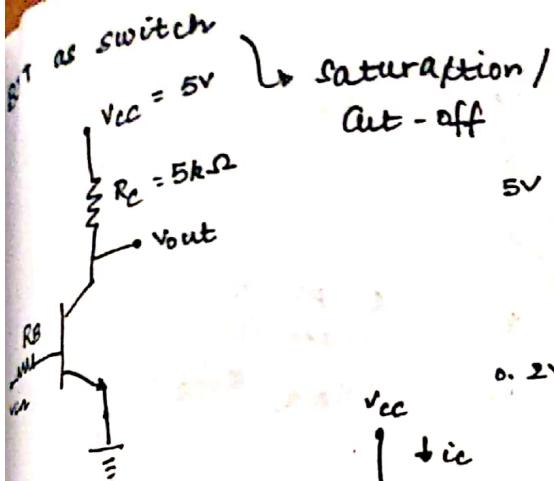
$$\beta' = \frac{i_c}{i_B} = \frac{2.45 \text{ mA}}{33.24 \mu\text{A}} \approx 74 < \beta$$

Load Line

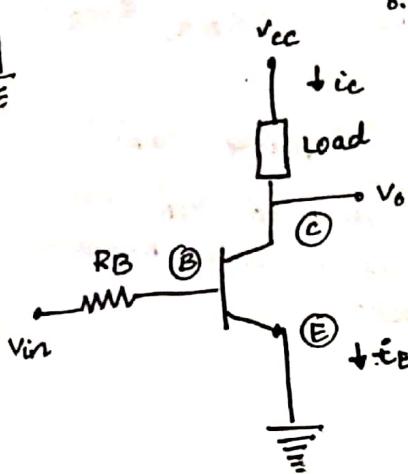
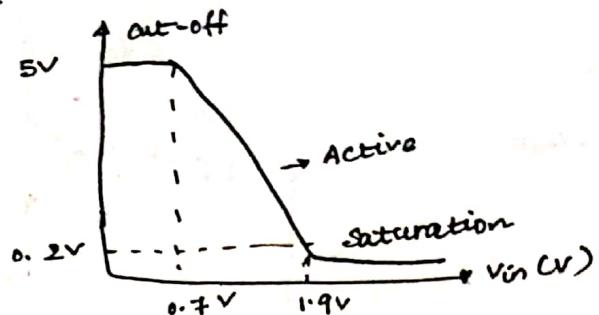


Voltage Transfer Characteristics (V_{TC})





saturation / cut-off



Electrically controlled

$v_{in} = 0V$, cut-off region

$$\Rightarrow i_B = 0 = i_C$$

$$v_o = V_{CC}$$

$v_{in} = V_{CC}$, saturation region

$$i_B = \text{finite}$$

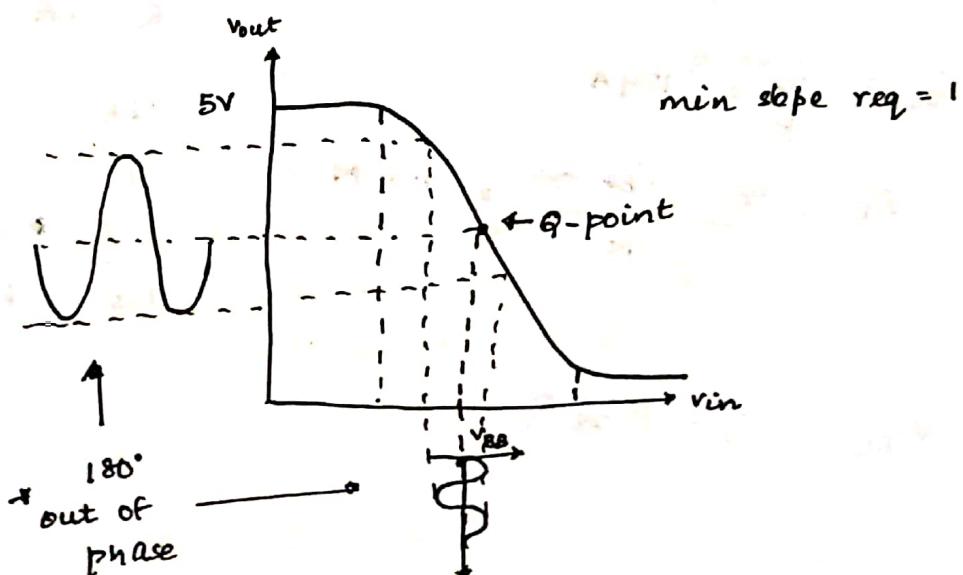
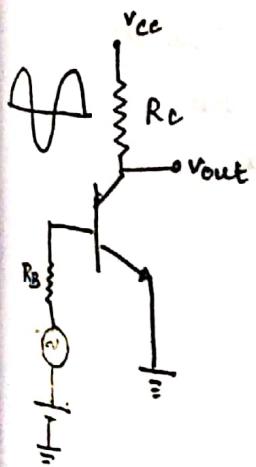
$$i_C = \text{finite}$$

$$v_o = V_{CC} - i_C R_L \approx 0.2V$$

$$i_C R_L = V_o - 0.2$$

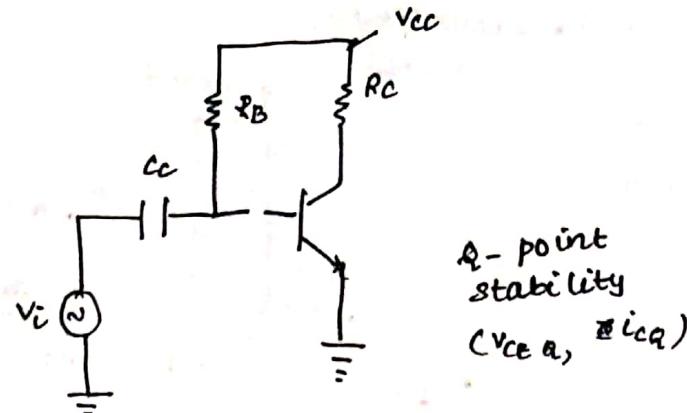
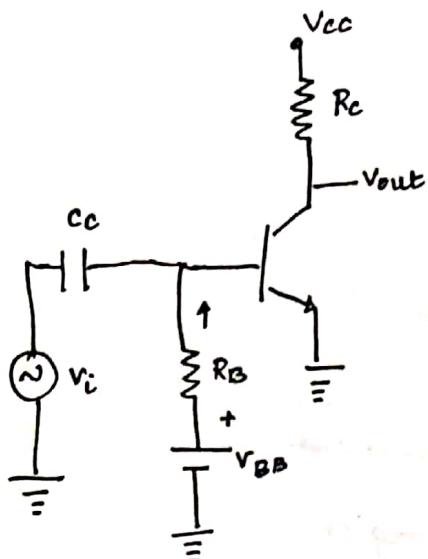
\hookrightarrow voltage drop is completely at load

BJT as Amplifier



$v_{in} \uparrow, i_B \uparrow, i_C \uparrow$, drop across $R_C \uparrow$, $v_{out} \downarrow$

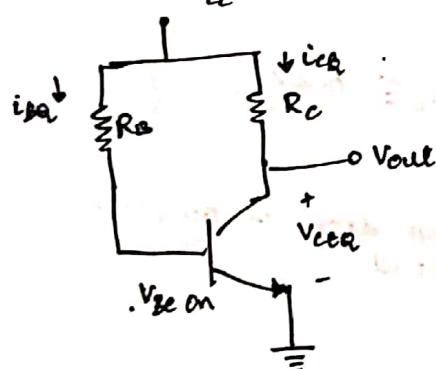
Biasing Schemes of BJT circuit



C_C is called the coupling cap.
The dc current due to V_{BB} can't cross the C_C , as C_C will behave like an open ckt.

For DC Analysis

$$V_{CC} = 12V$$



$$I_{CQ} = 1 \text{ mA}$$

$$V_{CEQ} = 6V$$

$$\beta = 100$$

$$R_B = ? , R_C = ?$$

$$V_{CEQ} = V_{CC} - i_{CQ} R_C$$

$$6 = 12 - 1 \times 10^{-3} R_C$$

$$\Rightarrow 6 \times 10^3 = R_C$$

$$R_C = 6k$$

$$i_{BQ} = \frac{i_{CQ}}{\beta} = 104 \text{ nA}$$

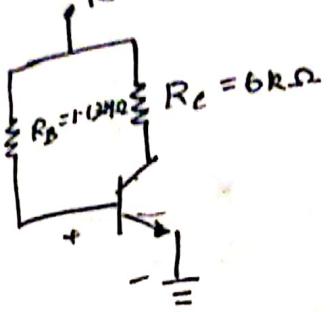
$$R_B = \frac{V_{CC} - V_{BE\text{-on}}}{i_{BQ}} = 1.13M\Omega$$

$$i_{BQ} = \frac{V_{CC} - V_{BE\text{-on}}}{R_B}$$

fixed

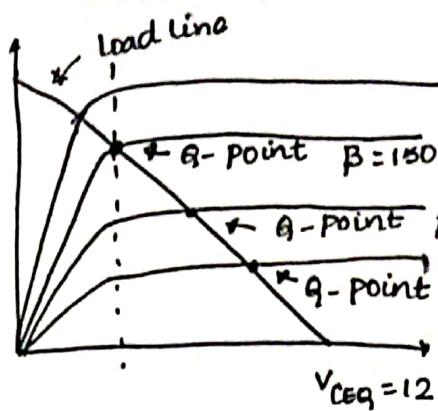
$$i_{CQ} = \beta i_{BQ}$$

$$V_{CEQ} = V_{CC} - \beta i_{BQ} R_C$$



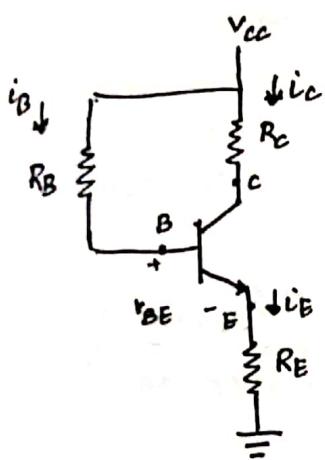
$$I_{CQ} = \beta I_{BQ} = \beta \cdot \frac{V_{CC} - V_{BE(on)}}{R_B}$$

$$V_{CEQ} = V_{CC} - I_{CQ} \cdot R_C$$



	$\beta = 50$	$\beta = 100$	$\beta = 150$
I_{CQ}	0.5	1	1.5
V_{CEQ}	9	12	3

Thus, there is no stability in Q-point. We introduce a feed back factor, resistor at emitter.



$$V_{CC} = i_B R_B + V_{BE(on)} + i_E R_E$$

$$i_E = (1+\beta) i_B$$

$$\frac{V_{CC} - V_{BE(on)}}{R_B + (1+\beta) R_E} = i_B ; \quad i_C = \beta i_B$$

$$i_C = \beta \left(\frac{V_{CC} - V_{BE(on)}}{R_B + (1+\beta) R_E} \right)$$

If $(1+\beta) R_E \gg R_B$

$$\Rightarrow i_C = \beta \left(\frac{V_{CC} - V_{BE(on)}}{(1+\beta) R_E} \right) \approx \frac{V_{CC} - V_{BE(on)}}{R_E}$$

$\therefore i_C$ becomes independent of β

$$\begin{aligned} V_{CE} &= V_{CC} - i_C R_C - i_E R_E \\ &= V_{CC} - i_C R_C - \frac{(1+\beta)}{\beta} i_C R_E \end{aligned}$$

$$= V_{CC} - i_C R_C - i_C R_E$$

$$= V_{CC} - (R_C + R_E) i_C$$

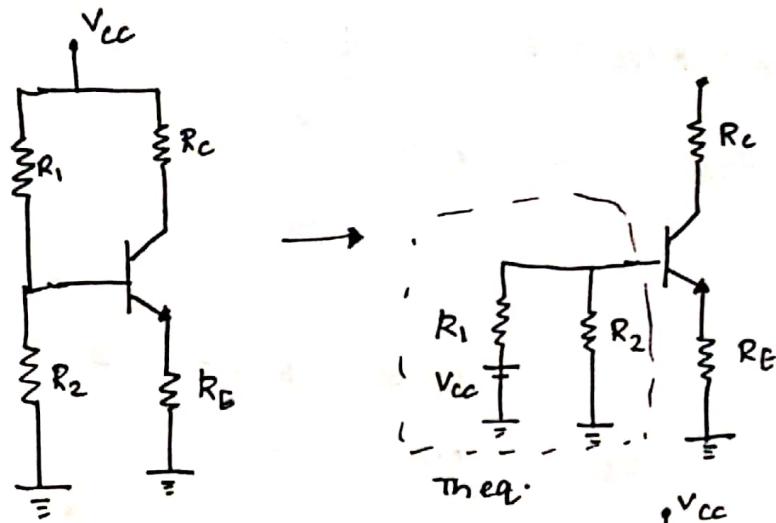
$$V_{CE} = V_{CC} - (R_C + R_E) \times \frac{V_{CC} - V_{BE(on)}}{R_E}$$

$\therefore V_{CE}$ is also independent of β

Hence the variation is significantly minimized

$i_C \uparrow, V_E \uparrow, V_{BE} \downarrow$
 $i_E \downarrow, i_B \downarrow$

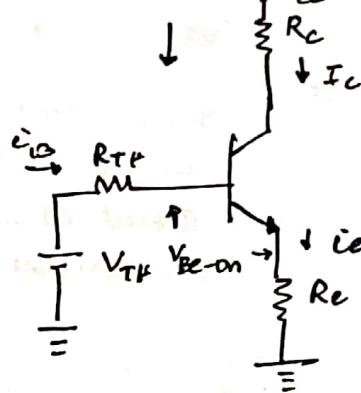
R_E is causing the negative feedback



$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

Theq.



$$V_{TH} = i_B R_{TH} + V_{BE-ON} + i_E R_E$$

$$V_{TH} = i_B R_{TH} + V_{BE-ON} + (1 + \beta) R_E i_B$$

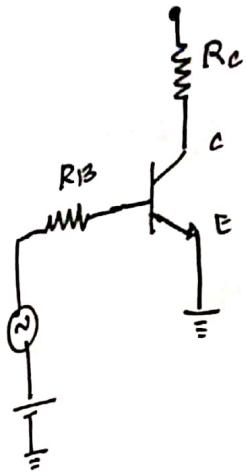
$$i_B = \frac{V_{TH} - V_{BE-ON}}{R_{TH} + (1 + \beta) R_E} ; \quad i_C = \beta \left(\frac{V_{TH} - V_{BE-ON}}{R_{TH} + (1 + \beta) R_E} \right)$$

If $R_{TH} \ll (1 + \beta) R_E$

$$i_C = \frac{V_{TH} - V_{BE}}{R_E} \quad \text{Again independent of } \beta$$

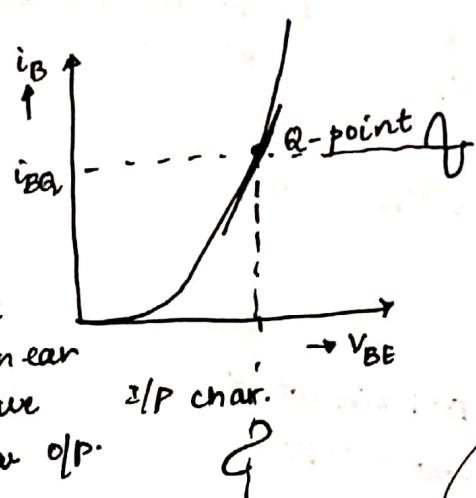
Similarly V_{CE} is independent of β

BJT Amplifiers



i_b, i_c are in same phase
 $i/p, o/p 180^\circ$ phase shift
 v_s should be small signal

thus, even though we have used a non-linear device, now we have a linear o/p.
 (Superposition, Thevenin etc. can be applied)



$$i_b \propto \exp\left(\frac{V_{BE}}{V_T}\right)$$

If signal is small, then change in i_{bQ} is linearly varying with V_{BE}

i_b is linearly related with input $\Rightarrow i_c$ is also linearly related

$$v_{out} = V_{CE} - i_c R_C$$

v_{out}

$$(V_{BE}/V_T)$$

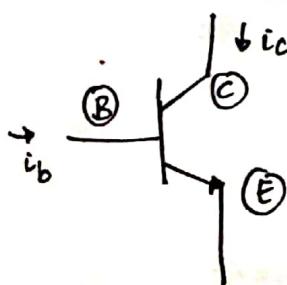
$$i_c = I_s e^{(V_{BE}/V_T)}$$

$$i_b = \frac{I_s}{\beta} e^{(V_{BE}/V_T)}$$

$$\frac{1}{r_\pi} = \frac{\partial i_b}{\partial V_{BE}} \Big|_{Q\text{-pt.}} = \frac{I_{bQ}}{V_T} = \frac{I_{cQ}}{\beta V_T}$$

$$r_\pi = \frac{V_T}{I_{cQ}}$$

diffusion resistance / base-emitter input resistance

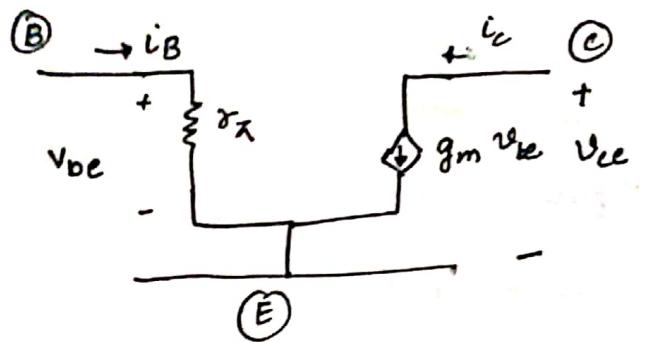


$$\Delta i_c = \frac{\partial i_c}{\partial V_{BE}} \Big|_{Q\text{-pt.}}$$

$$\frac{\partial i_c}{\partial V_{BE}} \Big|_{Q\text{-pt.}} = \frac{I_{cQ}}{V_T}$$

Trans conductance (g_m)

$$g_m = \frac{I_{cQ}}{V_T}$$

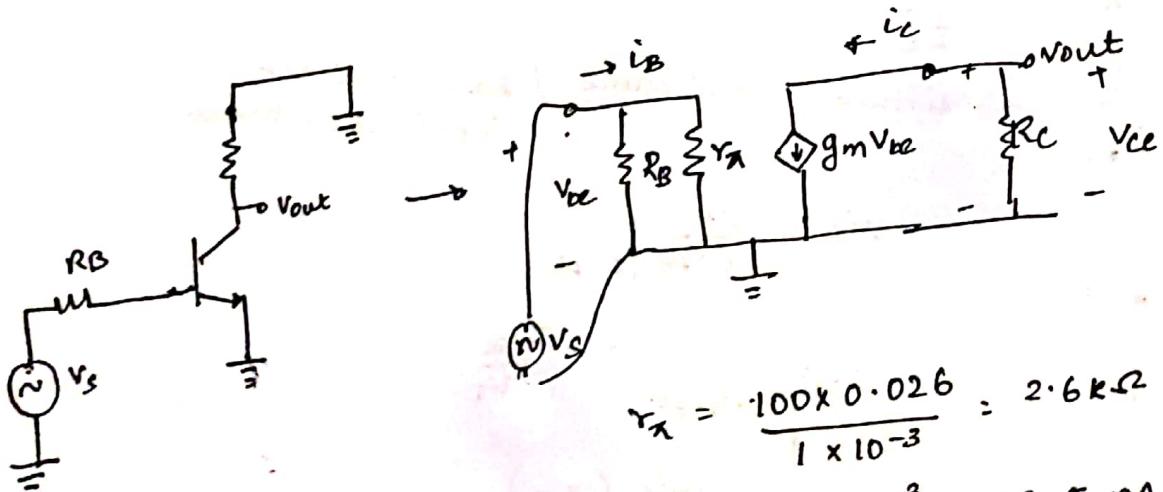
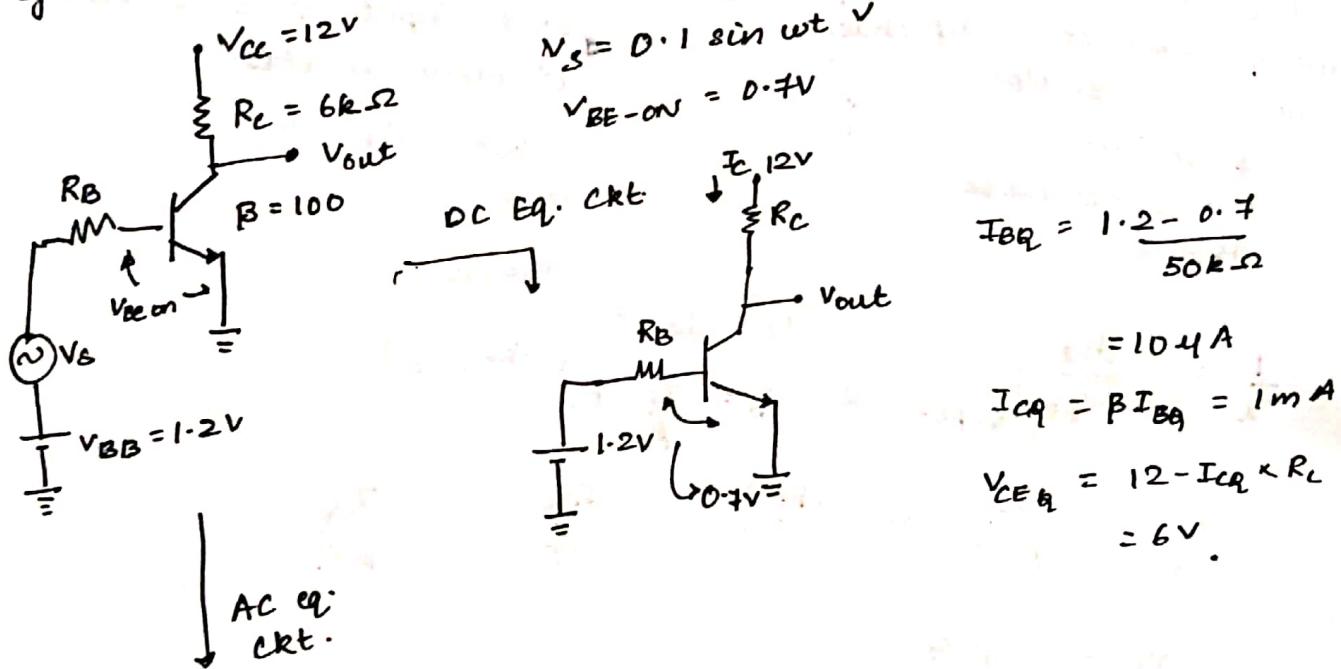


small signal eq. w.r.t. v_{be}
of BJT
(OR)
small signal hybrid π
eq. ckt.

$$r_A = \frac{B V_T}{I_{CQ}} \quad g_m = \frac{I_{CQ}}{V_T} \quad \left. \begin{array}{l} \text{Q-point DC biasing} \\ \text{point.} \end{array} \right\}$$

$$r_A \times g_m = B \quad , \quad g_m \cdot v_{be} = B i_b$$

Eg:-



$$r_A = \frac{100 \times 0.026}{1 \times 10^{-3}} = 2.6 \text{ k}\Omega$$

$$g_m = \frac{1 \times 10^{-3}}{0.026} = 38.5 \text{ mA/V}$$

$$\text{Gain} = \frac{V_{out}}{V_s}$$

$$v_{be} = \frac{r_A}{R_B + r_A} \times v_s$$

$$v_{be} = -g_m v_{be} R_C$$

$$v_{be} = -g_m R_C \cdot \frac{r_A}{R_B + r_A} \cdot v_s$$

=

$$\text{Gain} = \frac{V_{out}}{V_s} = -g_m R_C \frac{r_A}{R_B + r_A}$$

$$= -38.5 \times 10^{-3} \times 6 \times 10^3 \times \frac{2.6}{2.6 + 50} = -11.4$$

\uparrow
180° phase shift

$$i_b = \frac{V_s}{R_B + r_A} = 1.90 \sin \omega t \text{ mA}$$

$$i_c = \beta i_b = 0.19 \sin \omega t \text{ mA}$$

$$V_{ce} = V_{out} = -i_c R_C = -(0.19 \sin \omega t) \times 6 = -1.14 \sin \omega t$$

Harmonic Distribution

$$\exp\left(\frac{V_{be}}{V_T}\right) = \exp\left(\frac{V_m \sin \omega t}{V_T}\right) = 1 + \frac{V_m \sin \omega t}{V_T} + \frac{V_m^2 \sin^2 \omega t}{2V_T} + \frac{V_m^3 \sin^3 \omega t}{3V_T}$$

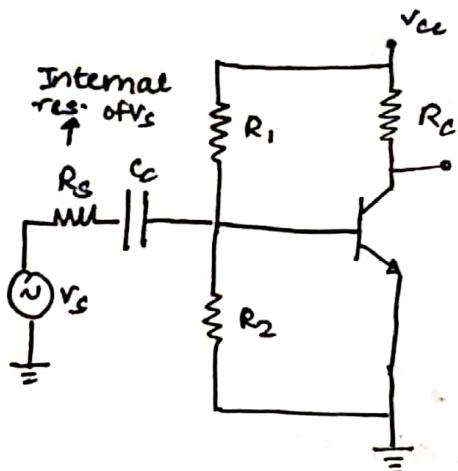
$$\sin^2 \omega t = \frac{1}{2} [1 - \sin(2\omega t + 90^\circ)]$$

$$\sin^3 \omega t = \frac{1}{4} [3 \sin \omega t - \sin 3\omega t]$$

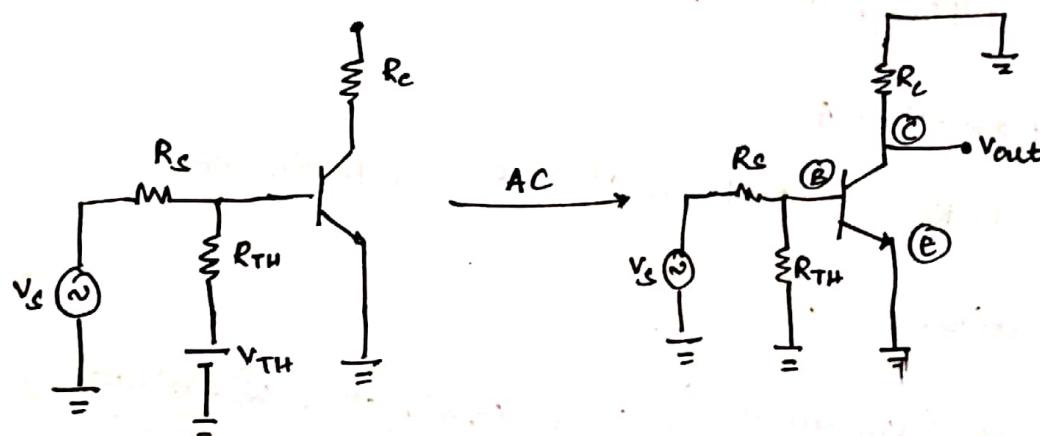
$$\begin{aligned} \exp\left(\frac{V_{be}}{V_T}\right) &= \left[1 + \frac{1}{4} \left(\frac{V_m}{V_T}\right)^2\right] + \frac{V_m}{V_T} \left[1 + \frac{1}{8} \left(\frac{V_m}{V_T}\right)^2\right] \sin \omega t \\ &\quad - \frac{1}{4} \left(\frac{V_m}{V_T}\right)^2 \sin(2\omega t + 90^\circ) \\ &\quad - \frac{1}{24} \left(\frac{V_m}{V_T}\right)^3 \sin 3\omega t \end{aligned}$$

$$\text{Total Harmonic Distortion} = \frac{\sqrt{V_2^2 + V_3^2 + \dots}}{V_1} \times 100\%$$

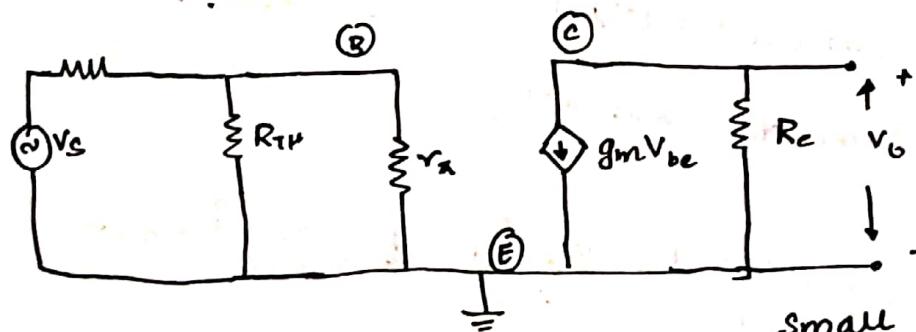
CE Amplifier circuit with voltage divider biasing :-



In case of AC analysis, C can be considered shortened (as we choose freq in such way)



$$R_{TH} = R_1 \parallel R_2$$

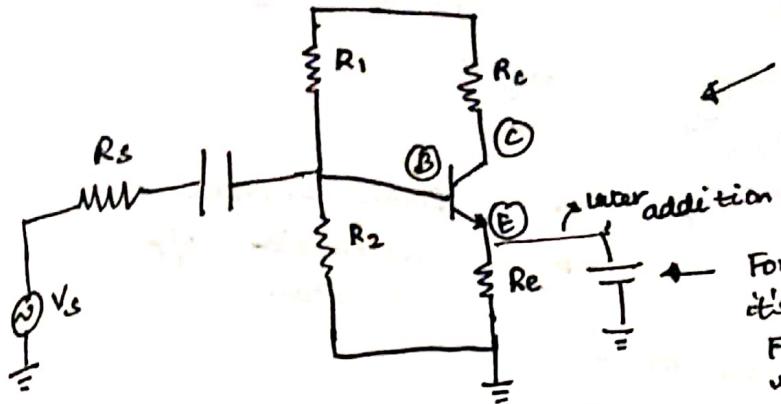


$$\text{Gain} = \frac{V_{out}}{V_s} ; \quad V_{out} = -g_m V_{be} \cdot R_C$$

$$V_{be} = V_s \times \frac{R_{TH} \parallel r_a}{R_s + R_{TH} \parallel r_a}$$

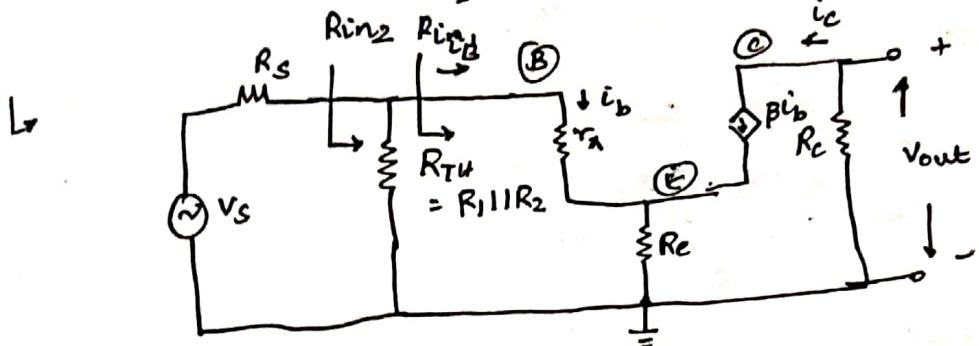
$$\text{Gain} = -g_m R_C \cdot \frac{(R_1 \parallel R_2 \parallel r_a)}{R_C + (R_2 \parallel R_1 \parallel r_a)}$$

CE Amp. with emitter resistance



After C-addition
CE Amplifier with
emitter bypass cap.

For DC analysis
it's open circuit,
For AC analysis
will be shorted due to C_1
thereby increasing
the gain



$$R_{in1} = \frac{V_{in}}{i_b} = r_A + (1+\beta) R_E$$

$$V_{in} = V_s \times \frac{R_{in2}}{R_{in2} + R_s}$$

$$R_{in2} = R_1 || R_2 || R_{in1}$$

$$V_{out} = -\beta i_b R_C$$

$$\text{Gain} = -\beta R_C \times \frac{V_{in}}{R_{in1}} \times \frac{V_s}{V_s}$$

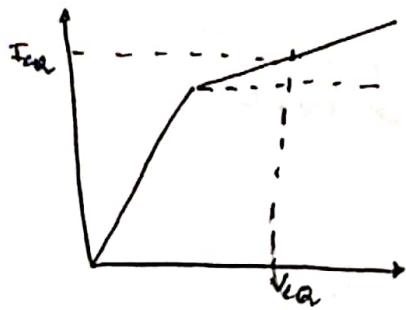
$$= -\frac{\beta R_C}{r_A + (1+\beta) R_E} \times \left(\frac{V_{in}}{V_s} \right)$$

$$= -\frac{\beta R_C}{r_A + (1+\beta) R_E} \times \frac{R_{in2}}{R_{in2} + R_s}; \text{ if, } R_E (1+\beta) \gg r_A \\ R_{in2} \gg R_s$$

$$= -\frac{\beta R_C}{(1+\beta) R_E} \approx -\frac{R_C}{R_E}$$

Q-point stable,
Independent of β

Gain drops when R_E is added



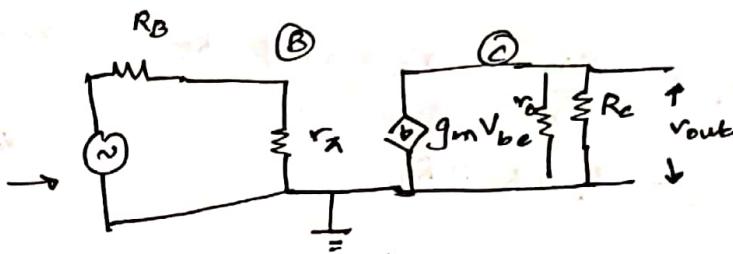
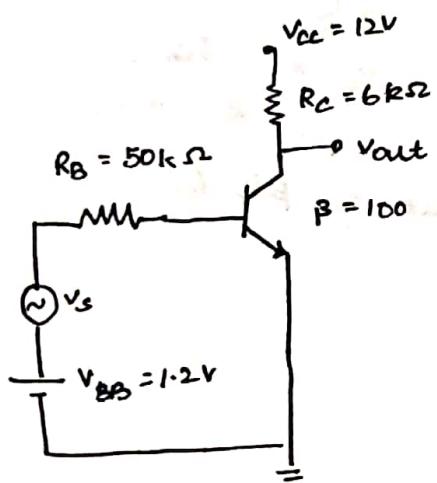
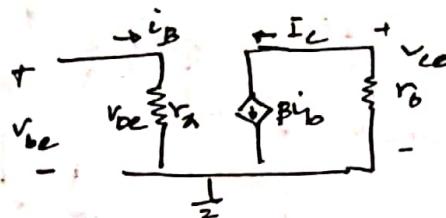
$$i_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) \left[1 + \frac{V_{BE}}{V_A} \right]$$

$$\frac{1}{r_0} = \frac{I_C R}{V_A}$$

$r_0 = \frac{V_A}{I_C R}$ → small signal transition o/p resistance

If $V_A \rightarrow \infty$, $r_0 \rightarrow \infty$, don't consider r_0

If V_A is finite, then consider r_0



$$v_{out} = -g_m v_{be} (r_o \parallel R_c)$$

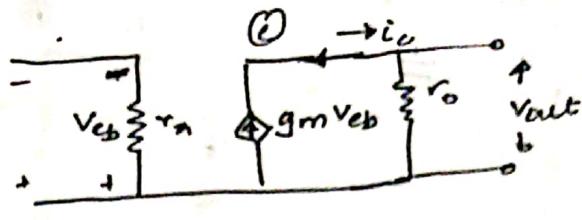
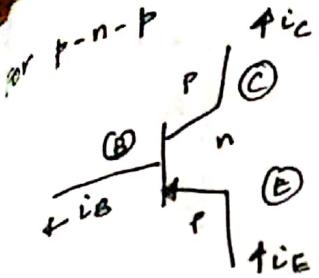
$$v_{be} = \frac{r_x}{R_B + r_x} v_s$$

$$\therefore v_{out} = -g_m \frac{r_x}{R_B + r_x} (r_o \parallel R_c) v_s$$

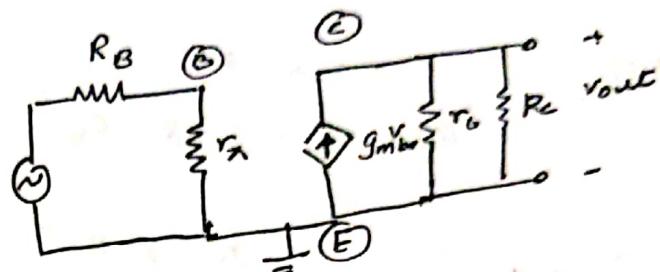
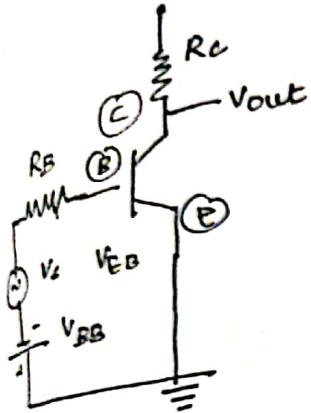
$$\text{Gain} = \frac{v_{out}}{v_{in}} = -g_m (R_c \parallel r_o) \times \frac{r_x}{R_B + r_x}$$

$$R_c > R_c \parallel r_o$$

Thus by considering r_o , gain reduces.



Eg:-

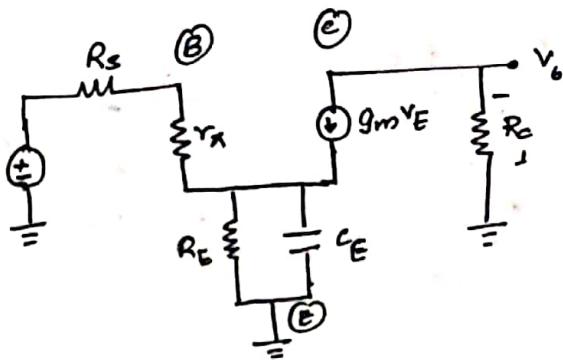
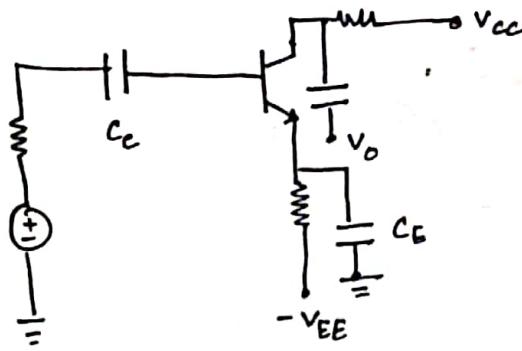


$$V_{out} = g_m V_{eb} (R_C \parallel r_o)$$

$$V_{eb} = -V_S \times \frac{r_A}{R_B + r_A}$$

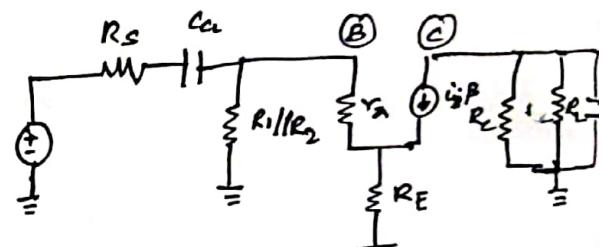
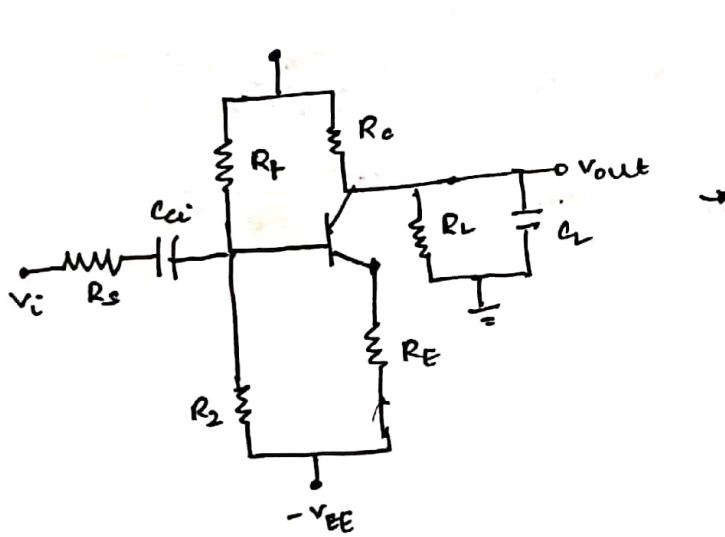
$$V_{out} = -g_m (R_C \parallel r_o) \times \frac{r_A}{R_B + r_A} \times V_S$$

$$\therefore \text{Gain} = -g_m (R_C \parallel r_o) \frac{r_A}{R_B + r_A}$$



$$|AV|_{\omega=0} = \frac{gm r_A R_C}{R_S + r_A + (1+\beta) R_E}$$

$$|AV|_{\omega=\infty} = \frac{gm r_A R_C}{R_S + r_A}$$



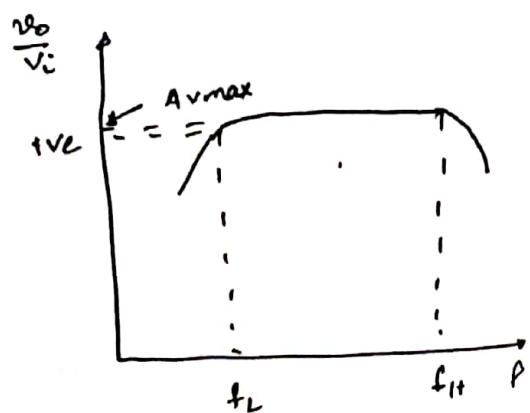
Lower corner freq: $f_L = \frac{1}{2\pi\tau_s}$ lower cut-off
 (HPF)

Upper corner freq: $f_H = \frac{1}{2\pi\tau_L}$ upper cut-off
 (LPF)

$$\tau_s = (R_s + (R_1 \parallel R_2 \parallel R_i)) C_c$$

$$\tau_L = (R_C \parallel R_L) C_L$$

$$R_i = r_A + (1+\beta) R_E$$



At mid band,

$$I_i = \frac{V_i}{R_s + (R_1 \parallel R_2 \parallel R_i)}$$

$$V_A = I_o r_A$$

$$I_o = \frac{R_1 \parallel R_2}{(R_1 \parallel R_2) + R_i} I_i \quad V_o = -g_m V_A (R_C \parallel R_L) \quad C_L \approx \text{small}$$

Gain,

$$A_v = -g_m V_A \left[(R_C \parallel R_L) \cdot \frac{R_1 \parallel R_2}{(R_1 \parallel R_2) + R_i} \cdot \frac{1}{R_s + (R_1 \parallel R_2 \parallel R_i)} \right]$$

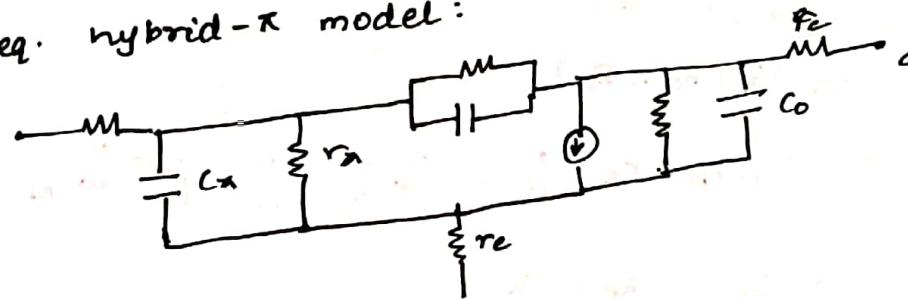
overall,

$$\text{Bandwidth} : f_{BW} = f_H - f_L$$

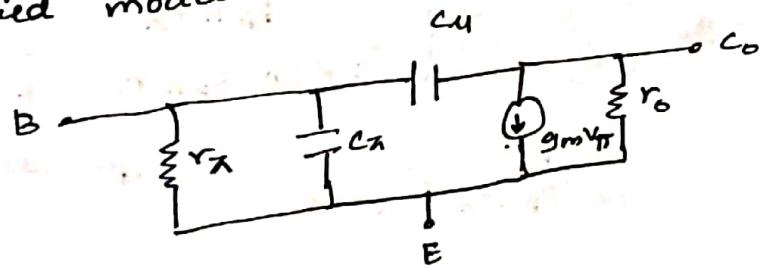
$$\text{Gain Bandwidth} : |A_v|_{\max} f_H \approx \text{const value.}$$

Pdt

High freq. hybrid- π model:



Simplified model



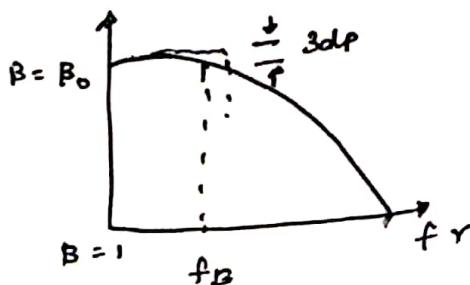
Bandwidth :

$$f_B = \frac{1}{2\pi r_A (C_x + C_u)}$$

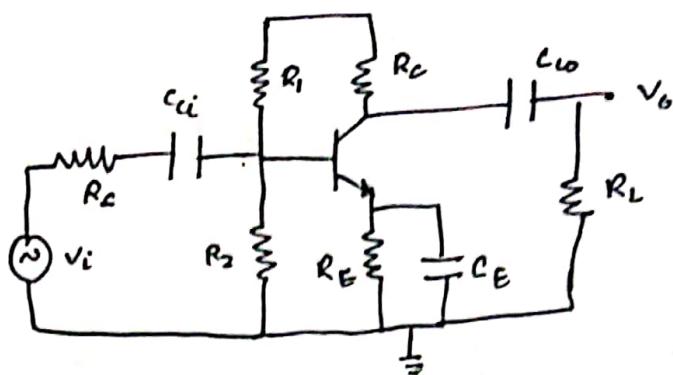
Gain Bandwidth pdt :

$$f_T = \frac{g_m}{2\pi r_A (C_x + C_u)}$$

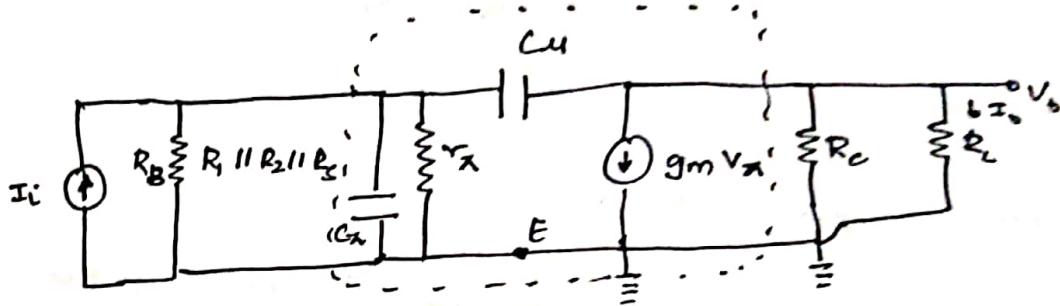
$$= \beta_0 \left[\frac{1}{2\pi r_A (C_x + C_u)} \right]$$



Miller effect Theorem and Miller Capacitance



Convert v_i into an input source and draw the eqn circuit / model.



$$\text{where, } C_M = C_M [1 + g_m (R_C \parallel R_L)]$$

$$= C_M [1 + |A_v|]$$

$$V_x = -g_m V_x (R_C \parallel R_L)$$

$$V_x = I_c \left[(R_B \parallel r_x) \parallel \left(\frac{1}{j\omega C_x} \right) \parallel \left(\frac{1}{j\omega C_M} \right) \right]$$

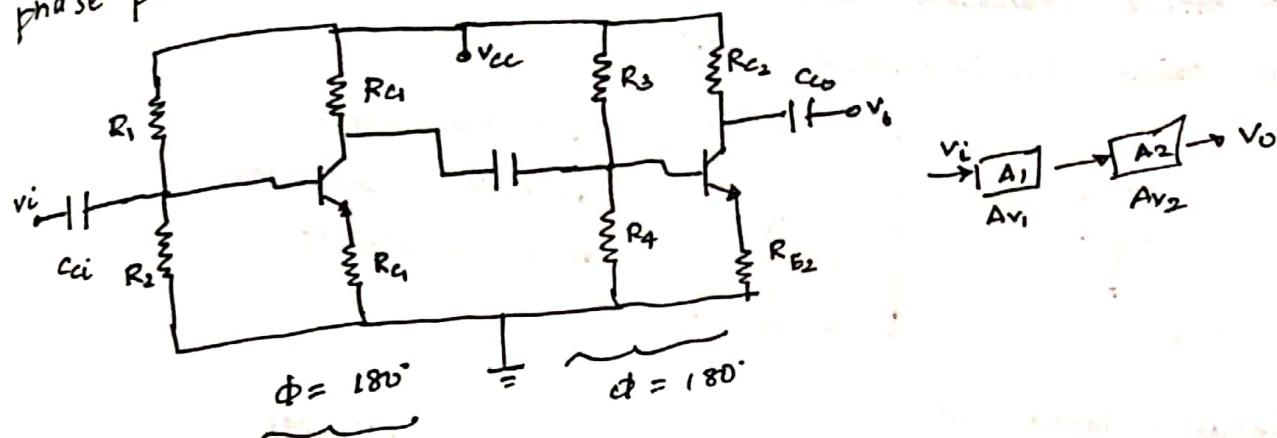
$$= I_c \frac{R_B \parallel r_x}{1 + j\omega (R_B \parallel r_x)(C_x + C_M)}$$

$$A_v = -g_m \left(\frac{R_C}{R_C + R_L} \right) \left[\frac{R_B \parallel r_x}{1 + j\omega (R_B \parallel r_x)(C_x + C_M)} \right]$$

$$f_{3\text{db}} = \frac{1}{2\pi (R_B \parallel r_x)(C_x + C_M)} \quad (\text{LPF like})$$

1) Two stage Amplifier :

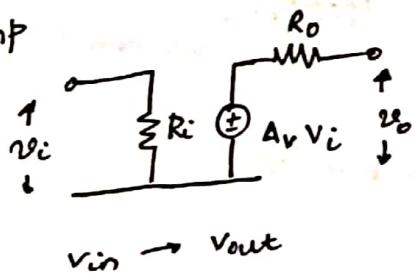
obtains a larger gain w/o bandwidth reduction and phase presentation ($\phi = 0^\circ$)



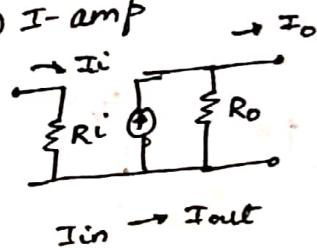
$$\text{Gain}, \quad A_v = |A_{v1}| \cdot |A_{v2}| \quad \phi = \phi_1 + \phi_2$$

2) Q. 2-port networks

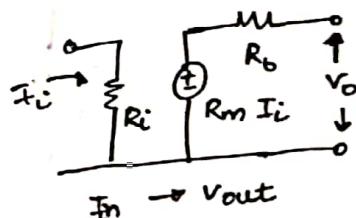
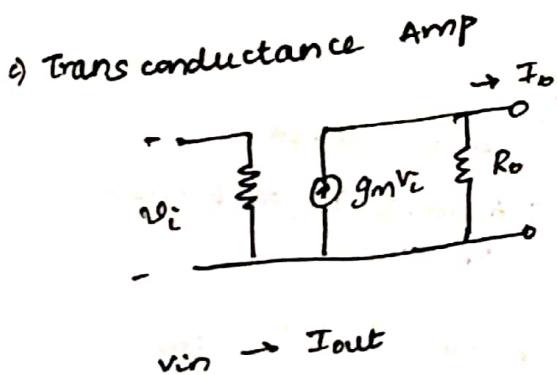
a) v-amp



b) I-amp



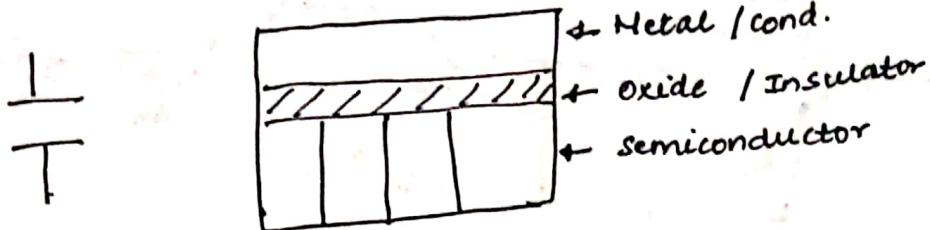
c) Transconductance Amp



MOSFET

Field Effect Transistor (FET)

Metal Oxide semi-conductor (MOS)

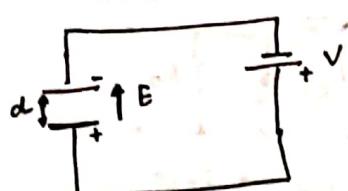


Metal : Gold, Al

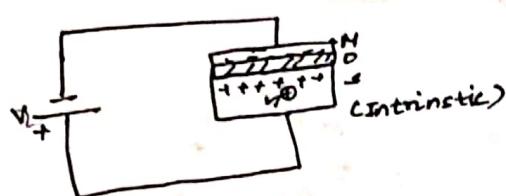
Oxide / Insulator : Silicon dioxide , silicon Nitride

Semi-cond. : Si, Ge

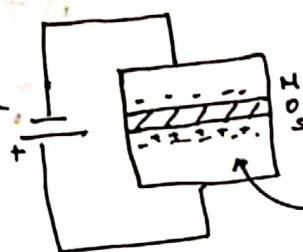
→ MOS is a special capacitor



standard Biasing
of cap.



(intrinsic)



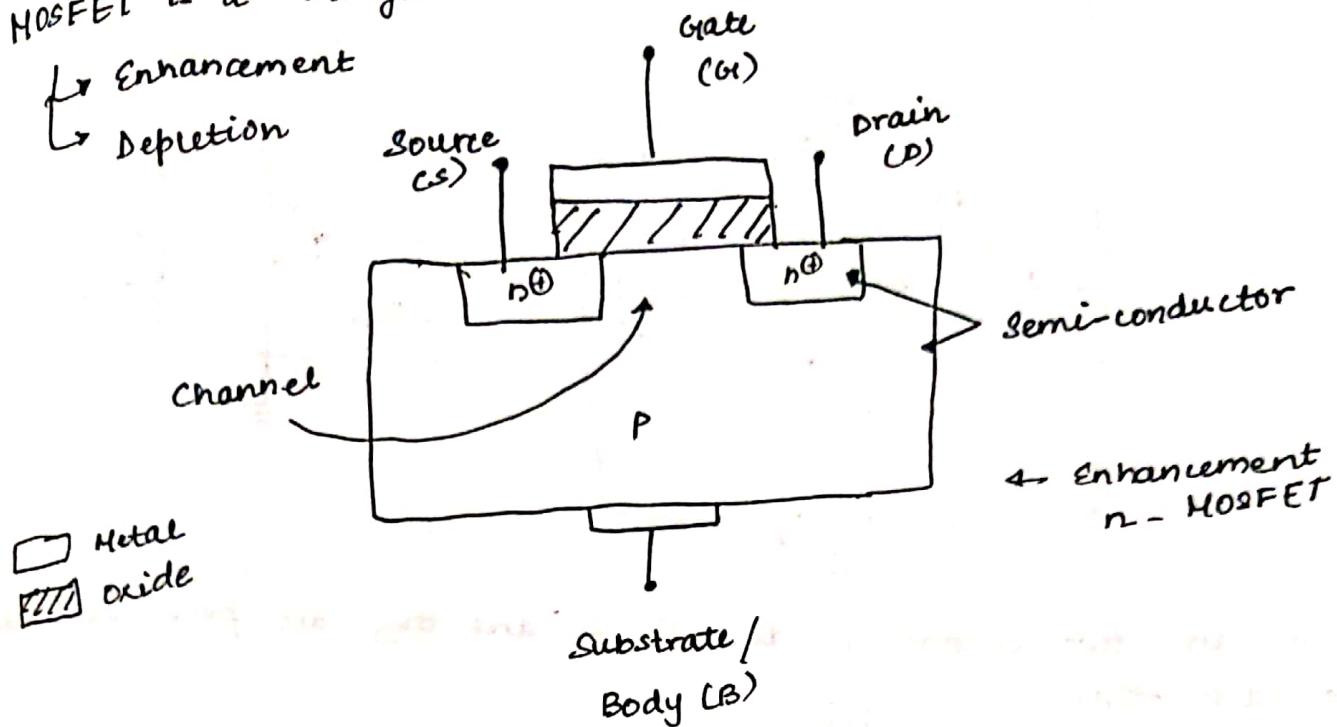
lightly doped
Accumulation / of Inversion
of holes

consider p-type semiconductor, apply +ve to 's'. The supply of holes will be abundant, there is more 'accumulation of holes' as they get move from the +ve to -ve side.

Now if we apply -ve side to the 's'. In that case, the boundary of semi-cond. oxide layer will have lots of e^- around it, although the minority carriers were spreaded around, due to the polarity they get collected, as a result we can think that the upper surface behaves like an n-type material i.e if not inverted to n-type \Rightarrow "Inversion of p"

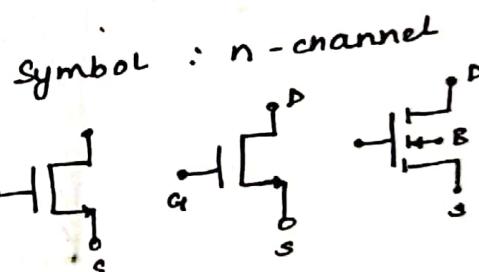
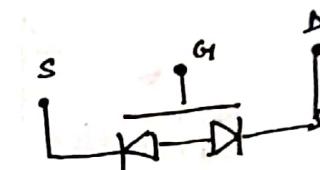
, MOSFET is a voltage

- Enhancement
- Depletion

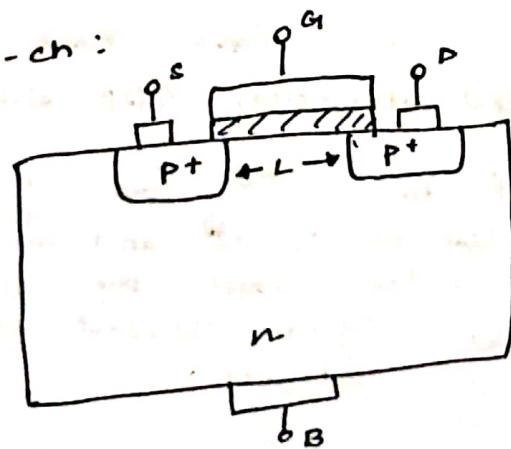


In general

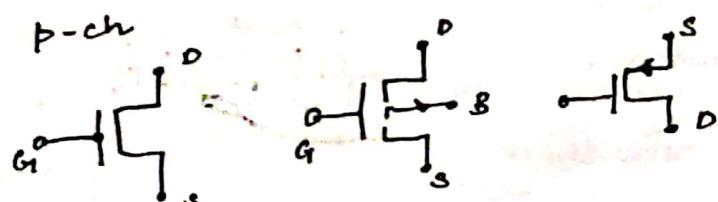
Source → Emitter
Gate → Base
Drain → collector
Substrate → —
→ Doping conc. same,
size also same



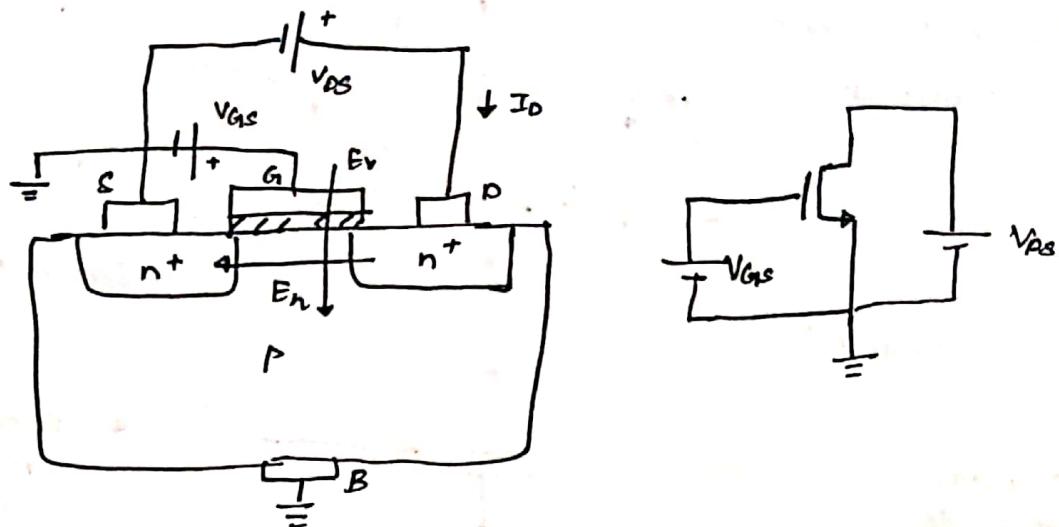
enhancement P-ch:



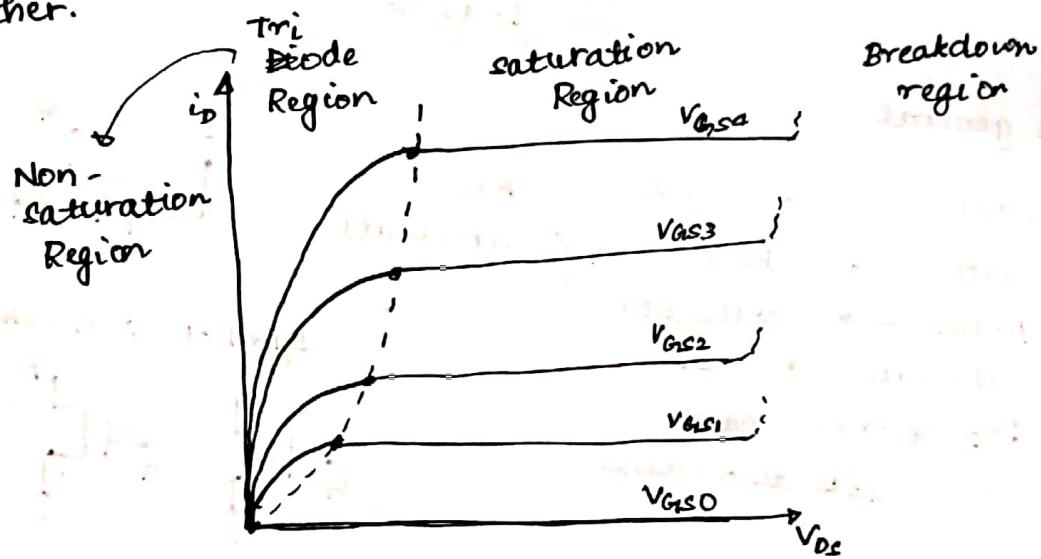
Symbol: p-ch



MOSFET biasing and its V-I char.

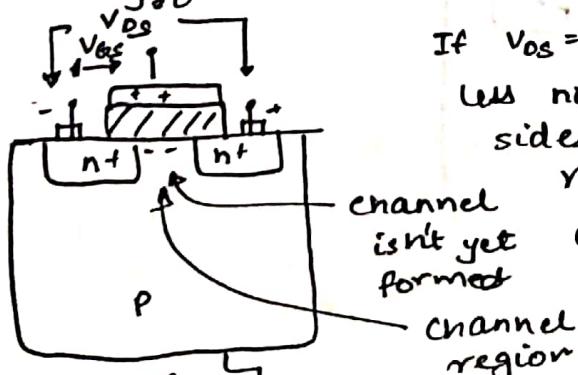


There are two electric fields, E_n , E_g and they are perpendicular to each other.

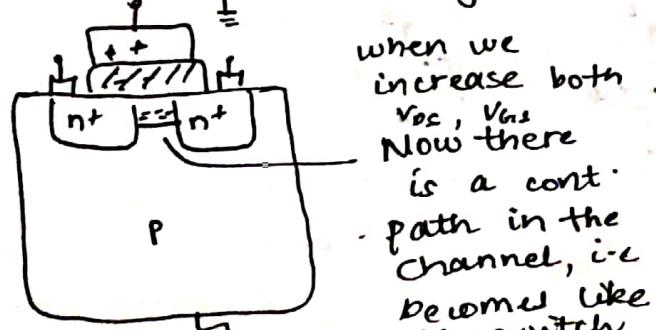


$$V_{GS1} < V_{GS2} < V_{GS3}$$

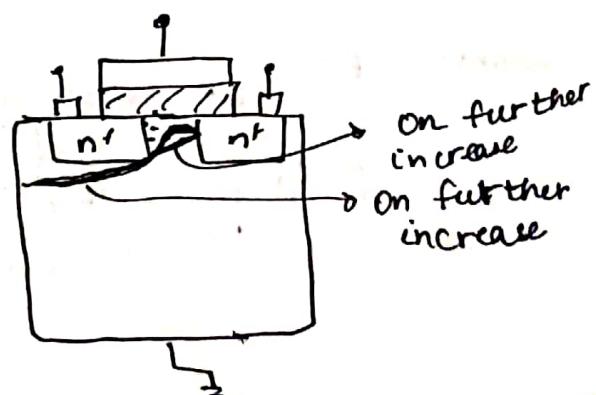
Boundary of triode and saturation also shifts with V_{GS}



If $V_{DS} = 0$, and $V_{GS} \ll 1$, there less no. of e^- and h^+ on both sides and the channel region doesn't enough carriers.



when we increase both V_{DS} , V_{GS} . Now there is a cont. path in the channel, i.e. deformed like an - switch



On further increase
On further increase

k is const for many transistors,
but width could be varying as
per necessity of drain current



$$i_D = K_n \left[2 (V_{GS} - V_{Tn}) v_{DS} - v_{DS}^2 \right]$$

↓
 Gate to source voltage
 ↑
 Drain current

↓ Voltage b/w
 Drain and source
 Threshold Voltage

$K_n \rightarrow$ Transconductor parameter
 Triod Region
 (Non-saturation Region)

$$i_D = K_n (V_{GS} - V_{Tn})^2$$

$$K_n = \frac{w}{L} \mu_n C_{ox} \cdot \frac{1}{2} = K_n' \cdot \frac{1}{2} \cdot \frac{w}{L}$$

↑ Mobility of e^-
 ↑ Gate oxide parameter

↓ Process conductor parameter

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

per unit area

$$r_o = \frac{\Delta v_{DS}}{\Delta i_D} \quad | \quad V_{GS} = \text{constant}$$

Output resistance
 Slope of
 V-I char in
 saturation
 region

p-channel mosfet

$$i_D = K_p \left[2 (V_{SG} + V_{TP}) v_{SD} - v_{SD}^2 \right]$$

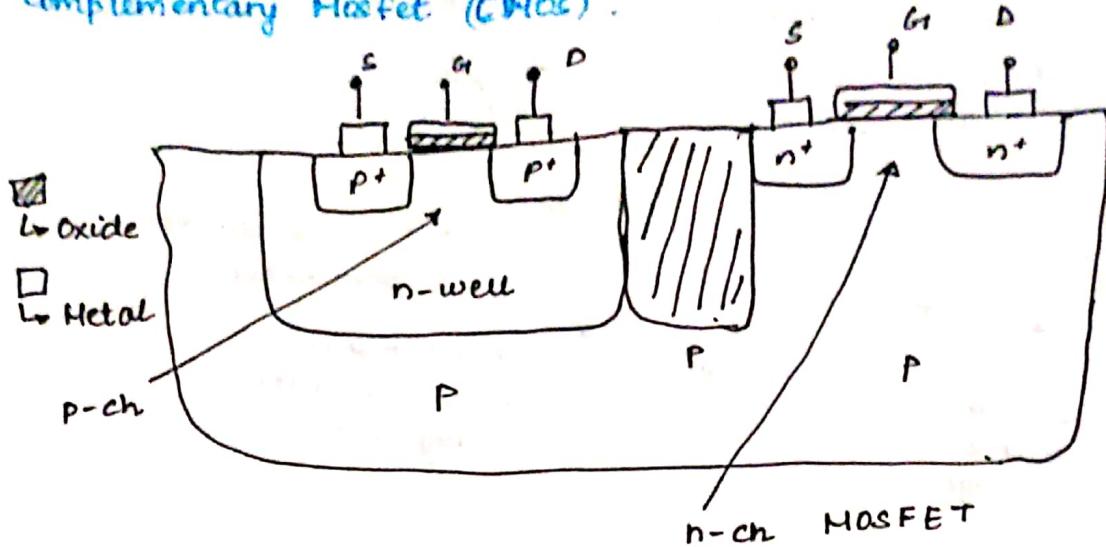
↓ voltage at which mosfet turns on

$$i_D = K_p (V_{SG} + V_{TP})^2$$

$$K_p = \frac{1}{2} \frac{w}{L} \mu_p C_{ox} = \frac{K_p'}{2} \cdot \frac{w}{L}$$

$$K_p' = \mu_p C_{ox}$$

Complementary MOSFET (CMOS) :

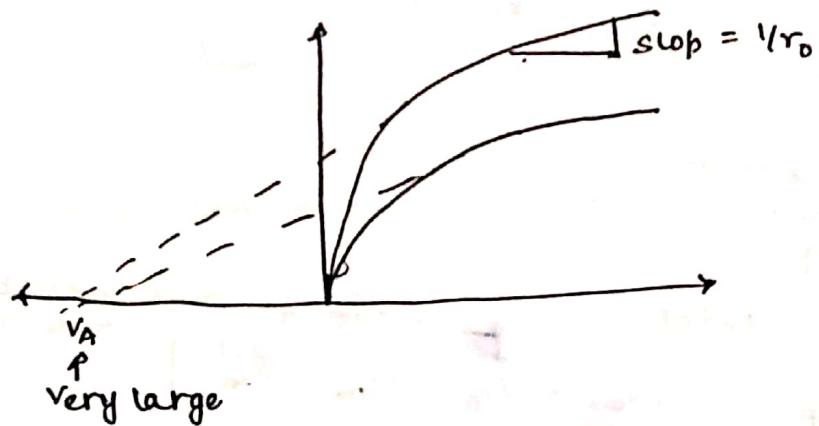


Advantages of CMOS

- Compact (very small)
- low power (As there is no current)
- Robust Technology
- High density fabrication

b) Non-Ideal MOSFET characteristics:

i) V-I characteristics gets modified due to V_A :



In saturation region,

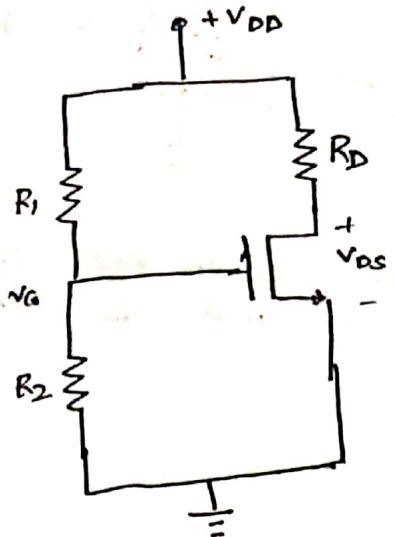
$$i_D = k_n \left[(V_{DS} - V_{TN})^2 \left(1 + \frac{1}{\lambda} \frac{V_{DS}}{V_A} \right) \right]$$

↑
channel length
modulation

$$r_0 = \frac{1}{\lambda I_{DQ}} = \frac{V_A}{I_{DQ}}$$

$$V_A = 1/\lambda$$

i) common Source (dc) circuit:



(n-channel MOSFET)

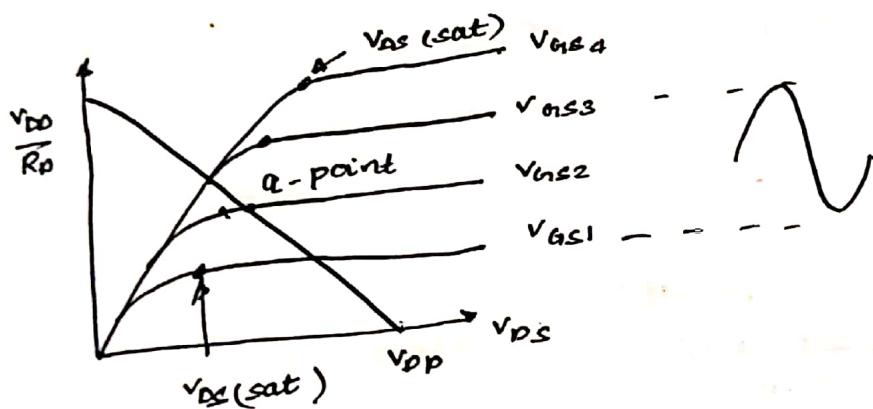
$$V_G = V_{GS} = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$I_D = K_n (V_{GS} - V_{Th})^2 \quad (\text{saturation})$$

$$V_{DS} = V_{DD} - I_D R_D$$

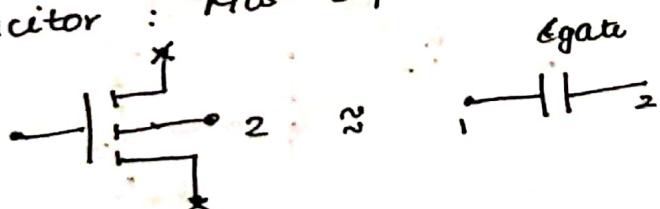
$$P_T = V_{DS} \cdot I_D$$

1
Inst.
voltage drop

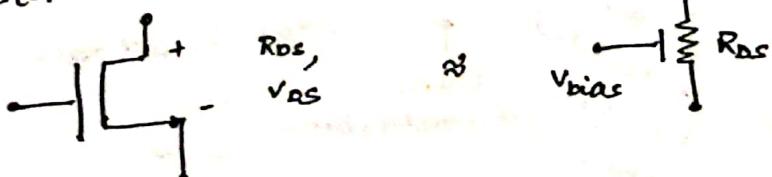


MOSFE as other electrical components :

① capacitor : MOS capacitor



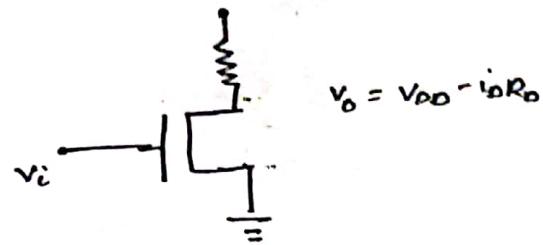
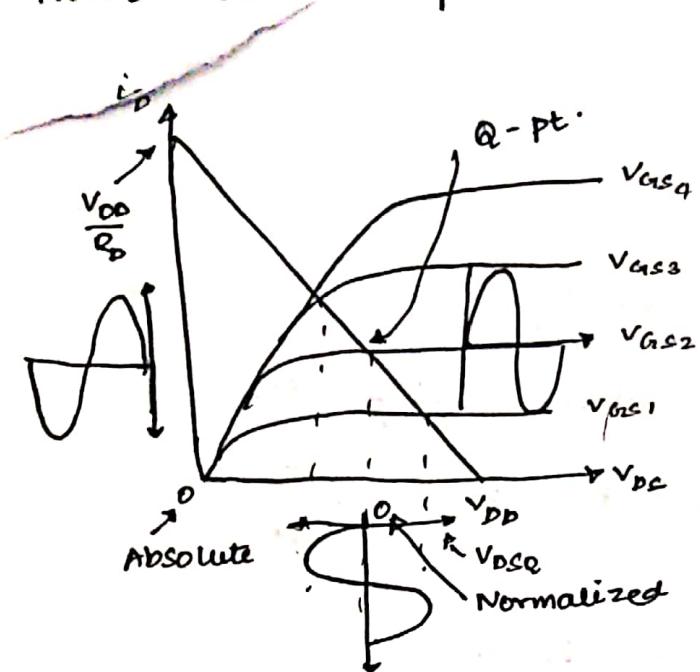
② Resistor



③ Diode

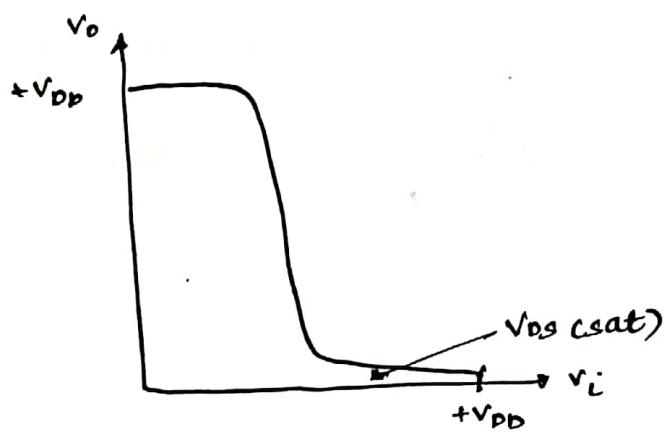


MOSFET as an Amplifier : Common Source

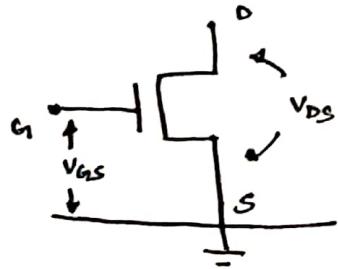


when v_{GS} is high i_D is high and v_{DS} reduces

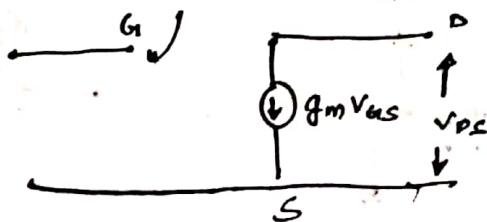
Transfer characteristics



Small signal Eq. circuit



Mosfet has gate capacitor
resistance intro cap

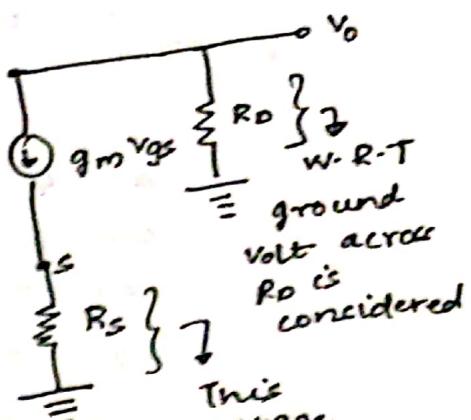
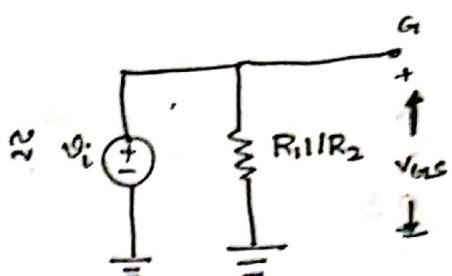
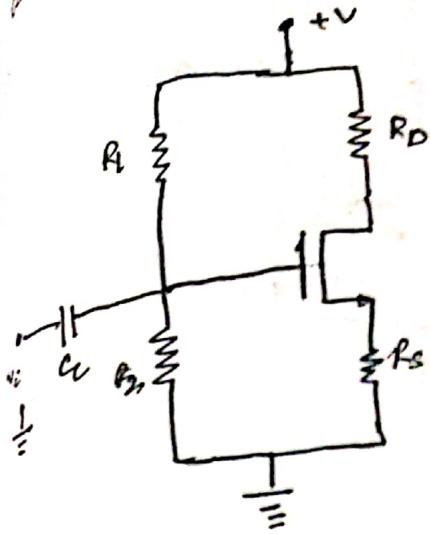


g_m also is affected by gate capacitance Trans conductance

$$g_m = \frac{\partial i_D}{\partial V_{GS}} \quad |_{V_{DS}, V_{GSq} = \text{constant}}$$

$$g_m = 2 \sqrt{k_n I_{Dq}} = 2 k_n C_{VGSq}^{-1/2}$$

Amplifier with source resistor (R_s)



current going from ground to output

$$v_o = -g_m v_{ds} R_D$$

$$\begin{aligned} v_i &= v_{gs} + (g_m v_{gs}) R_s \\ &= v_{gs} (1 + g_m R_s) \end{aligned}$$

This voltage drop isn't considered here, as it goes to ground

$$A_v = \frac{v_o}{v_i} = \frac{-g_m R_D}{1 + g_m R_s} \approx -\frac{R_D}{R_s}$$

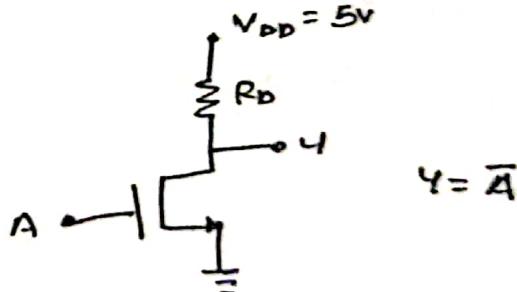
($\because g_m$ is large)

(unit: siemens)

Digital circuits using MOSFETS:

i) NOT gate (or inverter)

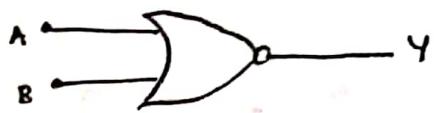
$A = 0V$	$y = 1$
$A = 5V$	$y = 0$
$0V < v_{TN}$	$5V > v_{TN}$
$v_{DS} = 0V$	$v_{DS} = 5V$



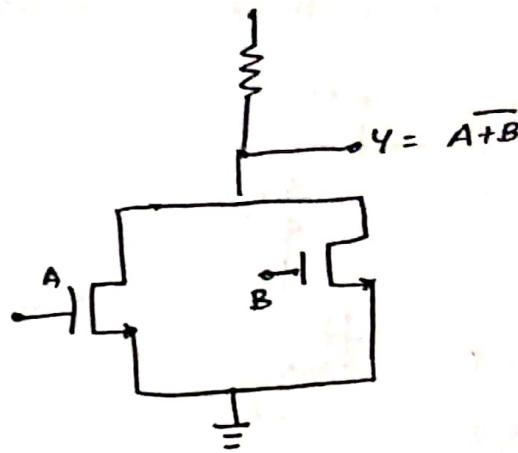
If input is 0V, then output is V_{DD} , if we apply V_{DD} at input output is 0V

↑
check TC for better understanding

(iii) NOR gate :



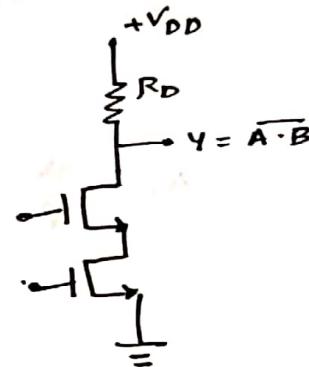
A	B	Y
0V	0V	5V
0V	5V	0V
5V	0V	0V
5V	5V	0V



(iii) NAND gate



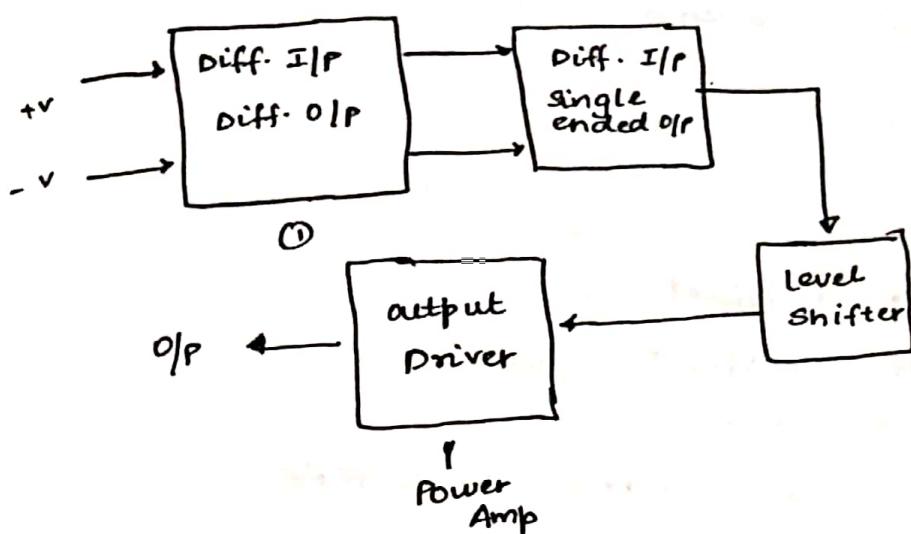
A	B	Y
0V	0V	5V
0V	5V	5V
5V	0V	5V
5V	5V	0V



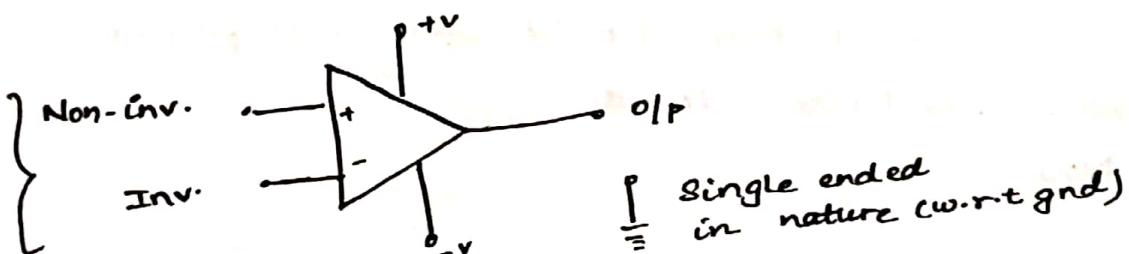
0V : '0' logic
1V : '1' logic

Opamps are specialized type of voltage amplifiers

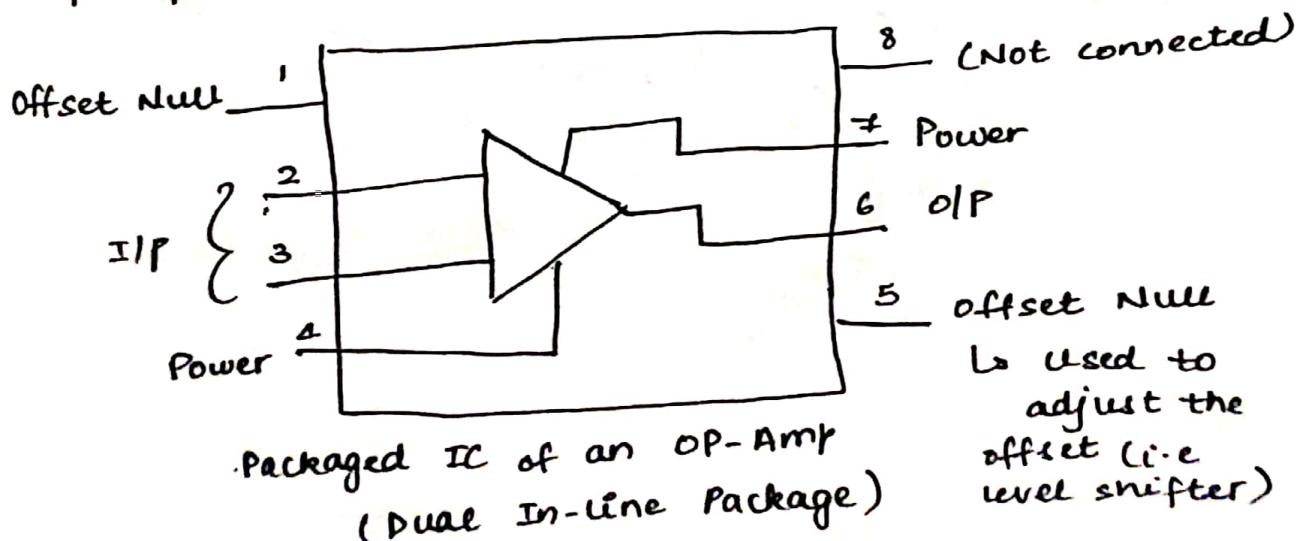
General block diagram:



We have some gain at ① A_1 , and then to the cascade A_2 . Both the gains would be multiplied, whose output is given to the level shifter, it is nothing but voltage offsetter, i.e. changes the voltage level, o/p driver is a power amp, it enhances the ability to drive thus enhancing the current.



741 op-amp: Commercial integrated circuit of an op-amp.



Ideal characteristics of Op-Amp

→ Input Impedance $\rightarrow \infty$

If we just connect a voltage source, no current would be entering op-amp chip.

→ Output Impedance

→ Gain as ∞

→ offsets → I/P v-offset
O/P v-offset
I/P I-offset } = 0

→ Common mode rejection ratio = ∞ (CMRR)

↳ Rejecting noise at Input

→ Power supply rejection ratio = ∞ (PSRR)

↳ If DC voltage fluctuates, the op-amp operation shouldn't change.

→ Slew rate = ∞

↳ ability to change O/P inst. without delay

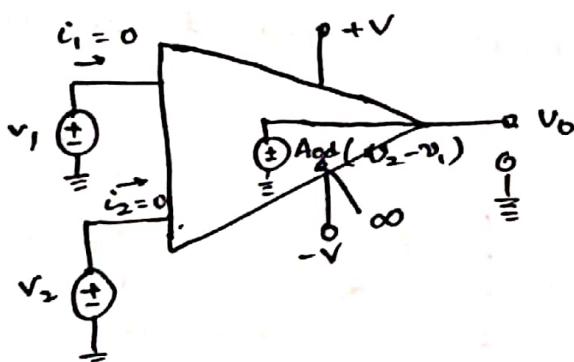
→ Quiescent power = 0

↳ Op-Amp should take zero power

→ Gain bandwidth pdt = ∞

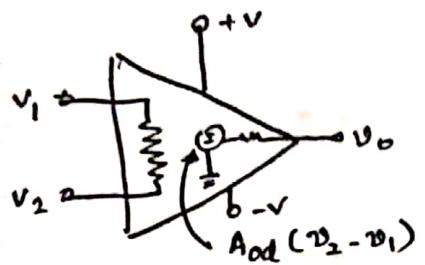
→ Noise = 0

equivalent circuit

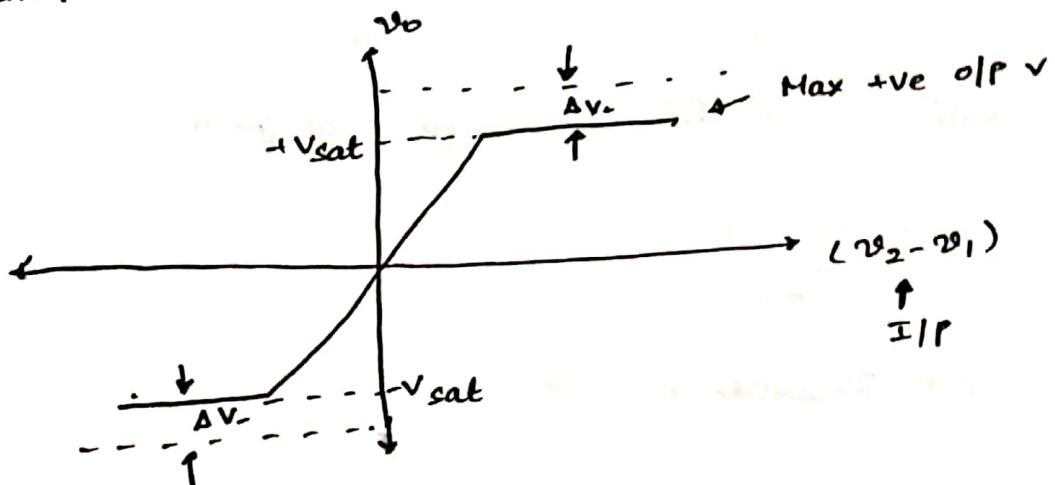


A_{od} = open loop differential gain

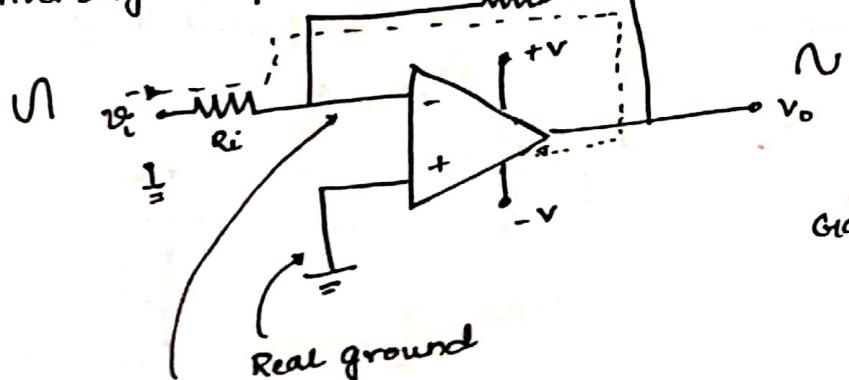
Practical Op-amp.



Voltage Transfer Characteristics



Inverting Amplifier



$$\text{Gain} = -\frac{R_f}{R_i}$$

$$i_i = \frac{v_i - 0}{R_i}$$

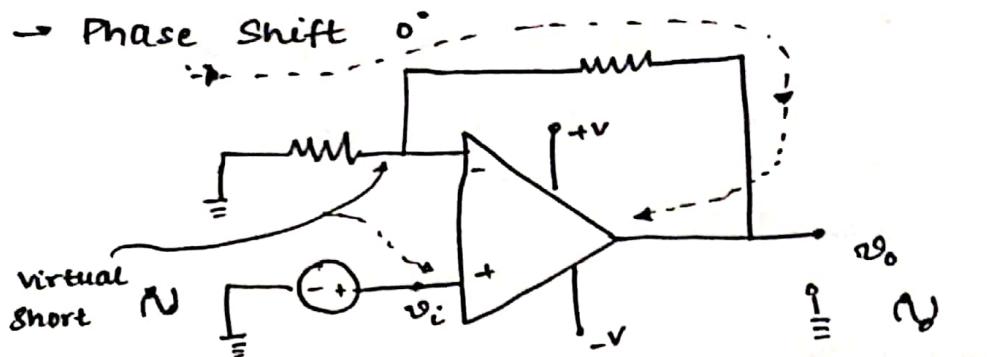
$$= \frac{0 - v_o}{R_f}$$

$$\therefore v_o = -\frac{R_f}{R_i} v_i$$

$$\text{I/P resistance} = \frac{v_i}{i_i} = R_i$$

No coupling capacitor \Rightarrow Both DC and AC can be applied

Non-Inverting Amp

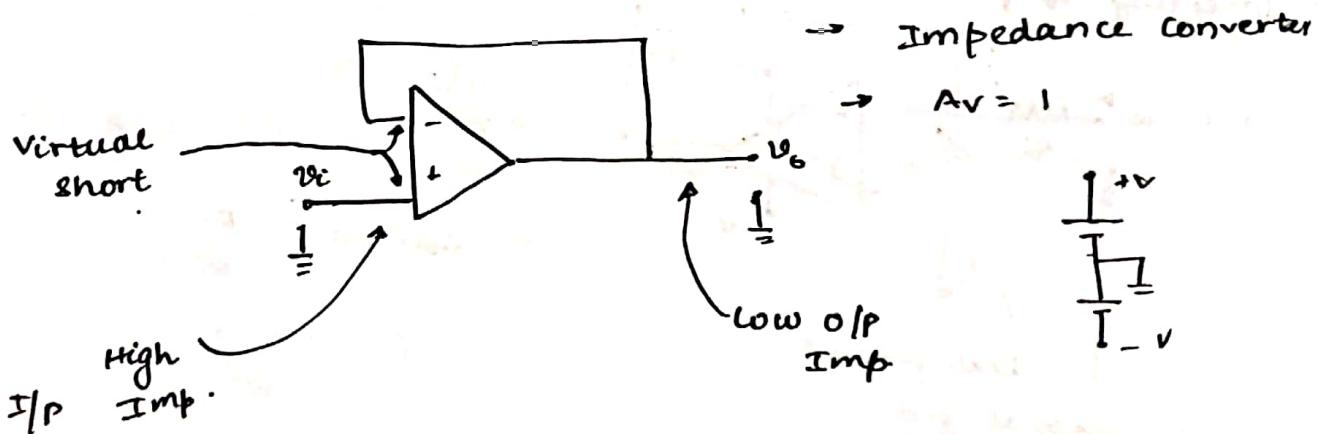


$$\text{Gain} = 1 + \frac{R_f}{R_i} \leftarrow \text{Closed Loop gain}$$

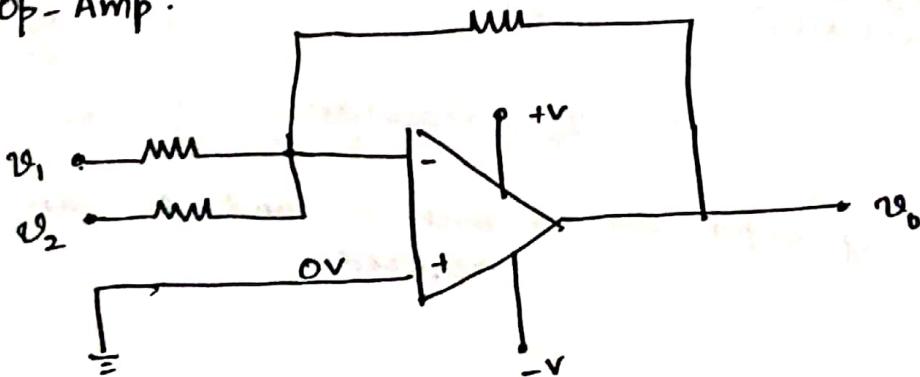
$$i_i = \frac{v_i - v_o}{R_f}$$

I/P Resistance = ∞

Voltage Follower (Unity Gain Amp.)



Adder Op-Amp.



Assume only v_1 is applied, while $v_2 = 0$

$$v_{o1} = -i_1 R_f = -\frac{R_f}{R_i} v_1$$

Assume, v_2 is applied while $v_1 = 0$

$$v_{o2} = -i_2 R_f = -\frac{R_f}{R_2} v_2$$

$$\therefore v_o = v_{o1} + v_{o2}$$

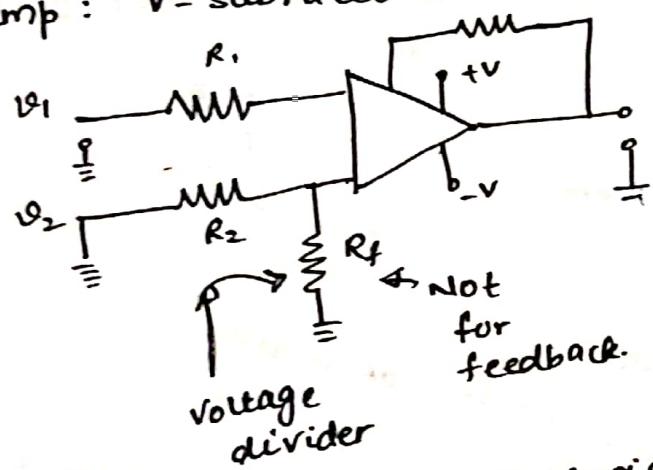
$$\Rightarrow v_o = -\frac{R_f}{R_i} v_1 - \frac{R_f}{R_2} v_2$$

$$v_o = -\left(\frac{R_f}{R_i} v_1 + \frac{R_f}{R_2} v_2\right)$$

$R_f = R_i \rightarrow$ v-adder
 $R_f > R_i \rightarrow$ summing Amp.
 $R_f < R_i \rightarrow$ summing attenuator.

$$\text{If } R_1 = R_2 = R_i : \quad v_o = -\frac{R_f}{R_i} (v_1 + v_2)$$

Dif. amp: v-subtractor



Applying superposition Analysis:

(Inv. opamp)

$$v_2 = 0 : \quad v_{o1} = -\frac{R_f}{R_i} v_1$$

$$v_1 = 0 : \quad v_{o2} = \left(\frac{R_f}{R_2 + R_f}\right) v_2 \quad \left(1 + \frac{R_f}{R_i}\right) \quad (\text{Non-inv. opamp})$$

$$v_{o2} = v_{o1} + v_{o2} = -\frac{R_f}{R_i} v_1 + \left(1 + \frac{R_f}{R_i}\right) \left[\frac{R_f/R_2}{1 + R_f/R_2}\right] v_2$$

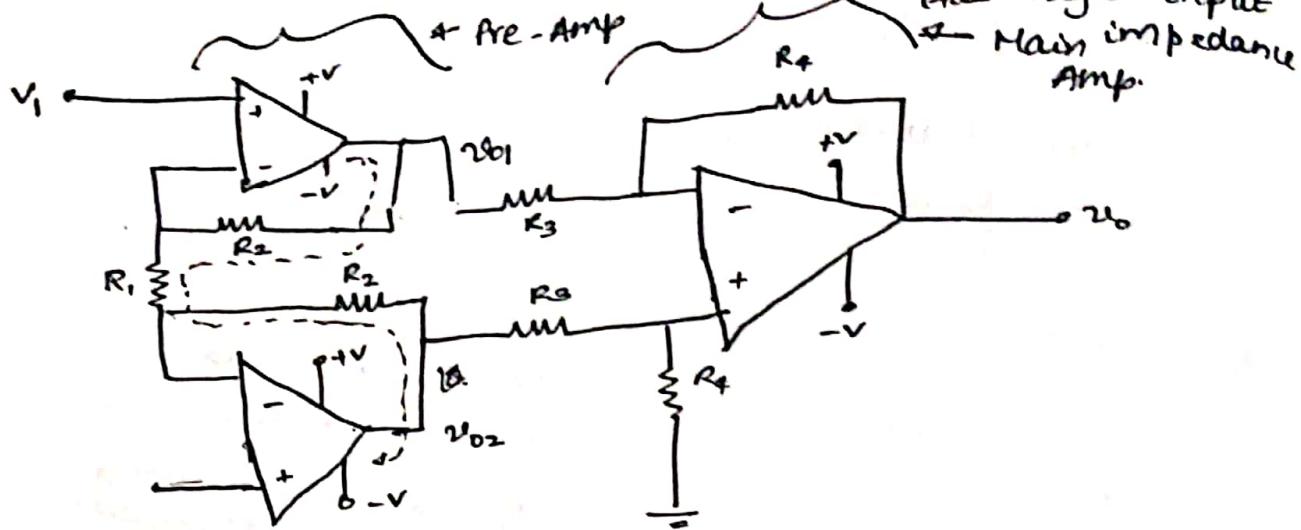
$$\text{If, } R_1 = R_2 = R_i \quad \text{or} \quad \frac{R_f}{R_i} = \frac{R_f}{R_2} = \frac{R_f}{R_i}$$

$$v_o = \frac{R_f}{R_i} (v_2 - v_1)$$

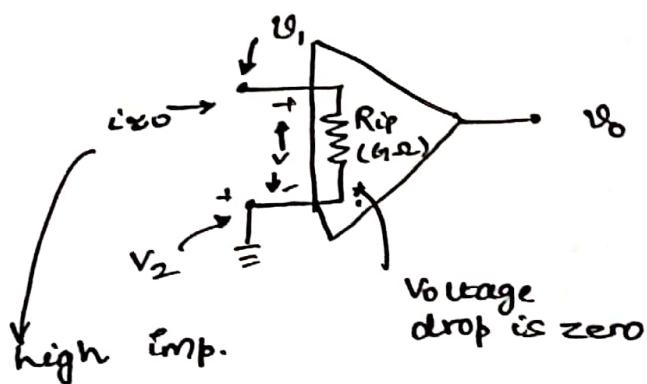
& diff. gain

I/P resistance = $2R_i$

I Instrumentation Amplifier \rightarrow special case of diff. amp.
 Has high input impedance Amp.



\rightarrow Virtual ground [short]:

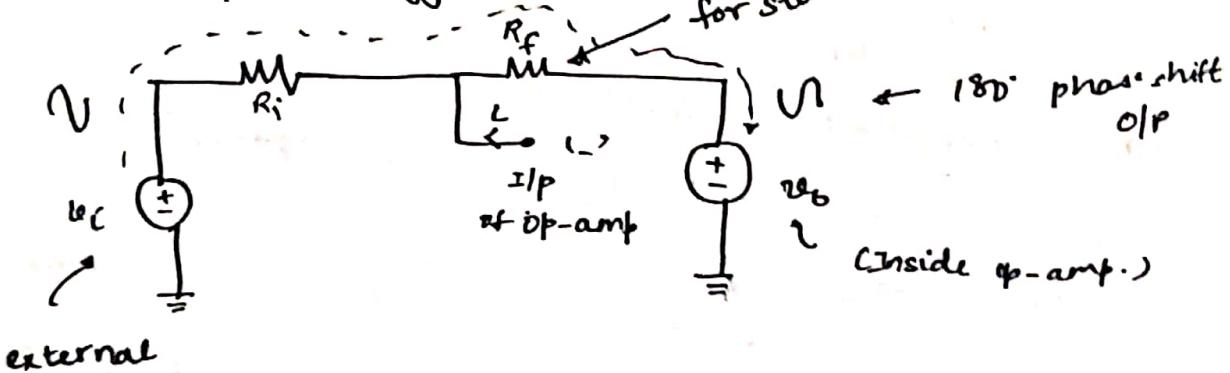


In open loop, input imp is high

Now if we apply ground at V_2

$$\begin{aligned} \theta &= V_2 - V_1 \\ &= iR_1/p \\ &= 0 \end{aligned}$$

\rightarrow closed loop Analogy: Inv. amp. for stabilisation



CMRR (Common Mode Rejection Ratio)

$$\text{CMRR (db)} = 20 \log_{10} \left| \frac{A_d}{A_{cm}} \right|$$

Diff. gain
common mode
gain signal

\rightarrow Selective ability to reject common mode noise signal now common to both '+' and '-' to an op-amp

$$v_{o1} = v_1 + iR_2 \approx \left(1 + \frac{R_2}{R_1}\right) v_1 - \frac{R_2}{R_1} v_2$$

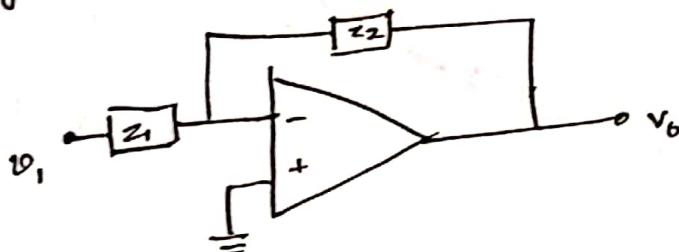
$$v_{o2} = v_2 + iR_2 = \left(1 + \frac{R_2}{R_1}\right) v_2 - \frac{R_2}{R_1} v_1$$

$$v_o = \frac{R_4}{R_3} (v_{o2} - v_{o1})$$

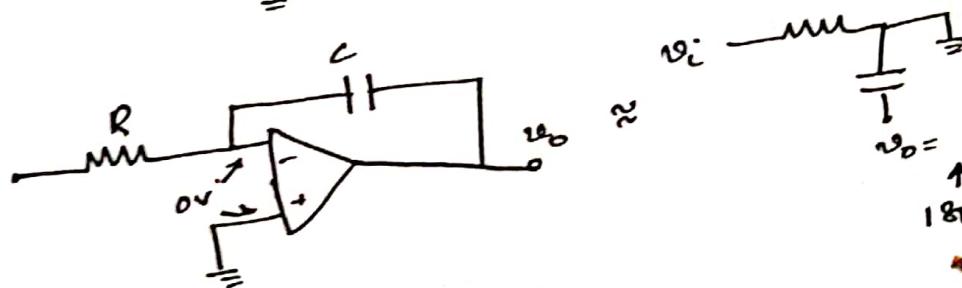
$$= \frac{R_4}{R_3} \left(1 + \frac{2R_2}{R_1}\right) (v_2 - v_1)$$

$\underbrace{\phantom{1 + \frac{2R_2}{R_1}}}_{\text{Diff. gain}}$

→ Integrator (Active low pass filter)



$$\frac{v_o}{v_i} = -\frac{Z_2}{Z_1}$$



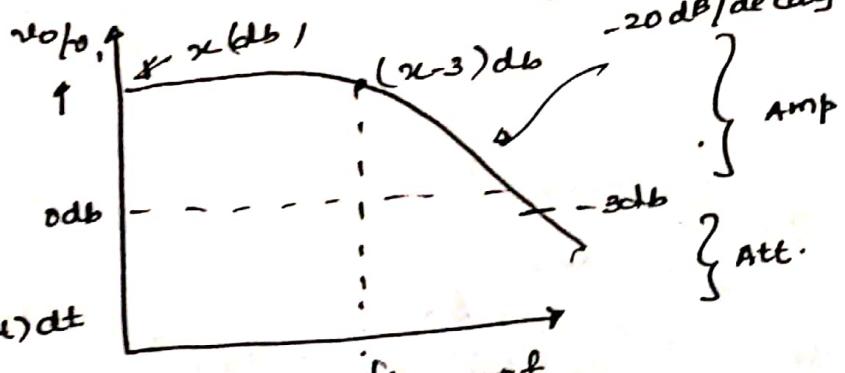
$$v_o = -\frac{Z_2}{Z_1} v_i$$

↑ 180° phase shift

$$x_c = \frac{1}{2\pi f C}$$

$$v_o = -\frac{1}{sRC} v_i$$

$$v_o = v_c - \frac{1}{RC} \int v_i(t) dt$$



If $v_c = 0$ at $t = 0$,

$$v_o = -\frac{1}{RC} \int_0^t v_i(t) dt$$