Centre for Heterogeneous and Intelligent Processing Systems

Department of ECE | PES University | Electronic City Campus

Presents

Two Day Workshop on

Standard Cell Design, Characterization and Synthesis

January 19th and 20th, 2024, PESU - EC Campus

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Standard Cell Design, Characterization and Synthesis

Centre for Heterogeneous and Intelligent Processing Systems

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Digital IC Design

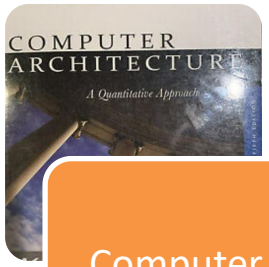
Course Flow for Digital IC Design : PES University

Computer Aided Digital Design

Digital VLSI Design

RISC-V Architecture

Electronic Device Automation – Verilog to Routing (E)



Computer Architecture

Memory Design and Testing (E)

FPGA based Design Flow-RTL using System Verilog

Digital Circuit Design (Schematic and Layout)

and Microarchitecture Design using RTL

Placement and Routing (RTL to GDS-II)

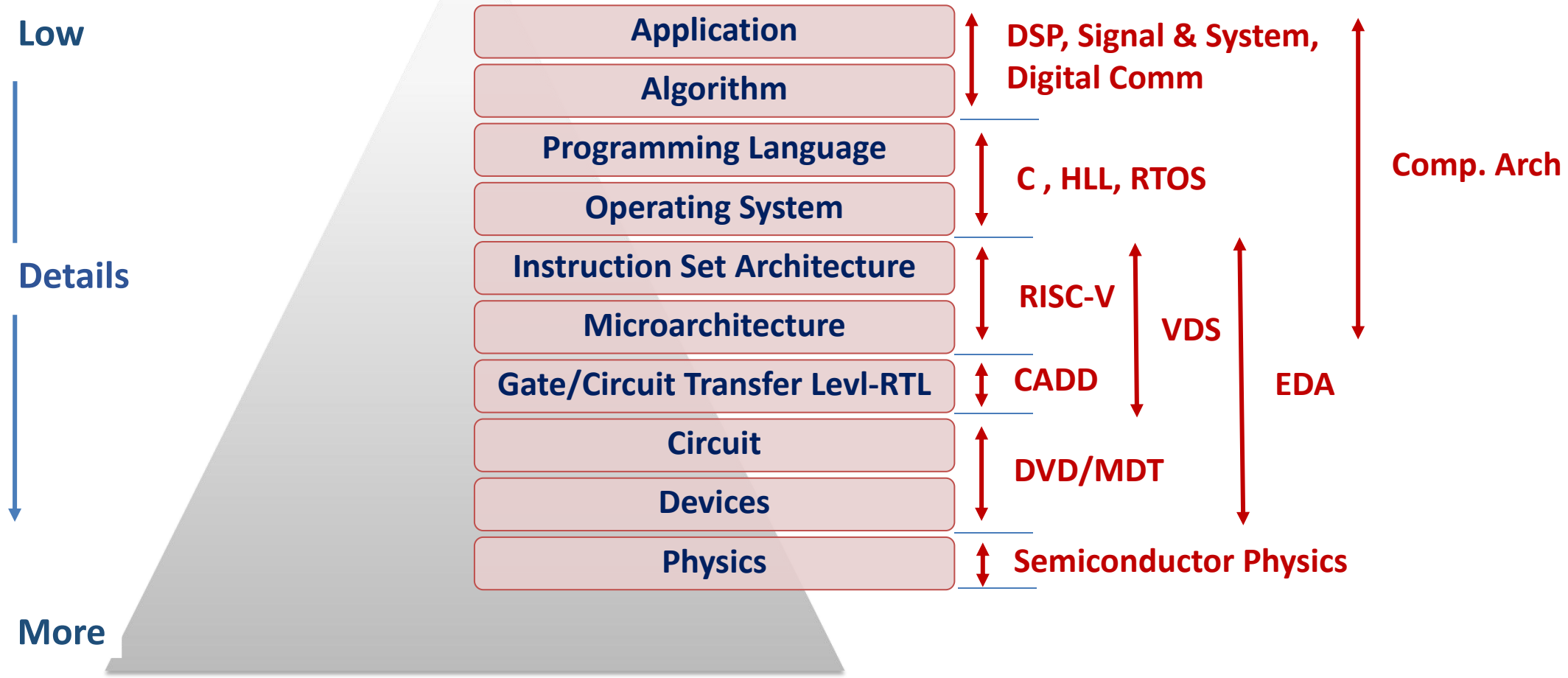
Memory Organizatio and Computer Architecture

SRAM and DRAM sign Concepts and the Testing

Verification and Testing of Digital Circuits

Digital IC Design

Abstraction: In Modern System



Digital VLSI Design

Mahesh Awati
Department of Electronics and Communication Engg.

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Introduction to VLSI Design Flow:

RTL - GDSII

VLSI Design Flow: RTL - GDSII

Different VLSI Design Flow

What is VLSI Design Flow?

- Methodology to design an IC such that it delivers the required functionality or behavior.

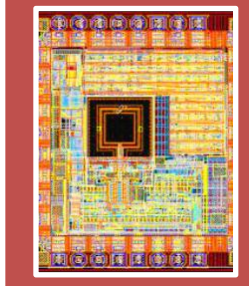
What decides VLSI Design Flow?

- The VLSI design flows depends on the type of integrated circuits:
  - Scope of application
  - Design Styles

VLSI Design Flow: RTL - GDSII

Different VLSI Design Flow – based on Scope of Application

Types of Integrated Circuit based on **scope of application**



Application Specific Integrated Circuits (ASICs)

General Purpose Integrated Circuits

VLSI Design Flow: RTL - GDSII

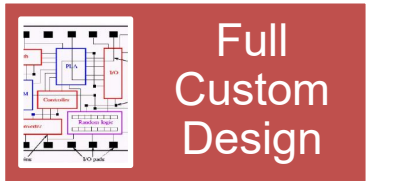
Different VLSI Design Flow – based on Scope of Application

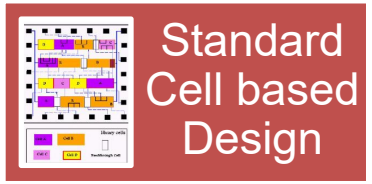
Difference between ASIC and GPIC

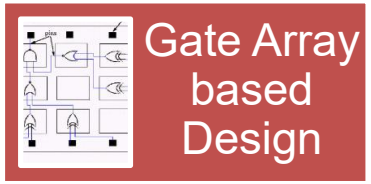
	Application Specific Integrated Circuits (ASICs)	**General Purpose Integrated Circuits**
Functionality	A chip designed to perform as a particular end system	A chip designed to perform as a wide range of end-system
Examples	IC for digital camera, audio/ video processor, security chip etc.	Microprocessors, memory, FPGA
Programmability	Not software programmable to perform a wide variety of different tasks	Usually software programmable to perform a wide variety of different tasks
Volume of production	Less	More

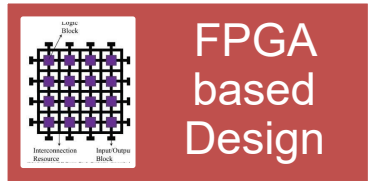
VLSI Design Flow: RTL - GDSII

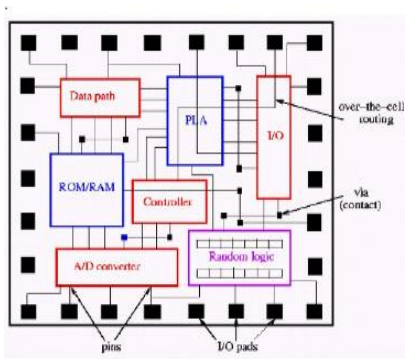
Types of Design style

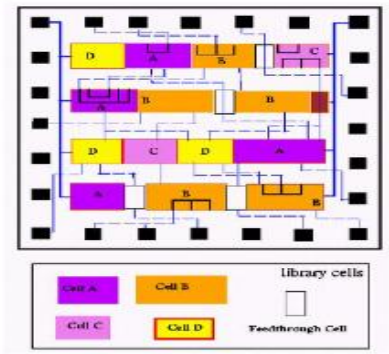


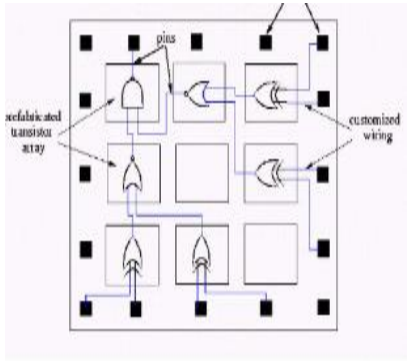


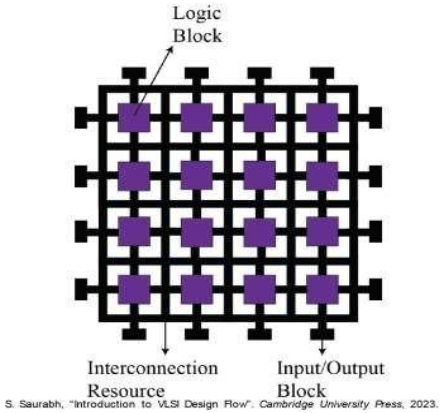












S. Saurabh, "Introduction to VLSI Design Flow", *Cambridge University Press*, 2023.

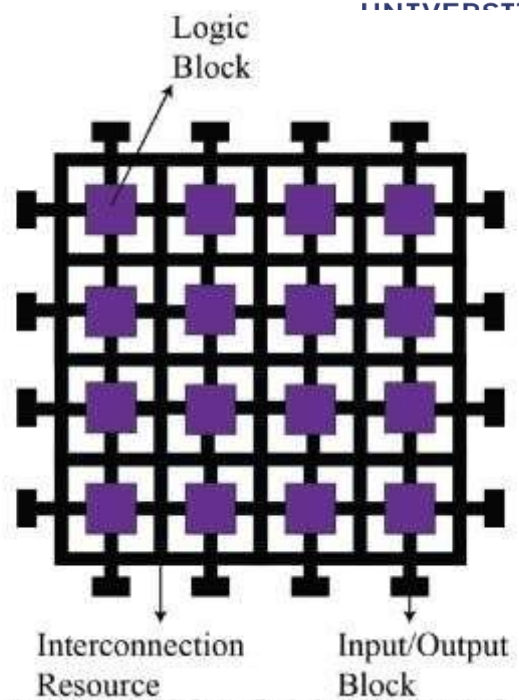
VLSI Design Flow: RTL - GDSII

Types of Design style

FPGA based design

- IC hardware is fixed
- Designer obtain the desired functionality by programming
  - Programming changes the interconnections between the elements of the circuits

- FPGA consist of array of logic blocks, I/O blocks and routing channels
- Logic blocks can be programmed to perform different functions such as AND, OR, adder etc.
- FPGA boards may also have embedded microprocessors, analog components and blocks performing special functions such as DSP block.



S. Saurabh, "Introduction to VLSI Design Flow", *Cambridge University Press*, 2023.

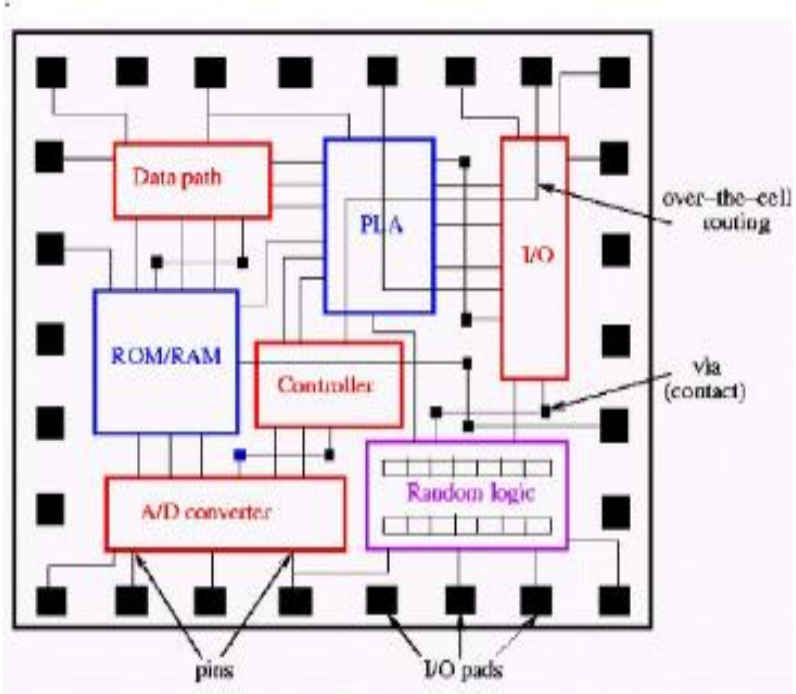
- Xilinx (AMD), Altera (Intel)

VLSI Design Flow: RTL - GDSII

Types of Design style

Full-custom design

- Layout of transistors and interconnects are design specific
- Huge design effort
- Very few designs are full-custom
- Analog mixed/signal designs
- High volume products such as microprocessors (some portion)
- Merit: design can be highly optimized

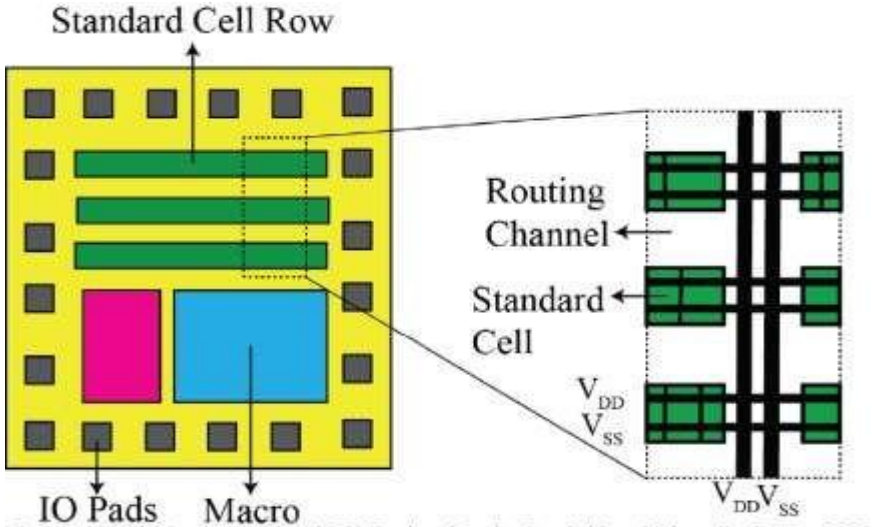


VLSI Design Flow: RTL - GDSII

Types of Design style

Standard-cell based design

- **Standard Cells**: simple cells such as AND, NAND, flip-flop etc. that are optimally designed and modeled in a library, fixed height
- **Macros:** complex cells such as full-adder, multiplier, memory etc.
- Allows high degree of automation



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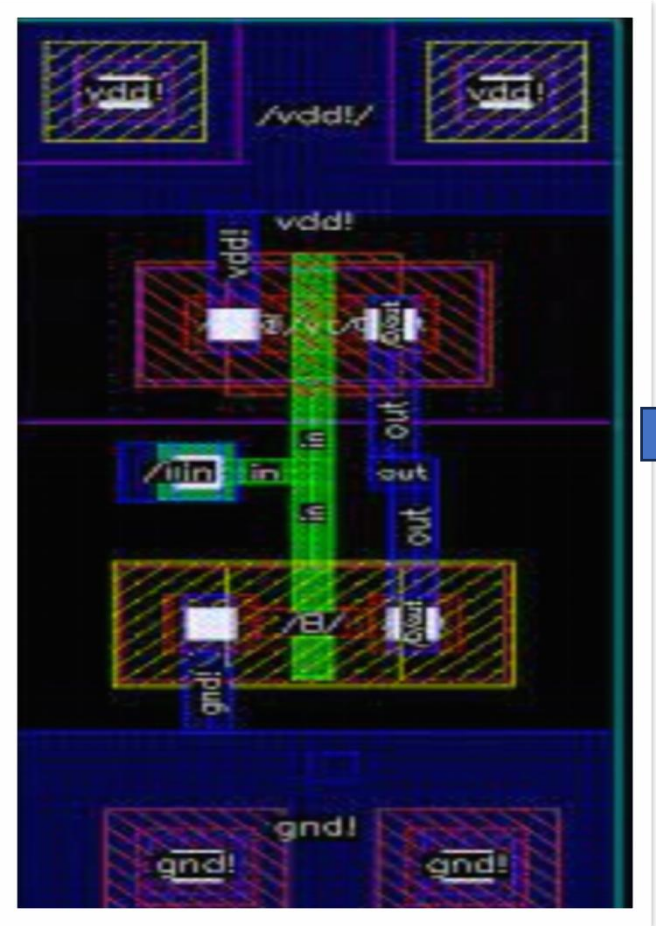
- Rows of standard cells with interconnection in between
- Custom blocks can also be embedded in a design
- Types, locations and interconnections of standard-cells are design specific
  - ➢ All layers have different masks for different designs

Workshop Objective

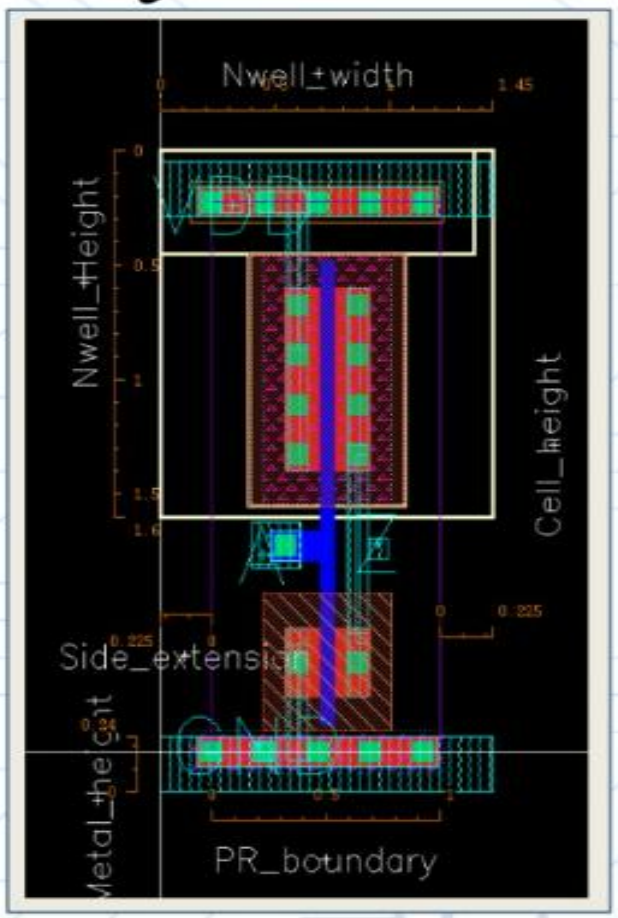
- Understand SCL design flow
- ASIC Flow - Role of Std cell library
- Importance of Different files associated with ASIC Flow

Outcome of Workshop

DVD Lab Outcome



Workshop Outcome



Layer	Dimension
Nwell	Width : PR + 0.450um
	Height : 1.6um (⅔ * 2.4um)
Metal Rail	0.24um (Via_width*4)
PR Boundary	Ciel(cell_width)
Cell Height	2.4 um
Cell extension	0.225 um

Outcome

Hands-on experience of SCL using Cadence tool chain.

VLSI Design Flow: RTL - GDSII

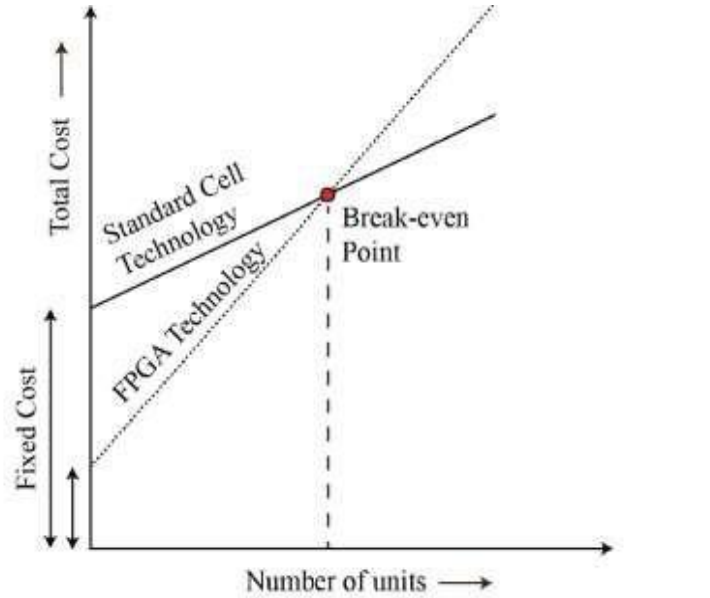
Comparison of Design style

	Full-custom design	**Standard-Cell based design**	**Gate-array based design**	**FPGA based design**
Description	Design specific customization at the level of transistors and layout	Pre-characterized cells/macros instantiation and interconnect design specific	Transistors predefined on wafer, interconnect design specific	Programming logic blocks and interconnect
Design effort	Highest	High	Lower	Lower
Custom Mask Layers	All	All	Top few layers	None
Performance, Power, Area	Best	Very Good	Comparatively Inferior	Comparatively Inferior

VLSI Design Flow: RTL - GDSII

Economics of Integrated Circuits: Comparison

	Standard-cell based design	**FPGA-based design**
Fixed Cost	High: designing cost, tools, mask	Low: tools for programming
Variable Cost	Low: cost of die (small die size, higher yield)	High: cost of die (large die size, low yield)



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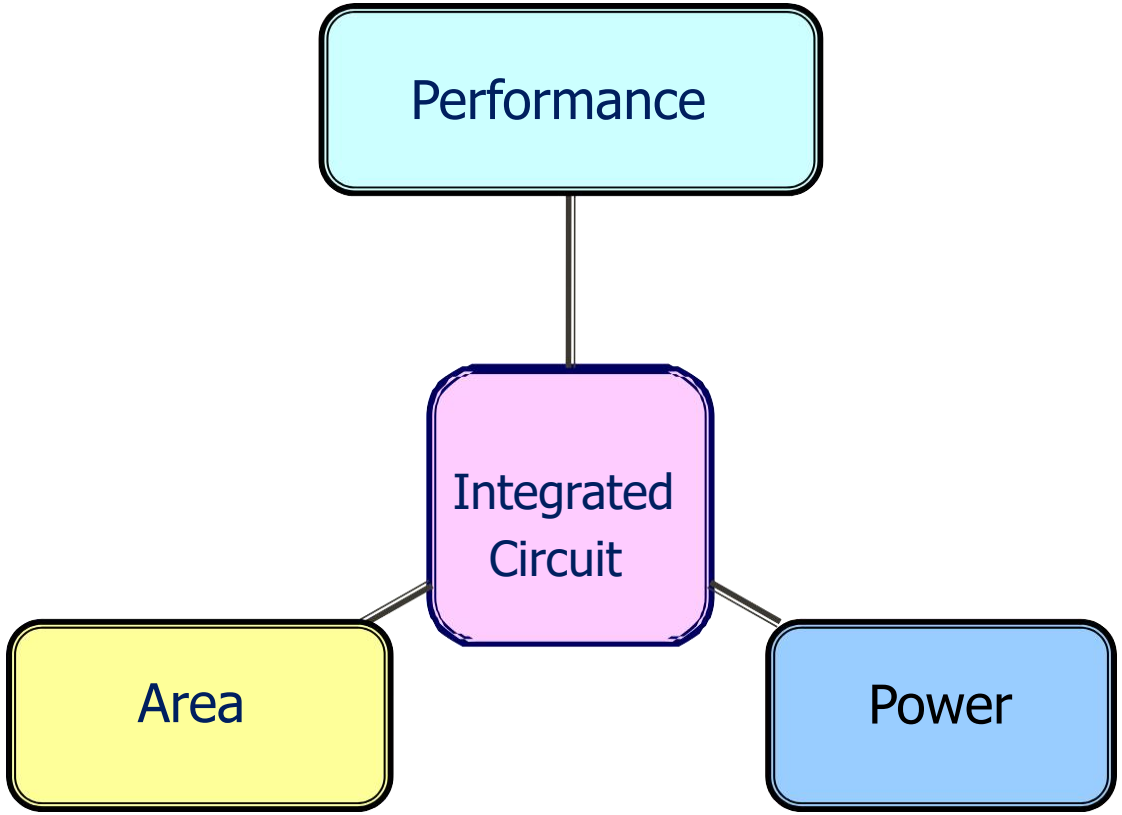
For small volume FPGA is better, for large volume standard-cell based design is better.

VLSI Design Flow: RTL - GDSII

Figures of Merit (FoMs) (1)

- How do we assess the "***goodness***" of an IC?

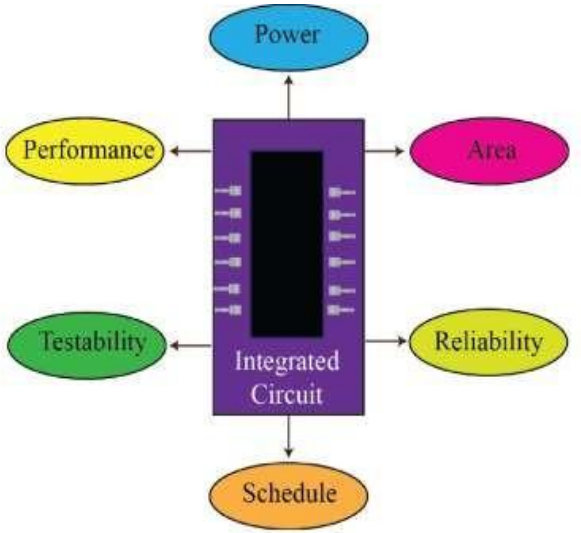
- **Power, Performance, Area (PPA) measure**
  - Power: sum of static and dynamic power consumed by an IC
  - Performance: maximum frequency of clock at which an IC will work
  - Area: area of the die for an IC
- Example: $(1\ W, 2.0\ GHz, 1\ mm^2)$



VLSI Design Flow: RTL - GDSII

Figures of Merit (FoMs) (2)

- Other FOMs:
  - Testability
  - Reliability
  - Schedule



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- Figures of Merit are also called Quality of Result (QoR) measure
- Improving one measure might adversely affect other measure(s)
  - Some measures might be required to be **traded-off**

- Mathematical optimum FoM for a given design is rarely known or achieved
- Goal of a design flow is to find one of the feasible solutions with acceptable FoM

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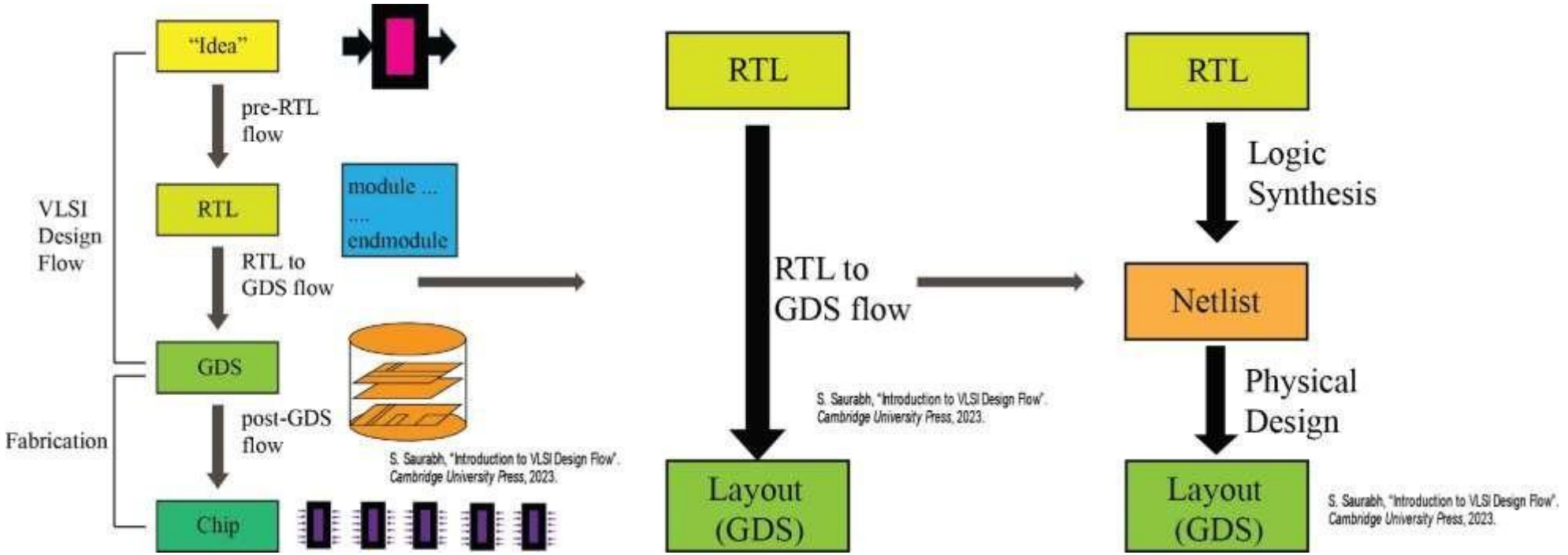
Introduction to Logic Synthesis

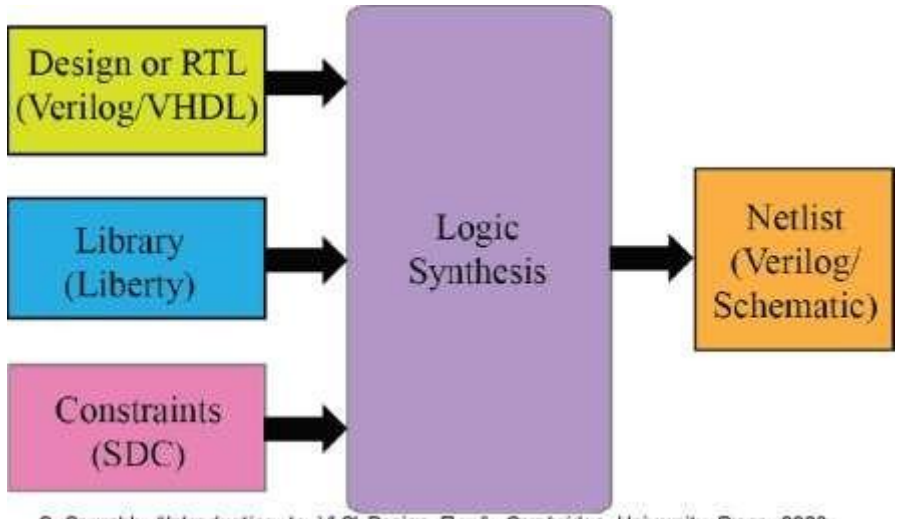
VLSI Design Flow: RTL - GDSII



VLSI Design Flow: RTL - GDSII

Logic Synthesis

Logic Synthesis: the process by which RTL is converted to an equivalent circuit as the interconnection of logic gates



S. Saurabh, "Introduction to VLSI Design Flow", *Cambridge University Press*, 2023.

- **RTL**: given design (Verilog, VHDL)
- **Library**: standard cells and macros (Liberty)
- **Constraints:** design goals, expected timing behavior, environment (SDC)
- **Netlist**:
  - Interconnection of logic gates
  - Usually represented using Verilog constructs or schematic

VLSI Design Flow: RTL - GDSII

Logic Synthesis: Illustration

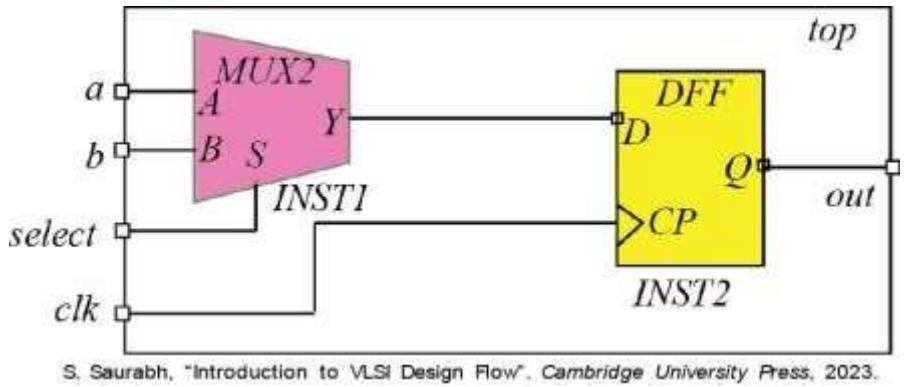
```
module top(a, b, clk, select, out);

    input a, b, clk, select;
    output
    out; reg
    out; wire
    y;

    assign y = (select) ? b : a;

    always @(posedge clk)
        begin
            out <= y;
        end

endmodule
```



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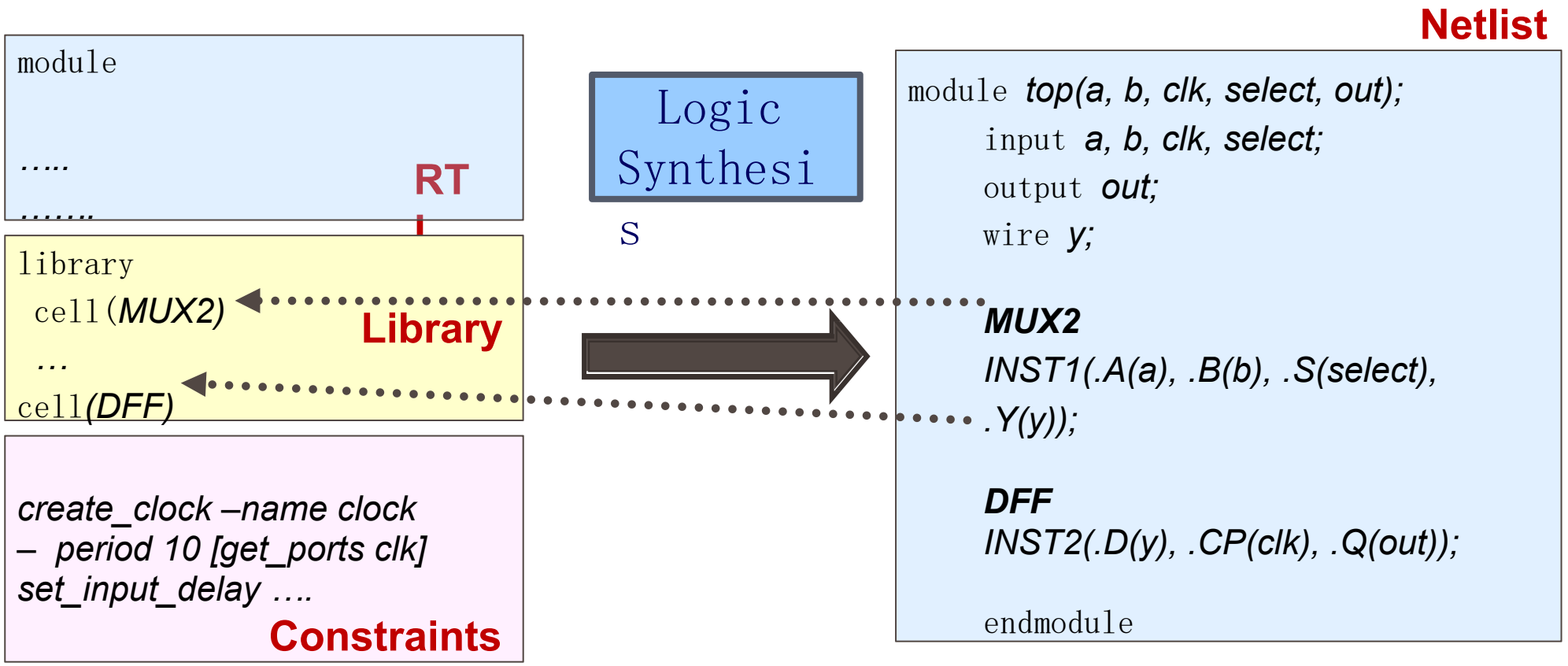
```
module top(a, b, clk, select, out);
    input a, b, clk, select; output
    out;
    wire y;

    MUX2 INST1(.A(a), .B(b), .S(select), .Y(y));
    DFF INST2(.D(y), .CP(clk), .Q(out));

endmodule
```

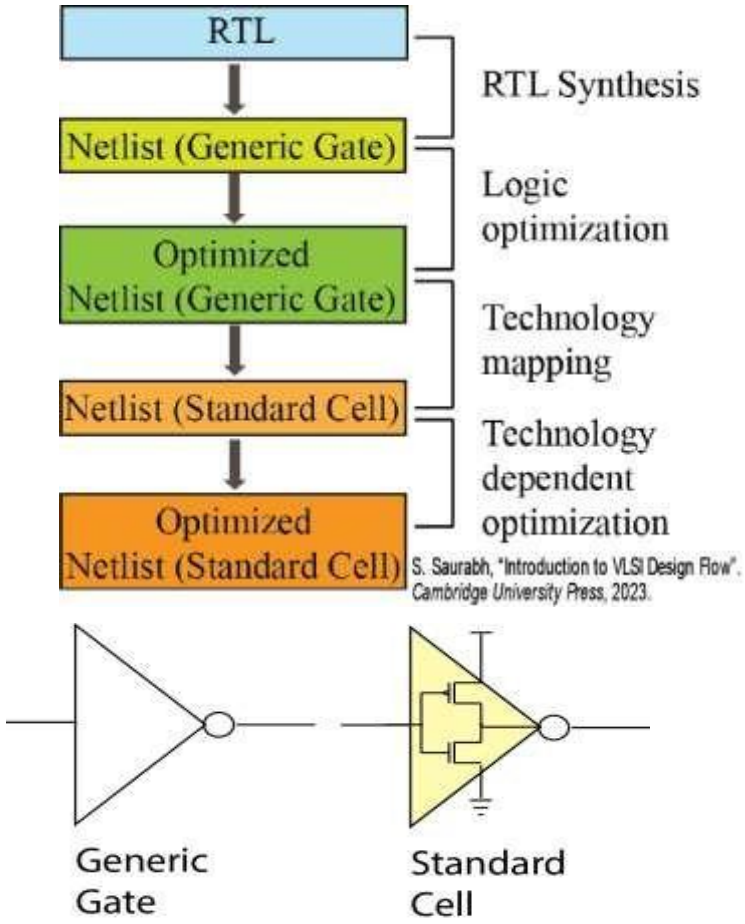
VLSI Design Flow: RTL - GDSII

Logic Synthesis: Inputs and Outputs



VLSI Design Flow: RTL - GDSII

Logic Synthesis Tasks: RTL Synthesis



RTL synthesis:

- Initial part of logic synthesis consisting of translating an RTL to a netlist of generic logic gates

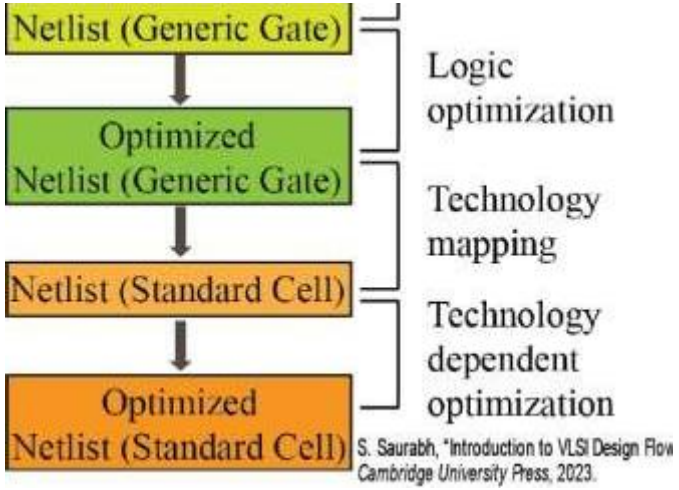
Generic Logic Gates

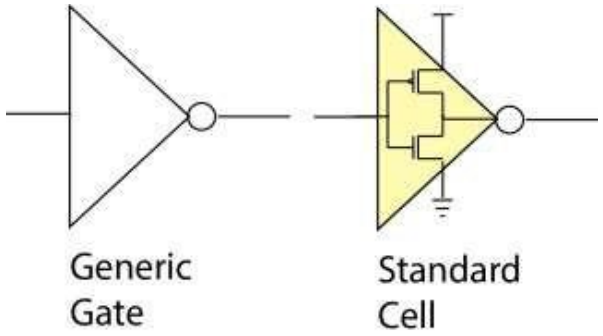
- A generic logic gate has a well-defined Boolean function.
  - AND, NAND, XOR, multiplexer, demultiplexer etc.
  - Latches and flip-flops.
- Does not have a fixed transistor-level implementation
  - Does not have a well-defined area, delay, and power attributes

Logic Optimization: Optimizations on a generic gate netlist is Typically area-driven

VLSI Design Flow: RTL - GDSII

Logic Synthesis Tasks: Technology Mapping and Optimization





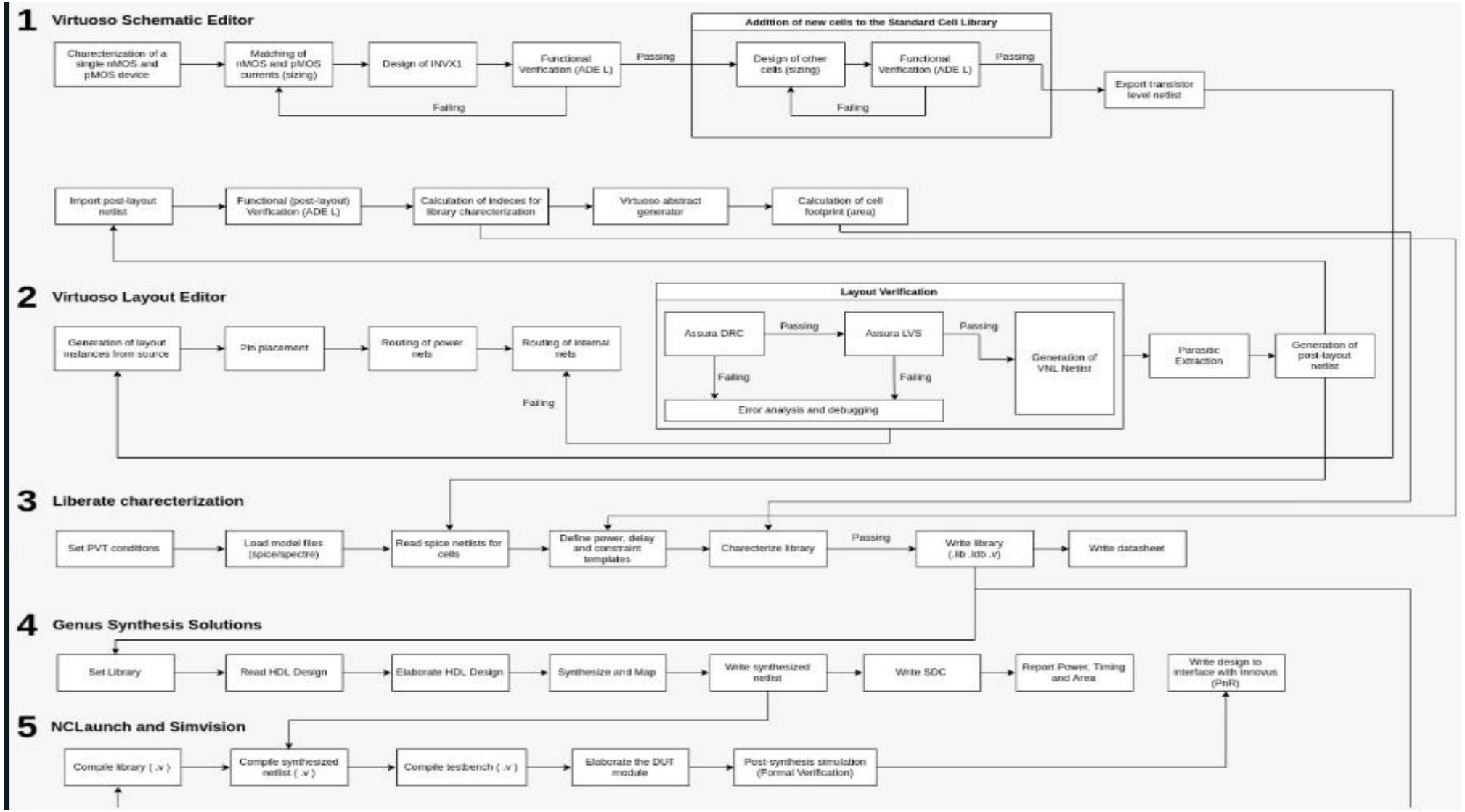
Technology Mapping:

- Map a netlist consisting of generic logic gates to the standard cells in the given technology library
- Obtain a netlist consisting of standard cells

Technology-dependent optimization:

- PPA can be estimated more accurately after technology mapping
- Perform timing, area, and power optimizations over netlist consisting of standard cells

Hands-on session : Day1



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