Centre for Heterogeneous and Intelligent Processing Systems

Department of ECE | PES University | Electronic City Campus

Presents

Two Day Workshop on

Standard Cell Design, Characterization and Synthesis

January 19th and 20th, 2024, PESU - EC Campus

PES UNIVERSITY

CELEBRATING 50 YEARS

Standard Cell Design, Characterization and Synthesis

Centre for Heterogeneous and Intelligent Processing Systems

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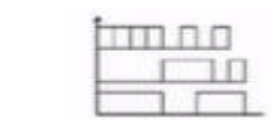
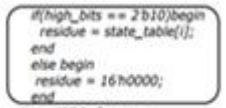
Standard Cell-based ASIC Design Flow



Pre-Layout Simulation

Design Specifications

Design Entry (Schematic/HDL

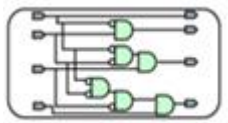


HDL Code

Synthesizer (RTL complier /genus)

Standard Cell Library

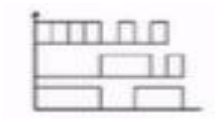
Technology Information (45n/90n/ 180n)



net list (Shows Inter connections of Different Logical blocks)

System Partitioning

A

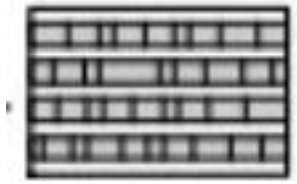


Post Layout Simulation

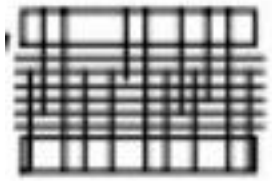
A

Floor Planning

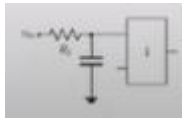
Placement



Routing



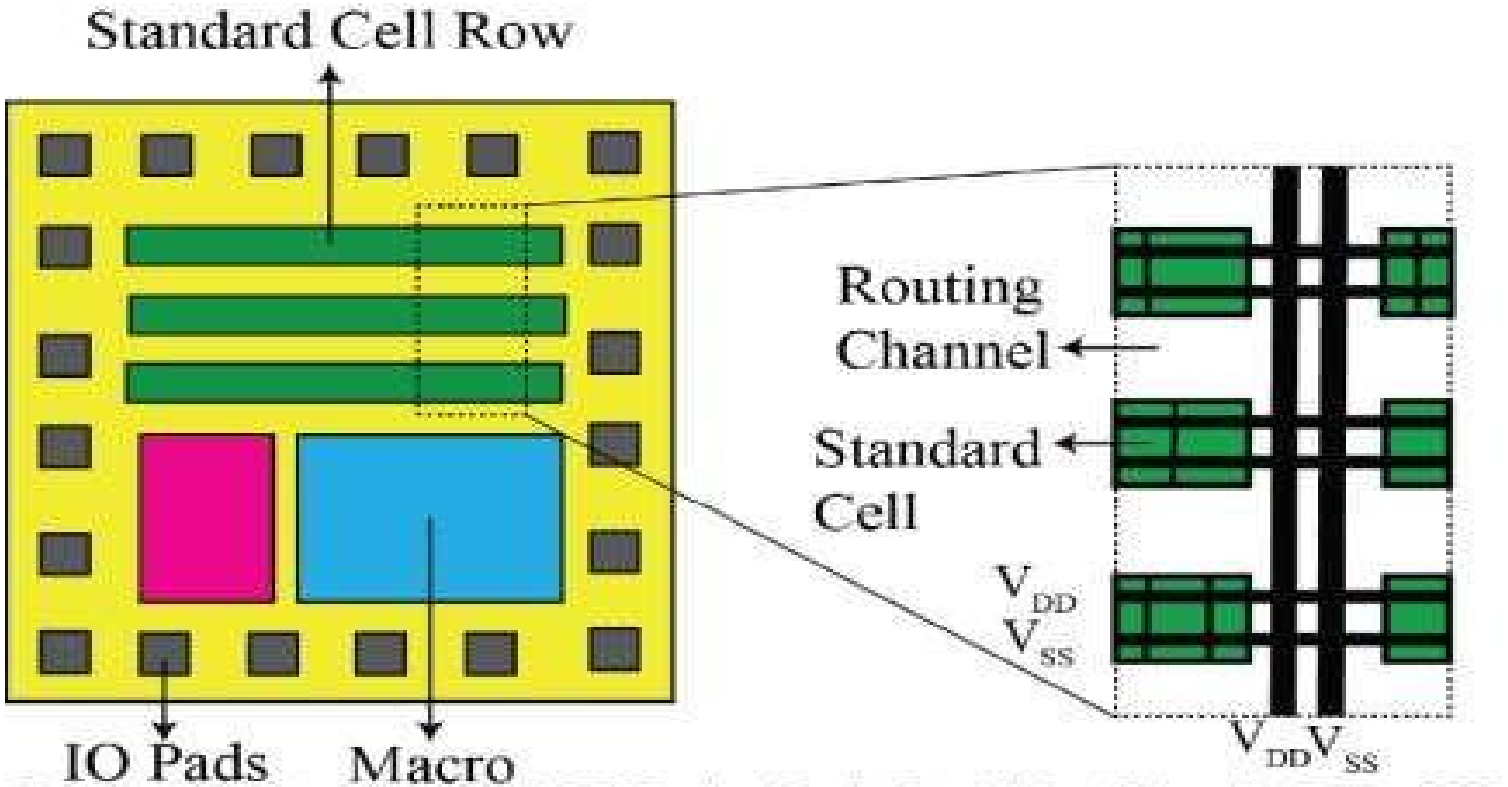
Circuit Extraction



Design Rule Checking

Fabrication

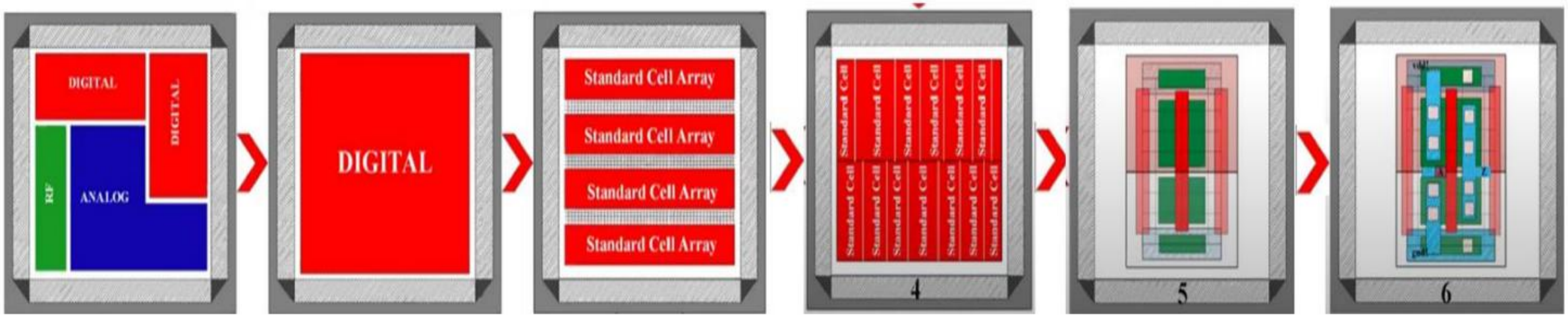
Standard Cell-based ASIC Design Flow



S. Saurabh, "Introduction to VLSI Design Flow". *Cambridge University Press*, 2023.

- **Standard Cells**: simple cells such as AND, NAND, flip-flop etc. that are optimally designed and modeled in a library, fixed height
- **Macros:** complex cells such as full-adder, multiplier, memory etc.
- Allows high degree of automation

Standard Cells in CHIPS (Digital)



1 2 3 4 5 6

- Standard cell methodology is widely used in ASIC design for efficiency and flexibility.
- ASIC library kits contain pre-defined cells for automated design and optimization.
- Multiple cell variations allow trade-offs between area, speed, and power.
- Challenge: Identifying specific cells within large libraries can be difficult.
- Solution: Standardization across libraries for easier use.

Standard Cells

What is a Standard cell why do we need it

- Designers work at **a higher level using hardware description languages (HDL) like Verilog or Very High-Speed Integrated Circuit HDL (VHDL).**
- Implementation at the device level involves converting **the design into an interconnection of simple, well-defined blocks**, akin to Lego toys.
- These **blocks, known as standard cells**, are crucial for achieving the final chip, and they must adhere to specific design rules.
- These Standard cells will have a standard height but can varying width. The height is fixed based on a Complex standard cell in the Library.
- Automated tools handle the interconnection process, ensuring that the final chip is DRC/LVS clean.
- Characterization of Standard cells is one of the important processes carried out in the process of designing and manufacturing the chip.

Standard Cells in CHIPS (Digital)

Standard cell Library?

The cells can be categorized as follows:

1) Logic Cells implementing Boolean logic.
2) Latches and Flip-flops to implement the state storage etc.
3) Clock Buffers (CLKBUF).
4) Regular Buffers/Inverters (BUF)
5) tri-state buffers (TBUF).
6) Special Cells – Tie, Filler, Tap, Boundary Cells

Cell Name Rules

The cell name is followed by

1) the **number of inputs it has,** and
2) ending with X1, X2, etc., indicate relative drive strengths.

Example: NAND2X1 Indicates Standard Cell NAND with 2 inputs and driving capacity of X1

Slide 51 and 52 to be added

Standard Cell Naming Convention

Objective: Ensure clarity, consistency, and efficiency in library management and design workflows.

Importance:

- **Reduced ambiguity:** Consistent naming helps engineers across departments easily identify and reference cells.
- **Streamlined communication:** Common language facilitates collaboration and problem-solving during design.
- **Improved efficiency:** Avoids redundancy and ensures efficient utilization of library resources.

Key Elements:

- **Logic Function:** Clearly defines the cell's functionality (e.g., NAND2, DFF).
- **Number of Inputs:** Specifies the number of input signals the cell accepts.
- **Drive Strength:** Indicates the cell's ability to drive subsequent logic (e.g., X2, X0P5M).

Naming Table

Category	Naming Standards	Example(s)
Combinational Cells	• Function prefix (e.g., NAND, OR) • Input count suffix (e.g., 2, 3) • Optional drive strength suffix	NAND2X4, AOI22X0P5M
Sequential Cells	• Function prefix (e.g., DFF, TFF) • Clock type suffix (e.g., C, P) • Optional drive strength suffix	DFFC1X2, TFFPX0P5M
Power Cells	• Function prefix (e.g., BUF, LDO) • Drive strength suffix	BUF1X2, LDOX0P5M

Category	Naming standards
Combinational	<logic><inputs>X<drivestrength>
Sequential	<Logic><special inputs><output>X<number>
Power cells	<function>X<pitchsize>

Naming Examples

Logic Function	Inputs	Drive	Cell Name
AND	2	1X	AND**2**X1
OR	3	2X	OR**3**X2
NAND	3	4X	NAND**3**X4

Storage Function	Output	Drive Strength	Cell Name
DFF	Q	1X	DFF**Q**X1
DFFN	QN	1X	DFFN**QN**X1
DFF	Q and QN	1X	DFFX1

Storage function	Edge Sensitivity	Set	Reset	1X Drive	Cell Name
DFF	-ve	X	X		DFFN**SR**X1
DFF	+ve	X	X		DFF**SR**X1
JKFF	+ve		X		JKFF**R**X1

Logic Function	Inputs	Drive Strengths	Cell Name
AND	2	1X	AND2**X1**
AND	2	2X	AND2**X2**
INV	1	1X	INV**X1**

Standard Cells in CHIPS (Digital)

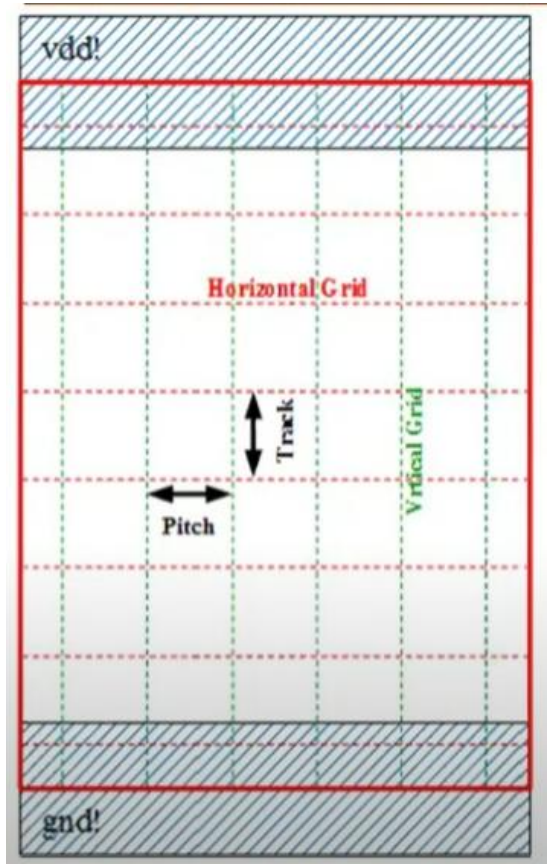
Standard cell Library?

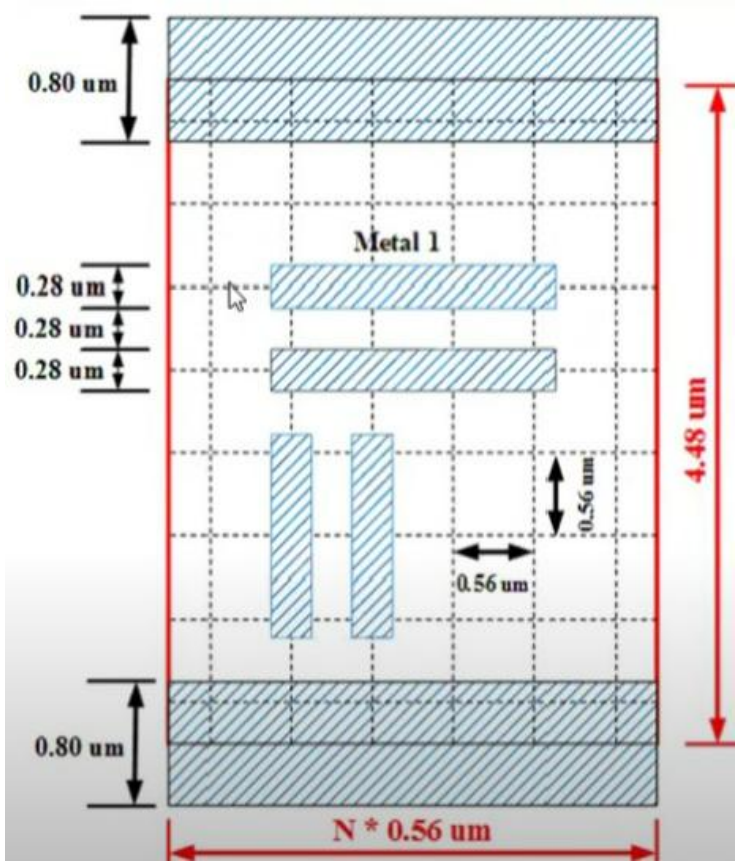
CELL NAME	FUNCTION
AND2X1	Y = A.B
AND2X2	Y = A·B
AOI21X1	Y=NOT(A·B + C)
AOI22X1	Y=NOT(A·B + C·D)
BUFX2	Y = A
BUFX4	Y = A
CLKBUF1	Y = A
CLKBUF2	Y = A
CLKBUF3	Y = A
DFFNEGX1	D-Type Flip-flop with negative edge clock
DFFPOSX1	D-Type Flip-flop with positive edge clock
DFFSR	D-Type Flip-flop with positive edge clock and negative SET and negative RESET
FAX1	YS = A B C\nYC = A·B + B·C + C·A
FILLCELL_1,2,4,8,16	Filler Cells
HAX1	YS = A B\nYC = A·B
INVX1	Y = NOT(A)
INVX2	Y = NOT(A)
INVX4	Y = NOT(A)

LATCH	D-Type Latch with positive clock level
MUX2X1	2 to 1 Multiplexer
NAND2X1	Y = NOT (A·B)
NAND3X1	Y = NOT (A·B·C)
NOR2X1	Y = NOT(A+B)
NOR3X1	Y = NOT(A+B+C)
OAI21X1	Y = NOT((A+B) ·C)
OAI22X1	Y = NOT((A+B) ·(C+D))
OR2X1	Y = NOT(A+B)
OR2X2	Y = NOT(A+B)
TBUFX1	Y = A·EN; Y = HiZ for(NOT E)
TBUFX2	Y = A·EN; Y = HiZ for(NOT E)
XNOR2X1	Y = NOT (A B)
XOR2X1	Y = A B

Standard Cells: Design Rules

Standard cell height can be measured as the number of tracks multiplied by track height.





Standard Cell height =Number of tracks x track height = 8 x 0.56 =4.48um

Metals are routed only on the grids

The minimum metal width is half of the track height Ex: 0.56/2 =0.28

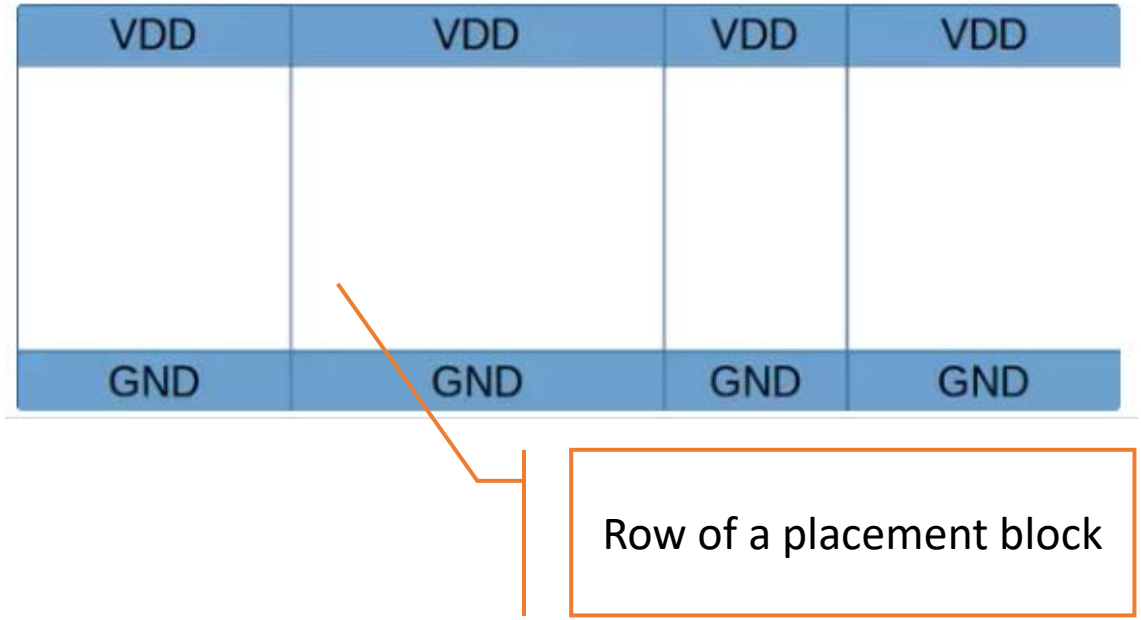
The minimum metal spacing is half of the track height. Ex: 0.56/2 = 0.28

Standard Cells: Design Rules

There are three main considerations in the Standard cell design. They are Height, Track and Pitch

Height : What is Height and Width of Each cell ?

- All cells in a standard cell Library should **have the same height and with varying Width.** The **cells are placed in rows of the placement blocks** in chip-level or block-level designs.
- The Standard cell height will be equal to the **height of the placement rows (track)** and the **width will vary according to the area and complexity that the cell has**.
- The height of the placement Row is **defined by the Largest cell in the standard Library.**
- Both **Height and width parameters should be multiple of Pitch (P)**

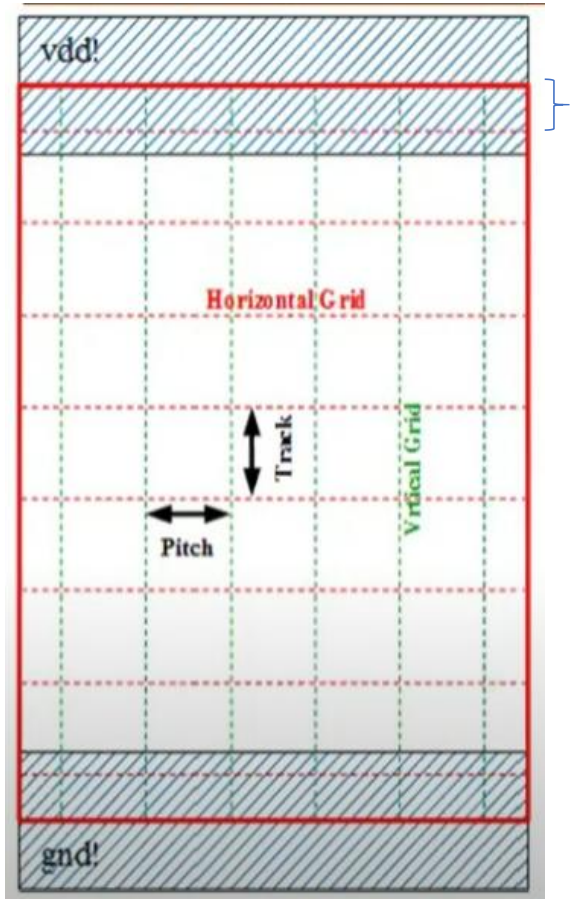


Standard Cells: Design Rules

There are three main considerations in the Standard cell design. They are Height, Track and Pitch

Track : The minimum spacing between the horizontal grids is 1 track

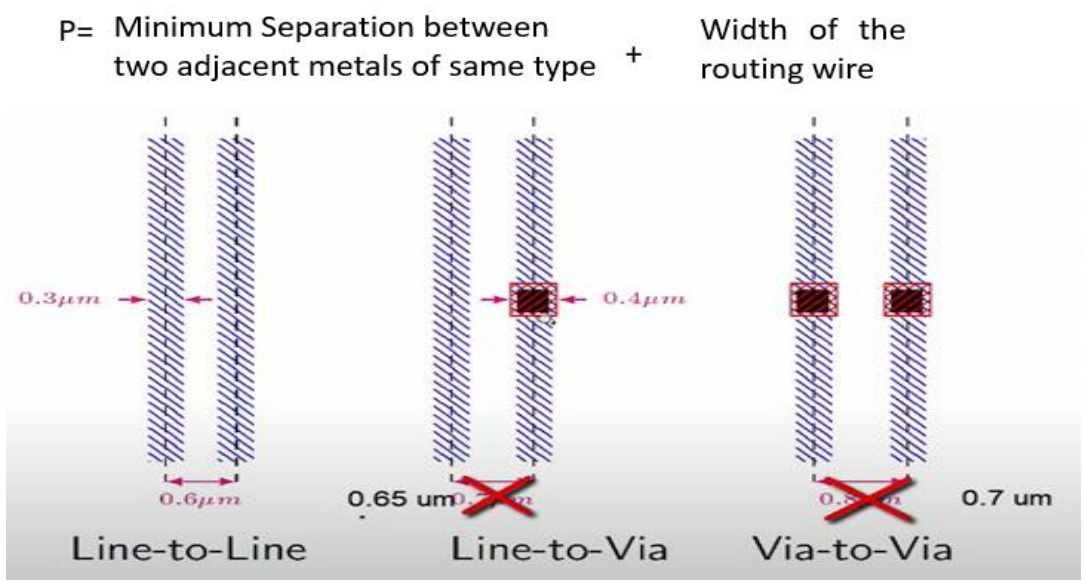
- **Track is the unit that is used to define the Standard cell height.**
- There can be various tracks such **as 12-track, 9-track, 7-track, 6.5 track** etc.
- A 12-track Standard cell is taller than a 9-track Standard cell. In 12-track more of the space is available for routing. These are not dense.
- **Lower tracks usually have less height** and they are **dense and hence used for dense-based designs.**
- **Higher track Standard cells have more area** hence the performance of this kind of **cells is less than lower track Standard cells.**

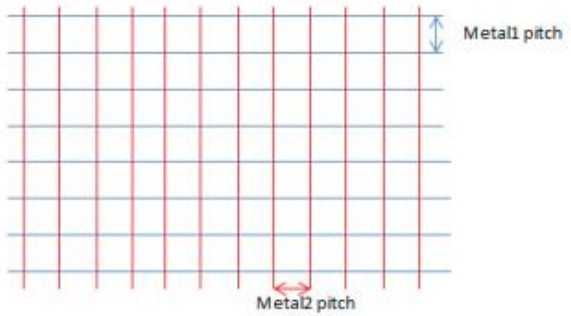


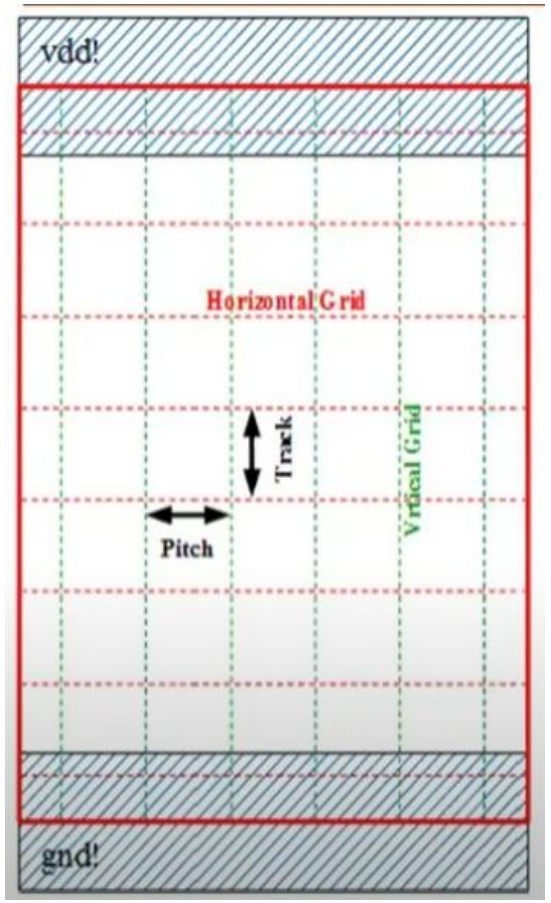
Standard Cells: Design Rules

Pitch : What about Pitch Size and How it is used in Routing?

- Pitch is an important terminology used in the Standard cells: the minimum spacing between the vertical grid line **pitch**







Standard Cells: Design Rules

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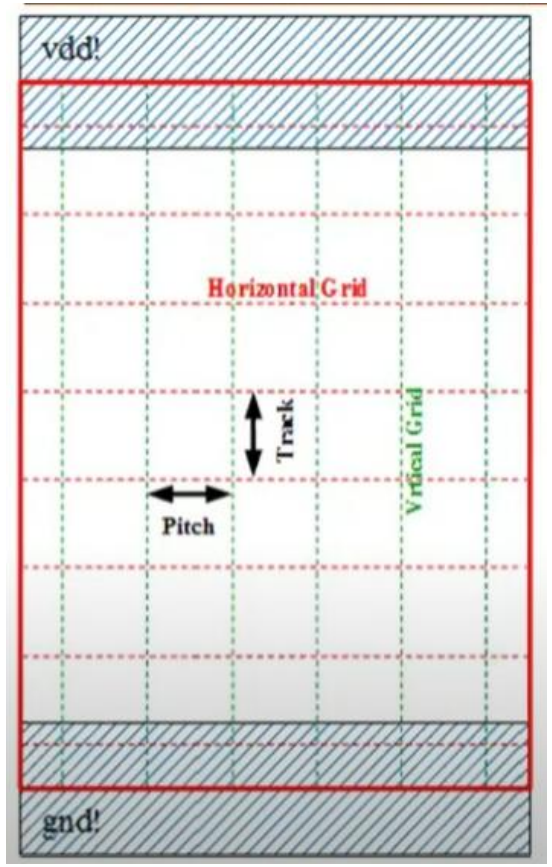

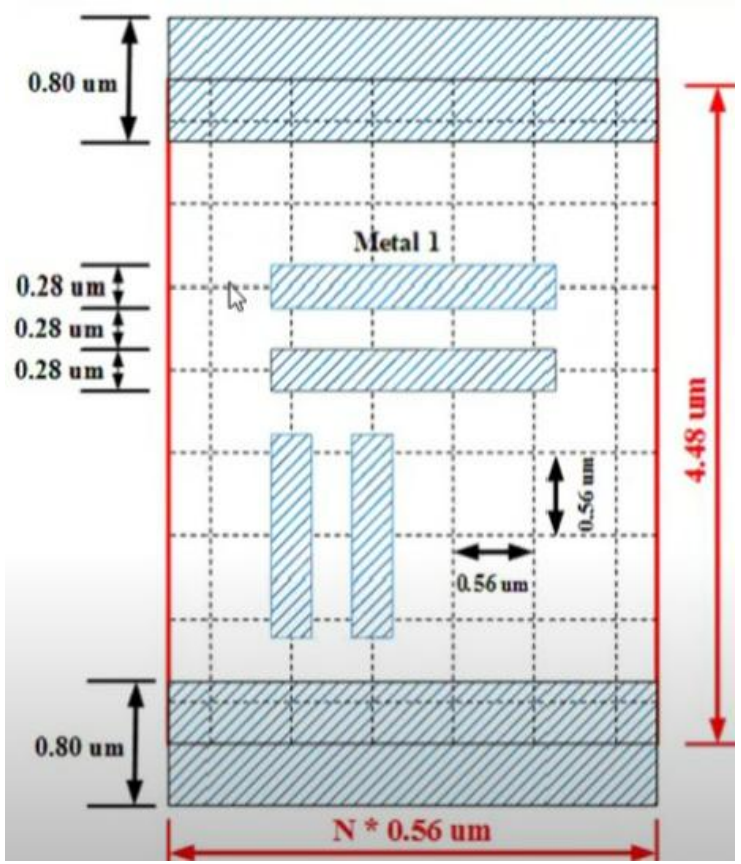

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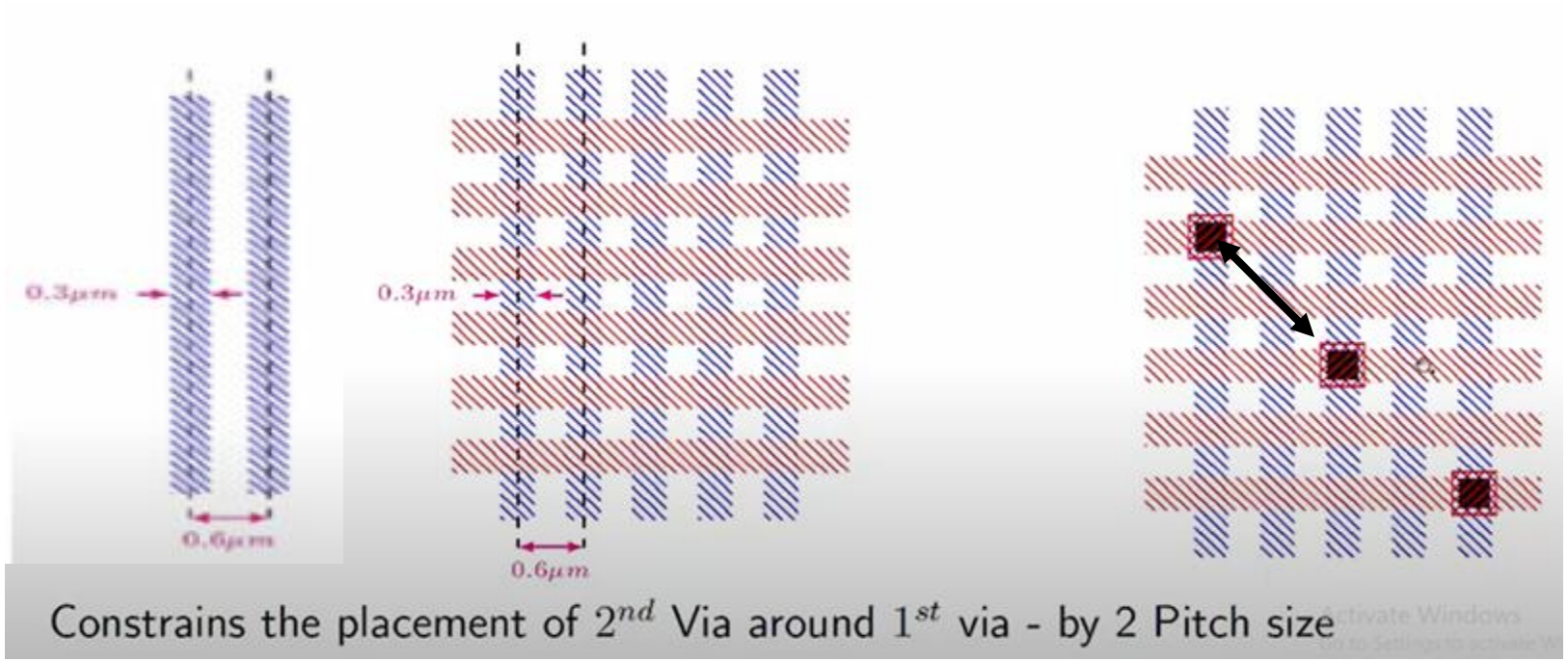
Standard Cells: Design Rules

Different Schemes used in defining Pitch Size

Line to Line

P= Minimum Separation between two adjacent metals of same type + Width of the routing wire



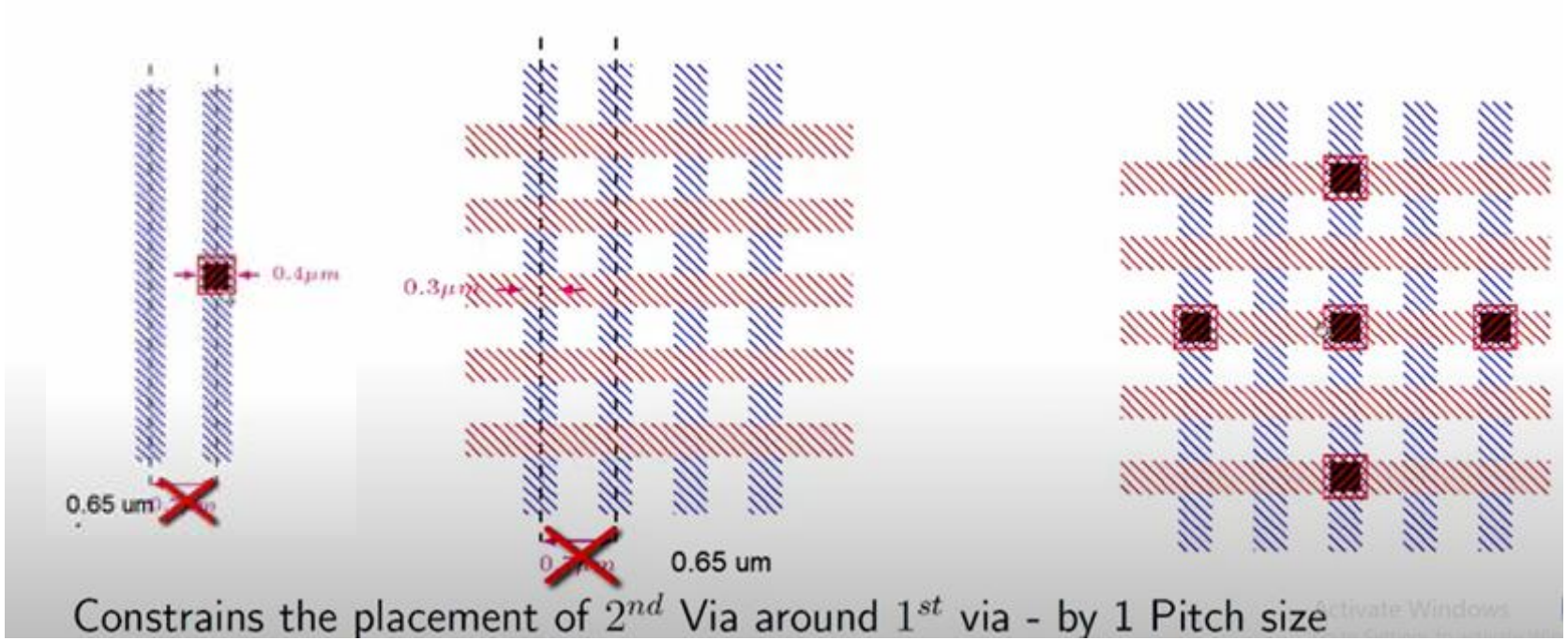
- Metal 1 routing wire width is 0.3uM and Minimum separation is two adjacent metal 1 layers is 0.3uM.
- The Pitch size is 0.6uM
- In this scheme, it will have High routing **grid density but the Via's should be placed with a separation of 2 pitch size vertically as well as horizontally.**
- For Simple circuits involving few Vias this scheme can be used.

Standard Cells: Design Rules

Different Schemes used in defining Pitch Size

Line to Via

P= Minimum Separation between two adjacent metals of same type + Width of the routing wire



Constrains the placement of 2^{nd} Via around 1^{st} via - by 1 Pitch size

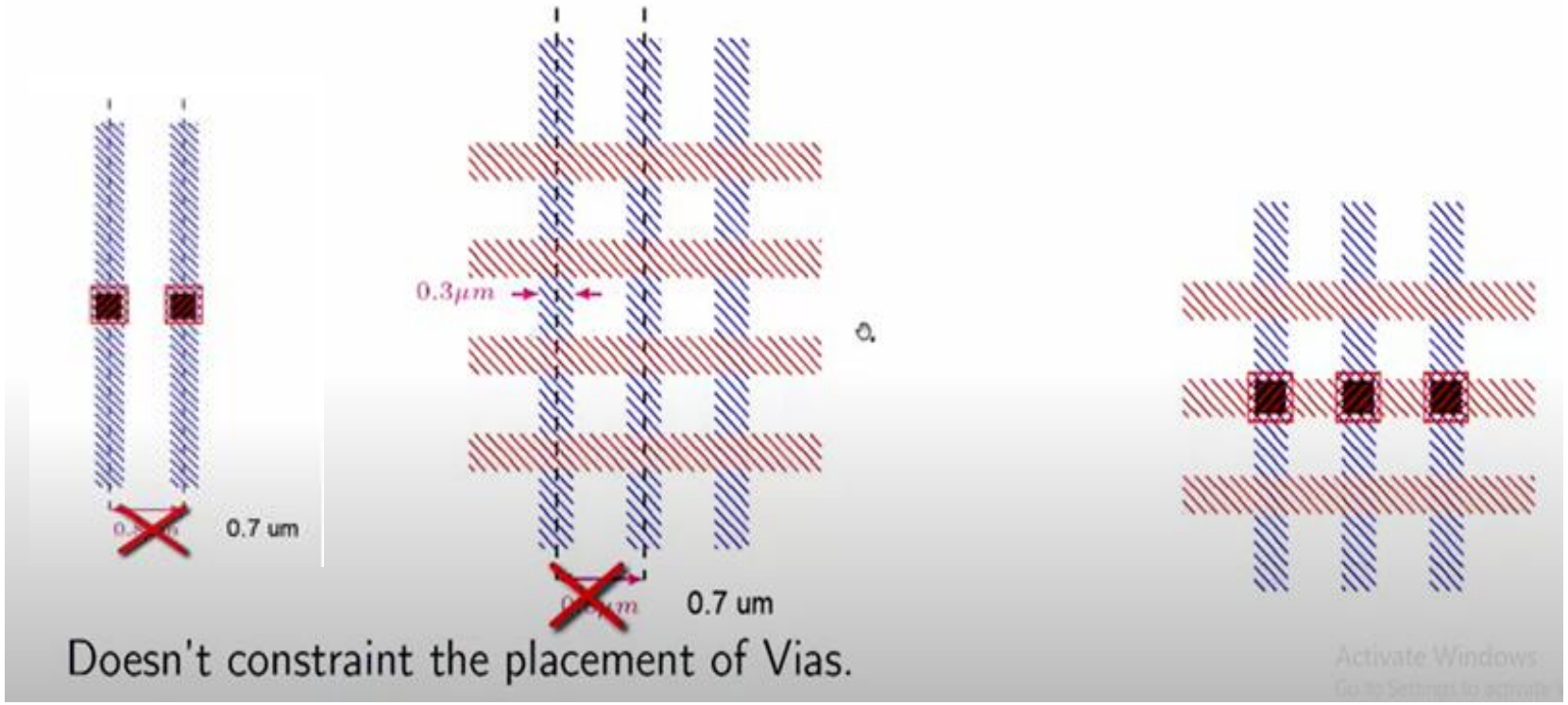
- Metal 1 routing wire width is 0.3uM and Metal1-2 Via is of 0.4uM.
- The Pitch size is 0.65uM
- In this scheme, it will have Medium routing grid density but the Via's should be placed with a separation of **2 pitch sizes vertically or horizontally**.
- For circuits involving average Vias this scheme can be used.

Standard Cells: Design Rules

Different Schemes used in defining Pitch Size

Via to Via

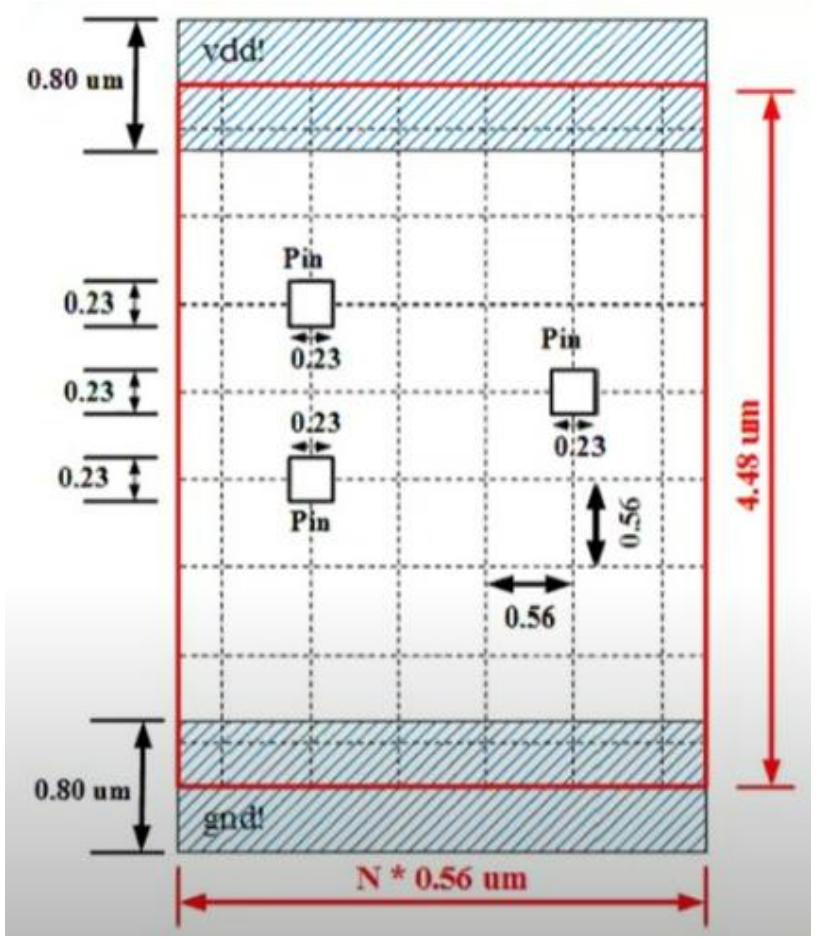
P= Minimum Separation between two adjacent metals of same type + Width of the routing wire



- Metal 1 routing wire width is 0.3uM and Metal1-2 Via is of 0.4uM.
- If two Via are adjacent, then the Pitch size is 0.7uM
- In this scheme, it will have Medium routing grid density but the **Via's should be placed with a separation of 1 pitch size vertically or horizontally.**
- For circuits involving HIGH Vias (more IOs) this scheme can be used.

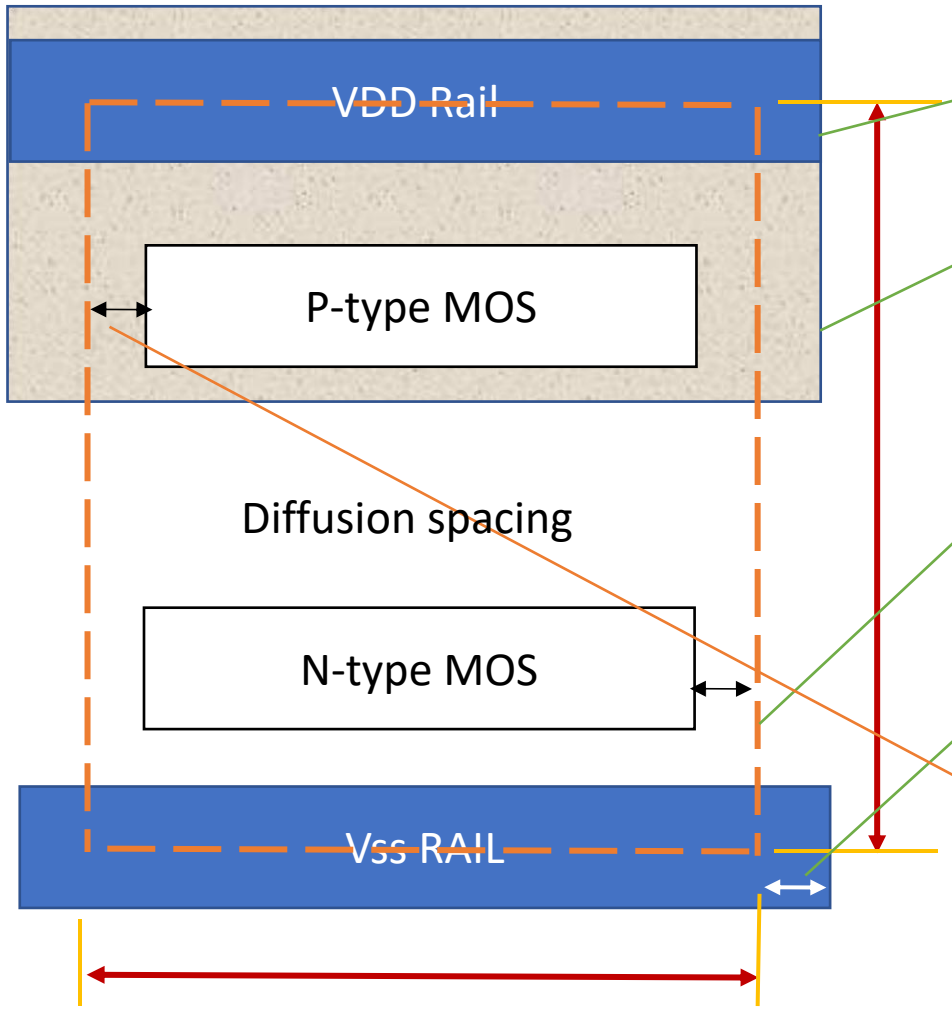
Standard Cells: Design Rules

Pin Position



Pins to be positioned on the crossing points of grids

Standard Cells: Design Rules



VDD Rail – Generally (3-5)times the Minimum width of the Metal1. Think Vdd and Gnd lines are used to provide adequate current to ALL the cells in the ROW

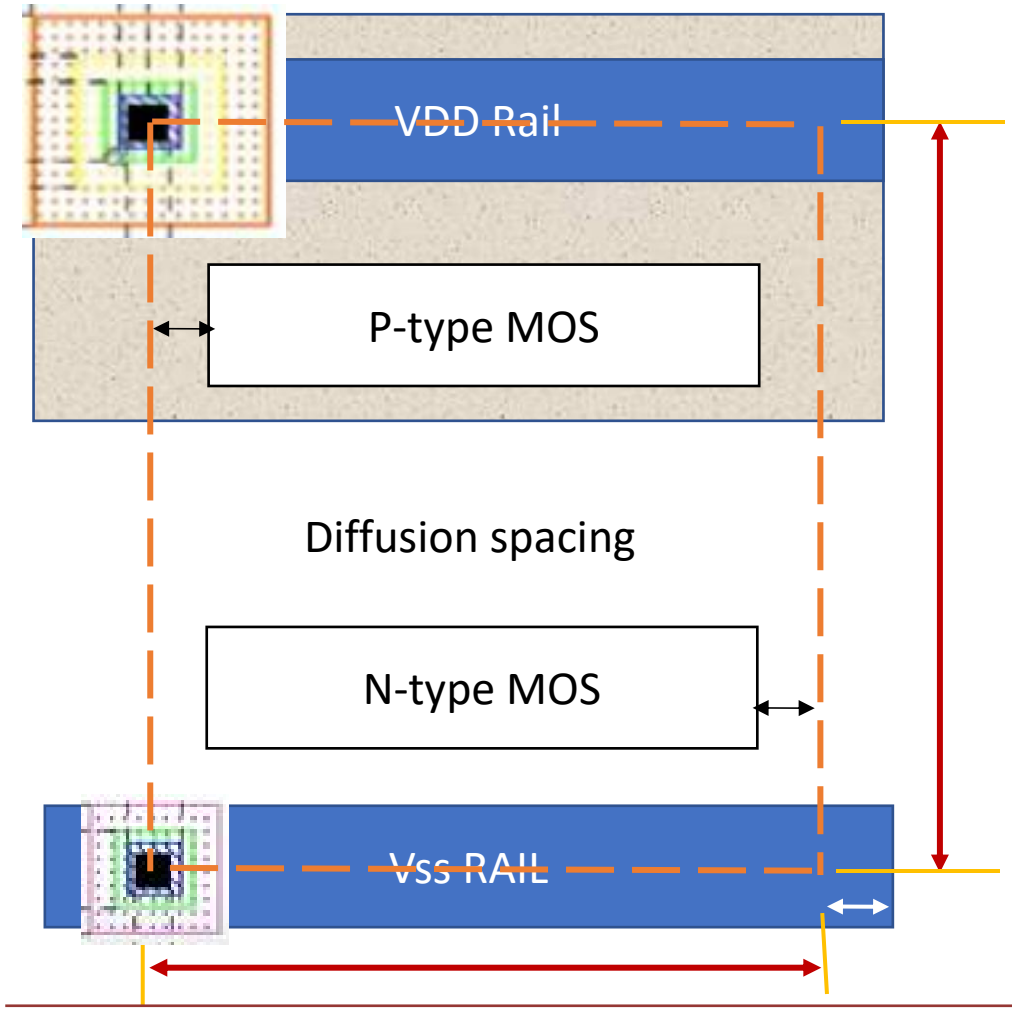
N well extension Outside PR boundary: Nwell is extended so that N-well of neighboring PMOS cells merges – i.e., Common N-Well

The PR boundary : This gives size of cell- It's height is taken from center of VDD and GND line and width by excluding the extensions

Outside PR boundary, The VDD and GND lines are extended which helps to abut the neighboring cells automatically

Spacing between PR boundary and n/P type active region is to provide spacing/isolation between neighboring standard cell MOS devices

Standard Cells: Design Rules



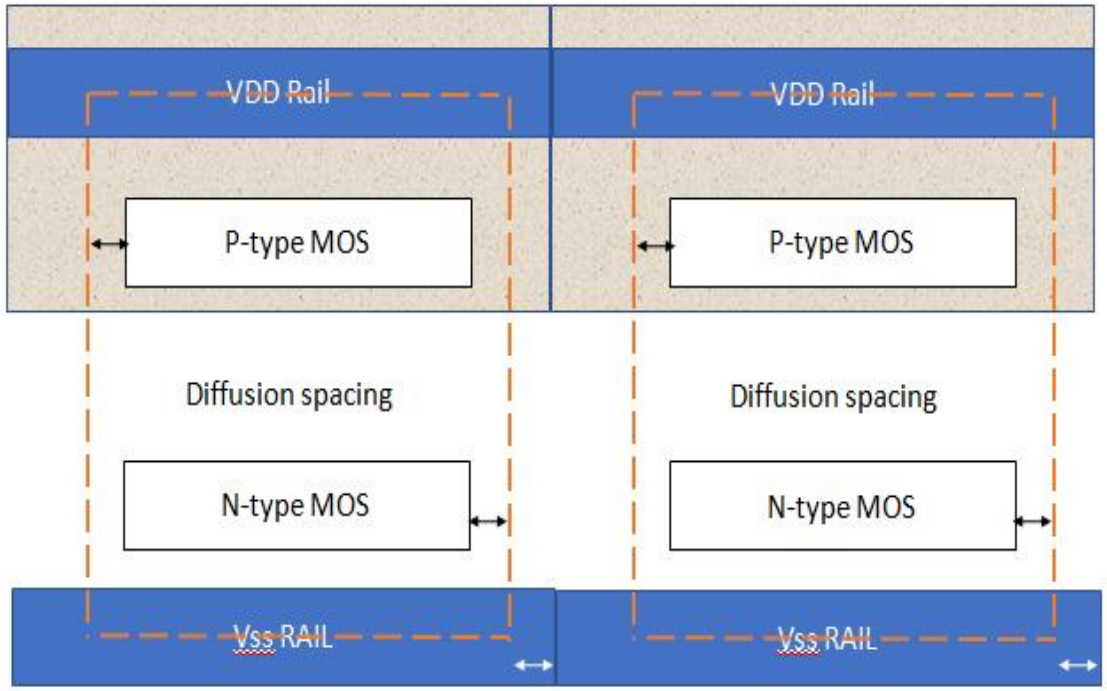
The M1_Nwell Via and M1_N+ diffusion Vias should be placed on the Left corners of the PR boundary.

The M1_Nwell Via placement leads to an extension of 0.8uM from PR boundary. Therefore VDD, GND, and N-well layers are extended by the same value.

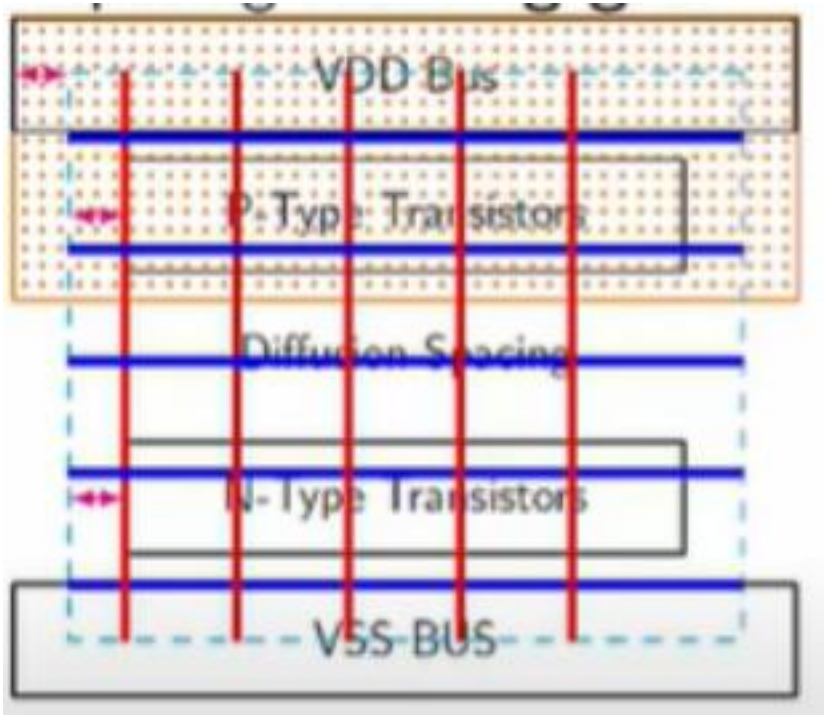
Standard Cells: Design Rules

Standard Cells – Abutment and Routing Grid

Imposing Abutment

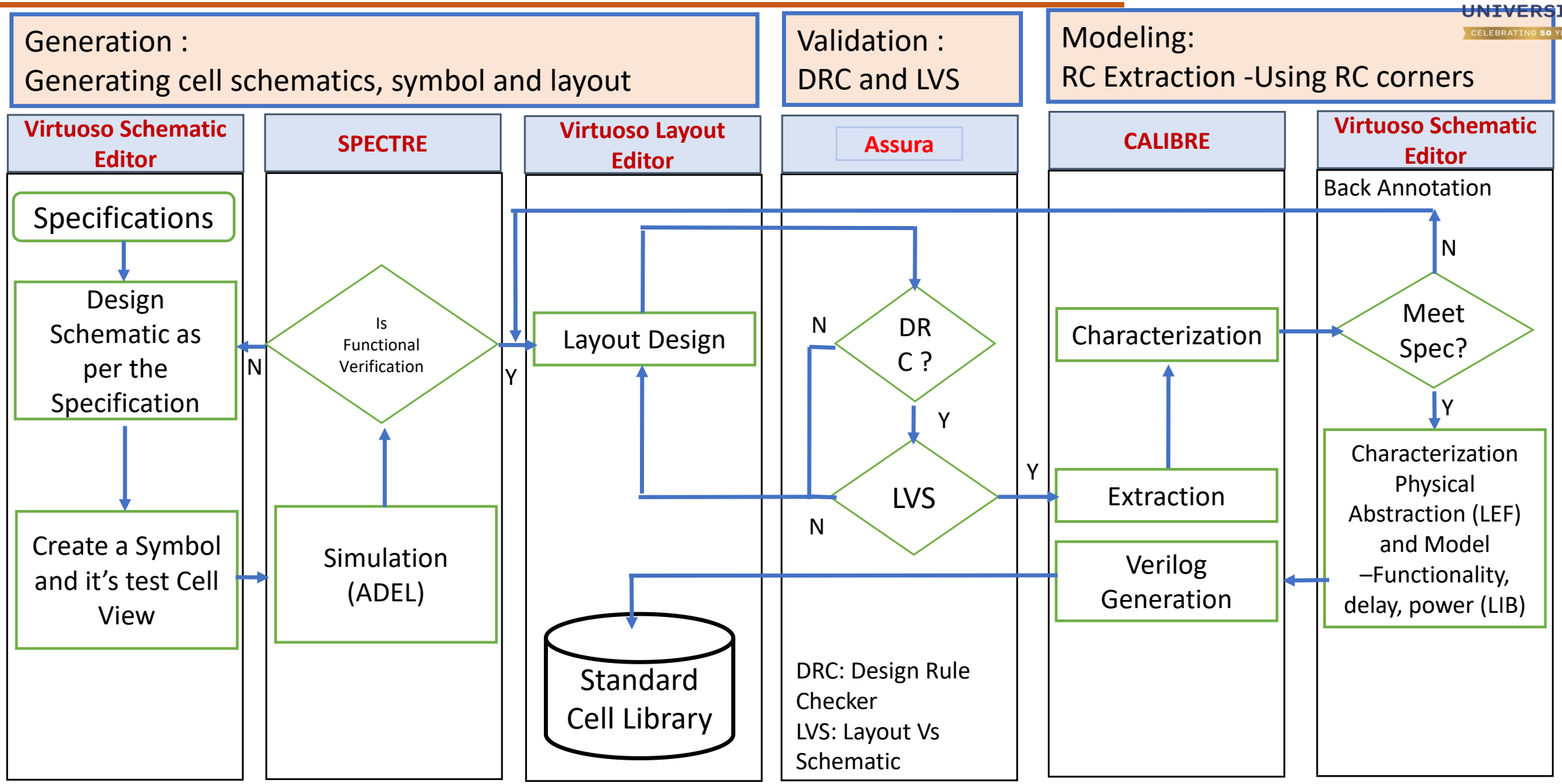


Imposing Routing Grid



Digital VLSI Design

Standard Cells - Characterization Steps

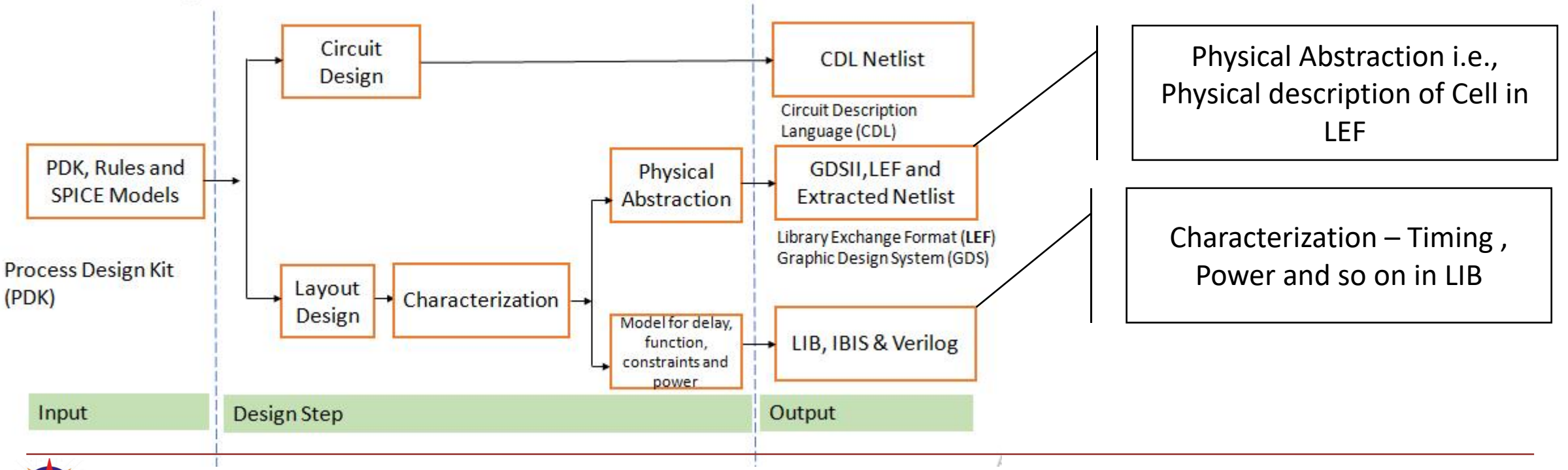


Standard Cells Characterization

Characterization of Standard cells will use

- ✓ Extracted **spice netlist** from layout,
- ✓ **Spice models** from Process Design Kit and
- ✓ **Characterization parameters** like **temperature, input slew, output loads, voltage supply**

The basic cell design flow contains:

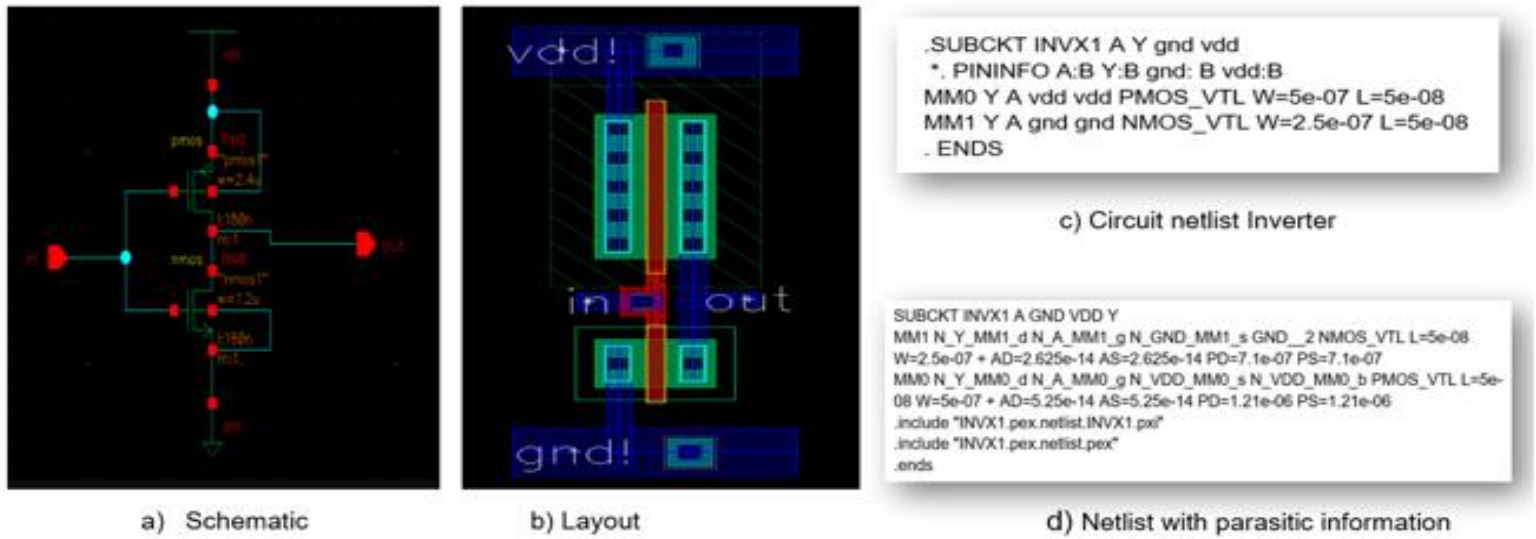


Standard Cells Information Required: In ASIC Design

Standard Cell library information required to implement an ASIC design is as follows

1. **Circuit Information:**

Circuit schematics, layouts, circuit netlists (derived from schematics), and parasitic extracted netlists (extracted from layouts) are essential.



a) Schematic b) Layout c) Circuit netlist Inverter d) Netlist with parasitic information

Figure 4: Circuit Information a) Schematic b) Layout c) Circuit Netlist d) Netlist with parasitic Information

The netlists are used for the following purposes:

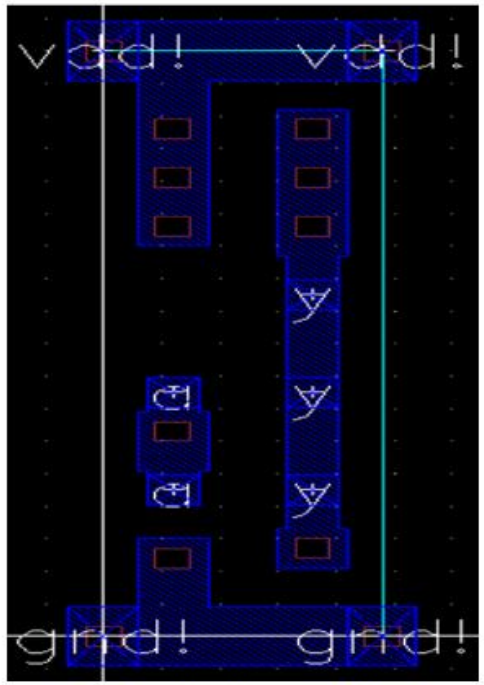
1. Schematic netlist - LVS.
2. Layout netlist - Timing extraction.

Standard Cells Information Required: In ASIC Design

Standard Cell library information required to implement an ASIC design is as follows

2. Abstracted Views of Standard Cells: Abstract views include

a) bounding dimensions,
b) Routing obstructions, and
c) Pin locations for each standard cell.



Standard Cells Information Required: In ASIC Design

Standard Cell library information required to implement an ASIC design is as follows

3. Timing, Power, Functionality, and Operating Conditions:

- Data provided in Synopsys Liberty format (*.lib file).
- Used by synthesizers and the Place and Route (P&R) tool.

4. Cell Models in Verilog/VHDL:

- Verilog/VHDL models are required for all standard cells.

Standard Cells: LEF file Generation

LEF File	
Header Part	Technological Information
Cell Descriptive Part	Standard Cell Information

Design Rules Related to Layers used in Place and Route (PAR) process like Minimum Metal Width, Space and so on

Library Designer defined rules like Pitch, Preferred Metal direction, Geometric Information of Vias used

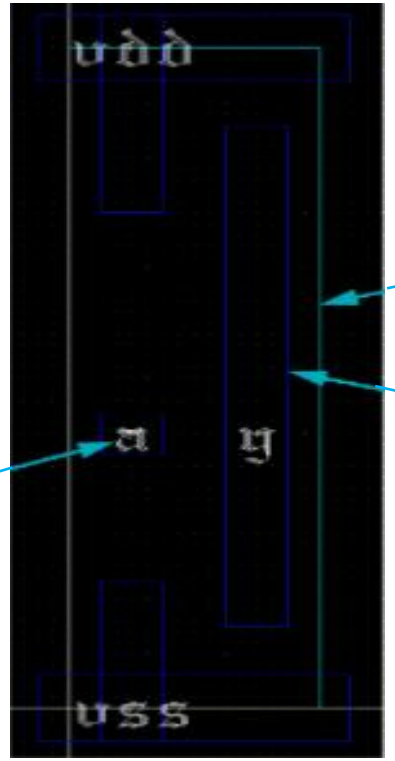
Optionally some electrical properties of layers like Maximum current , Resistance per square

```
LAYER Metal1
  TYPE ROUTING ;
  DIRECTION HORIZONTAL ;
  PITCH 0.6 0.6 ;
  WIDTH 0.3 ;
  SPACING 0.3 ;
  RESISTANCE RPERSQ 0.101 ;
  CAPACITANCE CPERSQDIST 0.000132 ;
  EDGECAPACITANCE 8.8e-05 ;
  MINIMUMDENSITY 0.25 ;
  ANTENNAMODEL OXIDE1 ;
    ANTENNAAREARATIO 200 ;
  DCCURRENTDENSITY AVERAGE 2 ;
END Metal1

LAYER Via1
  TYPE CUT ;
  SPACING 0.3 ;
  WIDTH 0.2 ;
  ANTENNAMODEL OXIDE1 ;
    ANTENNAAREARATIO 20 ;
  DCCURRENTDENSITY AVERAGE 0.1 ;
END Via1
```

Standard Cells: LEF file

LEF File	
Header Part	Technological Information
Cell Descriptive Part	Standard Cell Information



Physical Size: PR Boundary

Obstruction (OBS)

PINs:Terminals with Physical Placements

Physical Size: Shape and size of the cells defined by respective boundaries are reflected under keyword **SIZE**

Terminals with Physical Placements: Location of pins, layers on which pins are placed and geometrical descriptions

Obstruction (OBS) : Provides locations of all the metal tracks and vias in the layout of standard cell

```
MACRO INV1X1
  CLASS CORE ;
  ORIGIN 0 0 ;
  FOREIGN INV1X1 0 0 ;
  SIZE 2.4 BY 15 ;
  SYMMETRY X Y ;
  SITE core ;
  PIN A
    DIRECTION INPUT ;
    USE SIGNAL ;
    PORT
      LAYER Via1 ;
        RECT 0.65 6.8 0.85 7 ;
      LAYER Metal1 ;
        RECT 0.55 6.7 0.95 7.1 ;
        .
        .
    END
  END A
  .
  .

  OBS
    LAYER Metal1 ;
      RECT 0.6 4.9 1.01 5.3 ;
      RECT 1.28 1.5 1.68 3.3 ;

      .
      .
  END
END INV1X1
```

Standard Cells: LIF file

Why LIB File?

- In the process of synthesis, the RTL Code need to be converted into a Structural information containing interconnections of number of Standard cells to replicate RTL functionality.

- Extracting the Cell functionality, Wire delay, Power and timing constraints directly from Standard cells in GDSII form will be complicated.

- Therefore, LIB files are used where it gives simple model for delay, function, constraints and power of cell/gate level- Cell characterization

THANK YOU

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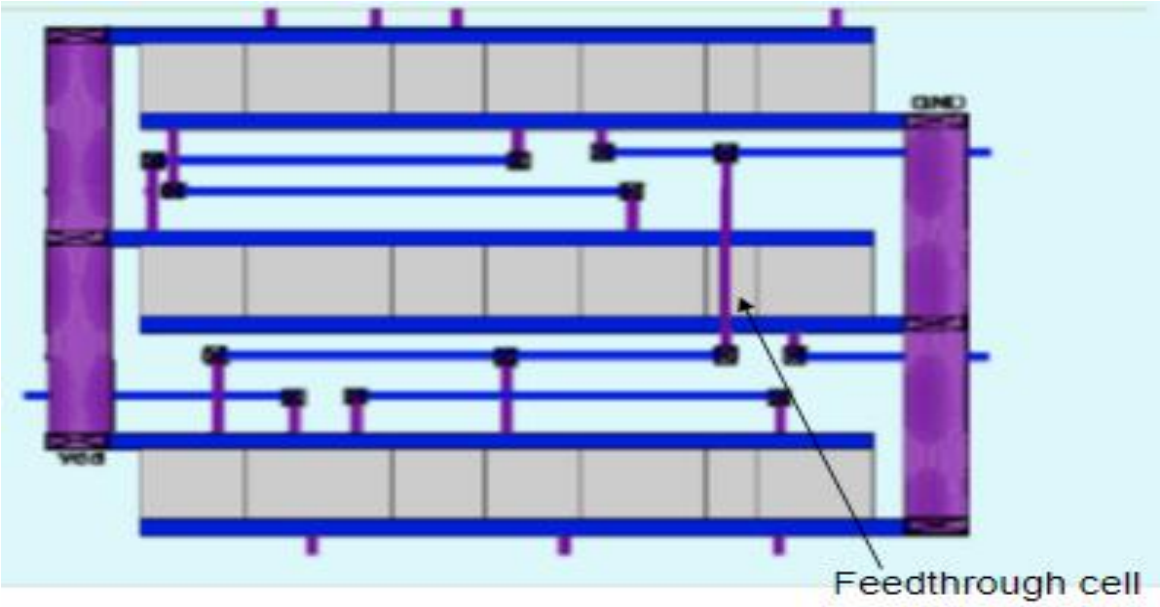
Half Track
One Track
Track height
Tracks
Track width
Half Track
12 Tracks
Half Track

Digital VLSI Design

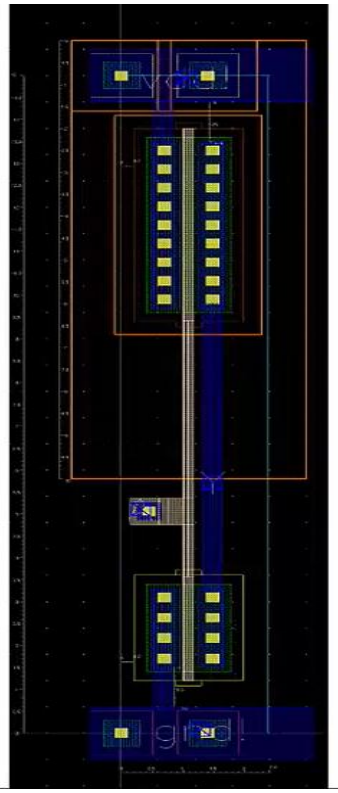
Standard Cells – Fixing Height for Standard Cell Library

- How to choose/Fix Cell Height for a standard cell Library ?
  - Height of cell is defined by Largest cell in the standard Library.
    Example: Let us say the standard Library has D-FF (which is the Largest cell) which is uses a Height of 15uM=25xP, then for all other cells the Height is defined as 25P



Digital VLSI Design

Standard Cells



Parameter values for INV1X1

Based on the discussion during *Lab 3: Dynamic characteristics*, we use $W_p = 2 \times W_n \Rightarrow W_p = 4\mu m$ and $W_p = 2\mu m$

Layer 1	Layer 2	Min. Spacing (μm)	Comments
PrBoundary	N-Imp	0.2	b/w 2 N-Imp, there should be atleast $0.4\mu m$
PrBoundary	P-Imp	0.2	b/w 2 P-Imp, there should be atleast $0.4\mu m$
PrBoundary	N-Well	$\geqslant 0.9$	To ensure overlapping b/w neighbor cells
M1(VDD/GND)	PrBoundary	$\geqslant 0.5$	Horizontal extension is chosen based on M1_PSUB placement
M1(VDD/GND)	S of MOS	0.9	In complex layout, this spacing would help us to route the signals through M1 between VDD & S/D of MOS
N-Well	PrBoundary (North west)	1.6	Based on M1_NWELL Via definitio