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Dual impedance

Dual impedance and dual network are terms used in electronic network analysis. The dual of an impedance Z is its reciprocal, or algebraic inverse $Z' = \frac{1}{Z}$. For this reason the **dual impedance** is also called the inverse impedance. Another way of stating this is that the dual of Z is the admittance $Y' = Z$.

The dual of a network is the network whose impedances are the duals of the original impedances. In the case of a black-box network with multiple ports, the impedance looking into each port must be the dual of the impedance of the corresponding port of the dual network.

This is consistent with the general notion duality of electric circuits, where the voltage and current are interchanged, etc., since $Z = \frac{V}{I}$ yields $Z' = \frac{I}{V}$[1]

Contents

Parts of this article or section rely on the reader's knowledge of the complex impedance representation of capacitors and inductors and on knowledge of the frequency domain representation of signals.

Scaled and normalised duals

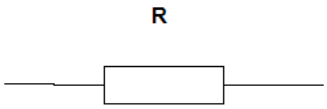
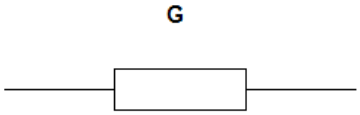
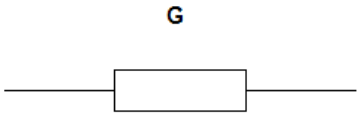
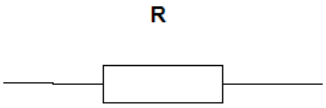
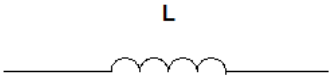
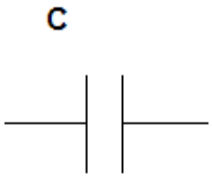
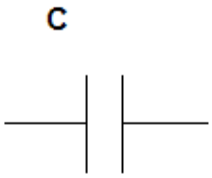
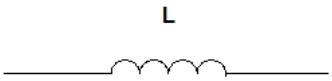
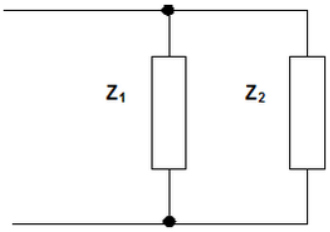
In physical units, the dual is taken with respect to some nominal or characteristic impedance. To do this, Z and Z' are scaled to the nominal impedance Z_0 so that

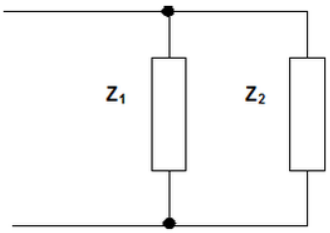
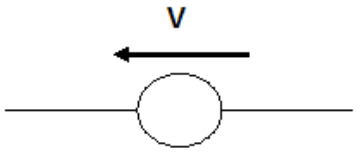
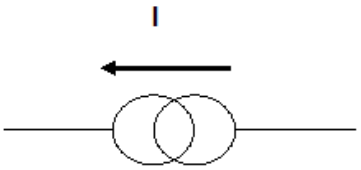
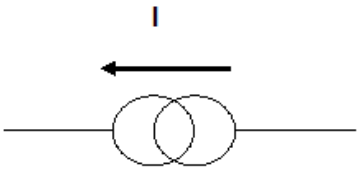
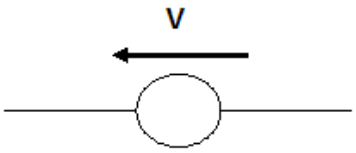
$$\frac{Z'}{Z_0} = \frac{Z_0}{Z}$$

Z_0 is usually taken to be a purely real number R_0, so Z' is changed by a real factor of ${R_0}^2$. In other words, the dual circuit is qualitatively the same circuit but all the component values are scaled by ${R_0}^2$.[2] The scaling factor ${R_0}^2$ has the dimensions of Ω^2, so the constant 1 in the unitless expression would actually be assigned the dimensions Ω^2 in a dimensional analysis.

Duals of basic circuit elements

[3]

Element	Z	Dual	Z'
 Resistor R	R	 Conductor G = R	$\frac{1}{R}$
 Conductor G	$\frac{1}{G}$	 Resistor R = G	G
 Inductor L	$i\omega L$	 Capacitor C = L	$\frac{1}{i\omega L}$
 Capacitor C	$\frac{1}{i\omega C}$	 Inductor L = C	$i\omega C$
 Series impedances Z = Z_1 + Z_2	$Z_1 + Z_2$	 Parallel admittances Y = Z_1 + Z_2	$\frac{1}{Z_1 + Z_2}$

 Parallel impedances $1/Z = 1/Z_1 + 1/Z_2$	$Z = Z_1 \parallel Z_2 = \frac{Z_1 Z_2}{Z_1 + Z_2}$ (Parallel sum)	 Series admittances $1/Y = 1/Z_1 + 1/Z_2$	$\frac{1}{Z_1} + \frac{1}{Z_2}$
 Voltage generator V		 Current generator I = V	
 Current generator I		 Voltage generator V = I	

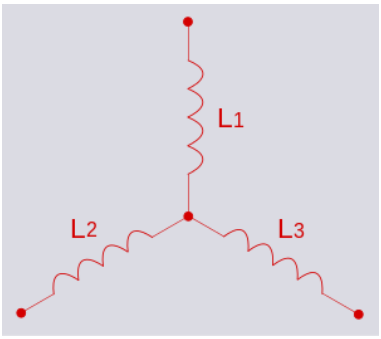
Graphical method

There is a graphical method of obtaining the dual of a network which is often easier to use than the mathematical expression for the impedance. Starting with a circuit diagram of the network in question, Z, the following steps are drawn on the diagram to produce Z' superimposed on top of Z. Typically, Z' will be drawn in a different colour to help distinguish it from the original, or, if using computer-aided design, Z' can be drawn on a different layer.

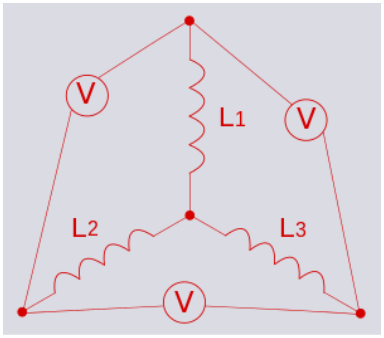
1. A generator is connected to each port of the original network. The purpose of this step is to prevent the ports from being "lost" in the inversion process. This happens because a port left open circuit will transform into a short circuit and disappear.
2. A dot is drawn at the centre of each mesh of the network Z. These dots will become the circuit nodes of Z'.
3. A conductor is drawn which entirely encloses the network Z. This conductor also becomes a node of Z'.
4. For each circuit element of Z, its dual is drawn between the nodes in the centre of the meshes either side of Z. Where Z is on the edge of the network, one of these nodes will be the enclosing conductor from the previous step.[4]

This completes the drawing of Z'. This method also serves to demonstrate that the dual of a mesh transforms into a node and the dual of a node transforms into a mesh. Two examples are given below.

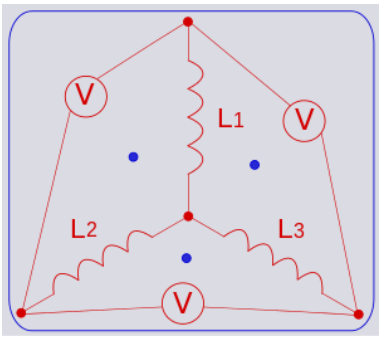
Example: star network



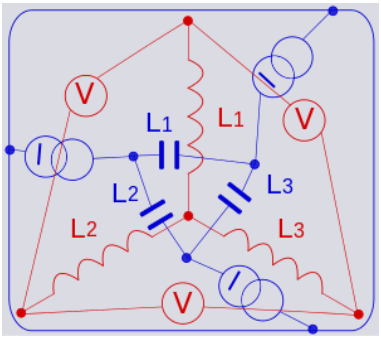
A star network of inductors, such as might be found on a three-phase transformer



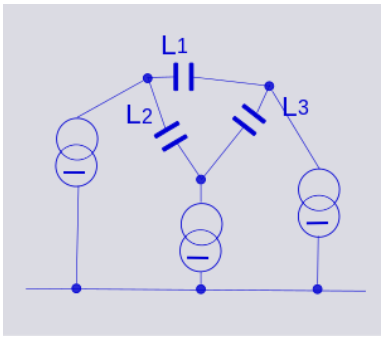
Attaching generators to the three ports



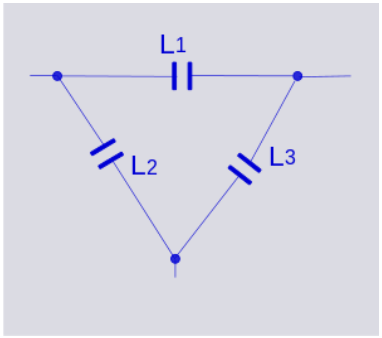
Nodes of the dual network



Components of the dual network



The dual network with the original removed and slightly redrawn to make the topology clearer

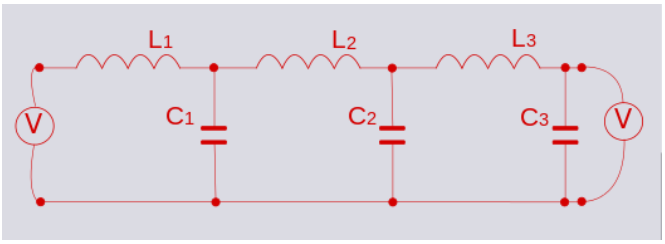


The dual network with the notional generators removed

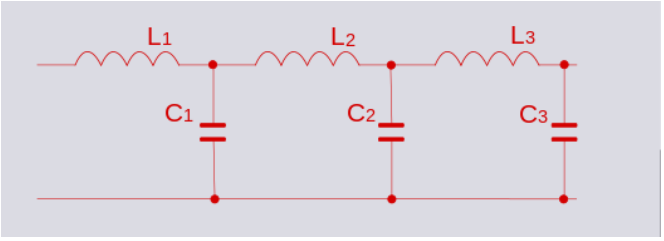
It is now clear that the dual of a star network of inductors is a delta network of capacitors. This dual circuit is not the same thing as a star-delta (Y-Δ) transformation. A Y-Δ transform results in an *equivalent* circuit, not a dual circuit.

Example: Cauer network

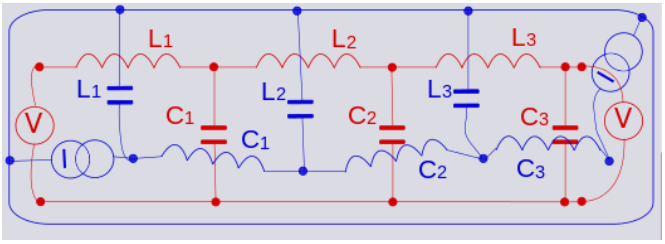
Filters designed using Cauer's topology of the first form are low-pass filters consisting of a ladder network of series inductors and shunt capacitors.



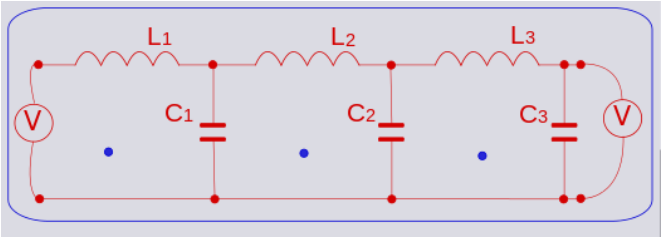
Attaching generators to the input and output ports



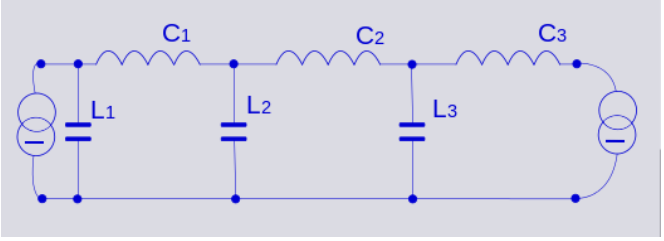
A low-pass filter implemented in Cauer topology



Components of the dual network



Nodes of the dual network



The dual network with the original removed and slightly redrawn to make the topology clearer

It can now be seen that the dual of a Cauer low-pass filter is still a Cauer low-pass filter. It does not transform into a high-pass filter as might have been expected. Note, however, that the first element is now a shunt component instead of a series component.

See also

- Series-parallel duality
- Topology (electrical circuits)

References

1. Ghosh, pp. 50–51
2. Redifon, p.44
3. Guillemin, pp. 535–539
4. Guillemin, pp. 49–52
   Suresh, pp. 516–517

Bibliography

- *Redifon Radio Diary, 1970*, pp. 45–48, William Collins Sons & Co, 1969.
- Ghosh, Smarajit, *Network Theory: Analysis and Synthesis*, Prentice Hall of India

- Guillemin, Ernst A., *Introductory Circuit Theory*, New York: John Wiley & Sons, 1953 OCLC 535111 (https://www.worldcat.org/oclc/535111)
- Suresh, Kumar K. S., "Introduction to network topology" chapter 11 in *Electric Circuits And Networks*, Pearson Education India, 2010 ISBN 81-317-5511-8.

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