ANALOG IC DESIGN OF BUCK CONTROLLER

B.Tech.

in

ELECTRICAL AND ELECTRONICS ENGINEERING

By

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ABSTRACT

DC-DC buck converters have become inevitable in various fields of engineering ranging from automobile engineering, aeromodelling, solar and other renewable energy engineering. To obtain a regulated output voltage, a controller is required which produces a pulse-width modulated (PWM) pulse to trigger the gate of the switching device. This thesis presents the design of a controller for a buck converter using current - mode control technique. It uses an on-chip current sensor for feedback along with output voltage feedback control. The controller is designed for an input range of 1.8V and the expected regulated output voltage is 1.2V for a switching frequency of 1MHz. The output ripple voltage and transient time is 80mV and 0.6ms for an off-chip capacitor of 230.36μF and inductor of 70μH.

The methodology involves four steps: stability analysis of the system, design of compensator, simulation of the circuit in MATLAB Simulink and defining the individual components of the controller using CMOS technology. Given the closed-loop converter model, the transfer function of the compensator is derived which is then used to compute the closed loop transfer function of the entire system. The model also accounts for practical difficulties like lowering the sub-harmonic oscillations using artificial compensation ramp. The analysis of output for various input voltage and load current variations is carried out using MATLAB Simulink. Each individual component of the controller is then modelled using CMOS technology and is verified for sample inputs in LTspice.

Keywords: Current-mode control; DC–DC buck converter; pulse width modulation

(PWM); switched-mode power converter; compensation ramp; CMOS technology.

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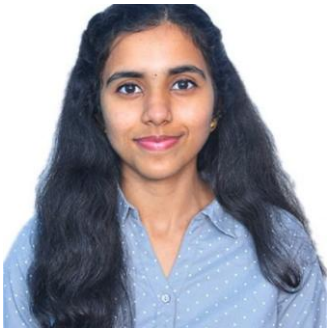
This support—both financial and moral—has not only propelled the technical progress of our project but has also inspired us to continue pursuing innovation with renewed enthusiasm and determination. We are proud of what we have achieved and are excited about the possibilities that lie ahead, made possible by the collective efforts and belief of everyone involved.



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CHAPTER 1

INTRODUCTION

1.1 ORGANIZATION OF THESIS

Chapter 1: Introduction - This chapter provides an introductory overview of the research project, including its purpose, motivation, and objectives. It sets the stage for the study by outlining the significance of DC-DC buck converters and their controllers in various engineering applications. The focus is on how these controllers can enhance power efficiency, reduce size and weight of electronic devices, and promote energy sustainability. By leveraging advanced control techniques and CMOS technology, the research aims to design reliable and efficient system-on-chip controller components for a buck converter that responds to real-time variations in input voltage and load current, thereby improving the overall performance and stability of power management systems.

Chapter 2: Literature Review - The literature review explores the progression of DC-DC buck converter control methodologies, starting from traditional voltage control method to current control methodologies. It examines the limitations of classical approaches and highlights the role of current-mode control in enhancing real-time regulation of output voltage. The review also discusses the integration of CMOS technology for implementing controller componnets, using simulation environments such as MATLAB Simulink and LTspice to design and evaluate the performance of buck converter controller components.

Chapter 3: Methodology - This section outlines the proposed designs for the buck converter components using current-mode control technique. It details the design of components such as Opamp, Compensators, Band Gap Reference, Open-loop operation, using CMOS

Technology of Semiconductor Laboratory (SCL) of India in Cadence Virtuoso. The design methodology includes transient stability analysis,

frequency stability analysis and load change analysis.

Chapter 4: Results and Observations - This chapter presents the simulation outcomes of proposed design and verifying if it meets the requirements.

Chapter 5: Summary and Conclusion - The conclusion summarizes the key contributions of the study, and the various developments made. It also reflects on the limitations of the current approach and suggests directions for future research for closed loop controller integration.

1.2 OVERVIEW

The rapid advancement in portable electronic devices and the need for efficient power management have led to significant challenges in designing compact and reliable DC-DC converters. Traditional control strategies, which operate based on fixed parameters or manually defined rules, are increasingly inadequate in handling the dynamic and unpredictable nature of modern electronic loads. This research proposes power converter using current-mode control, a technique capable of providing optimal regulation of output voltage through real-time feedback. The proposed system-on-chip controller design for a buck converter seeks to improve the efficiency of power management systems by enabling adaptive and precise control of the converter based on load and input voltage variations.

1.3 MOTIVATION

The inefficiency of conventional power management systems often leads to increased energy consumption, reduced battery life, and larger device sizes. As the demand for portable remote electronic devices grows, for IoT applications, we are required to provide a constant voltage to these devices, supported even when their input voltage varries. Advances in control techniques and semiconductor technology present an opportunity to revolutionize how power is managed. By utilizing current-mode control, buck converter controllers can adapt to complex load scenarios and unstable input voltages (batteries) to provide with constant output voltage. This research is motivated by the potential of these intelligent systems to enhance power efficiency, reduce energy consumption, and make electronic devices more compact and sustainable.

1.4 NEED

Power converter systems lack the flexibility to respond to real-time variations in load and input voltage, leading to suboptimal energy efficiency and increased power consumption. It is required for the converter system to feedback from the output to regulate the output in case of any input voltage variations, load variations or both, and optimize power regulation accordingly. Current-mode control provides a promising solution to address these limitations by enabling the above required output variations while also handling frequency changes in a much more stable manner than the voltage control model. This study is essential to bridge the gap between traditional voltage control method to the emerging current control method.

1.5 OBJECTIVES

The primary objective of this thesis is to design, develop, and simulate key analog control components essential for the implementation of a Buck Converter on an integrated circuit (IC) chip. A Buck Converter, being a fundamental power electronics circuit used in voltage regulation, requires precision analog components to maintain stable and efficient operation under varying load conditions. In this context, a comprehensive design framework has been established to create the controller parts of the Buck Converter using industry-standard simulation platforms such as Cadence Virtuoso and LTspice. The focus is on achieving high performance and integration compatibility using a 180nm CMOS process, with the ultimate aim of progressing towards a fully integrated Buck Converter controller IC suitable for practical fabrication.

The development process involves the in-depth analog design of several critical modules—namely, the Operational Amplifier (Op-Amp), Compensation Network (Compensator), SR Latch, Power Switch, and Low Drop-Out Regulator (LDO), Band Gap Reference (BGR). Each of these modules plays a distinct and vital role in the regulation, feedback, and switching functionalities of the Buck Converter. These components have been architected based on specific design specifications obtained from vendor-compatible switches, provided by the SCL (Semi-Conductor Laboratory) in Chandigarh. The designs were tailored to ensure compatibility with existing semiconductor fabrication constraints, while maintaining operational integrity and meeting target performance metrics such as power efficiency, response time, and signal fidelity. The use of 180nm technology ensures a balance between performance and manufacturability, making the designs viable for real-world implementation.

A structured simulation and verification methodology has been adopted to validate the performance of each component both in isolation and within subsystem configurations.

Cadence Virtuoso was utilized for schematic capture, simulation, and layout considerations, while LTspice served as a cross-verification tool for behavioral and transient response analysis. Special attention was given to documenting the operational characteristics, design trade-offs, and performance benchmarks of each component, laying a strong foundation for future integration into a unified Buck Converter controller IC. This thesis, therefore, not only presents the functional analog designs but also builds a framework for extending the work into more advanced power management systems through continued research and silicon prototyping.

CHAPTER 2

LITERATURE REVIEW

2.1 BUCK CONVERTOR

The Buck Converter is a ubiquitous DC-DC Switching Voltage Regulator used to step down the input voltage. The simplified schematic for the power stage of Buck converter is shown in the Fig. 1.1. The course "Power Management Integrated Circuits" by Khan (2017) gives a deep insight into various concepts of Buck converter. The Buck Converter operates in two different modes.

They are:

1. Discontinuous Conduction Mode (DCM)
2. Continuous Conduction Mode (CCM).

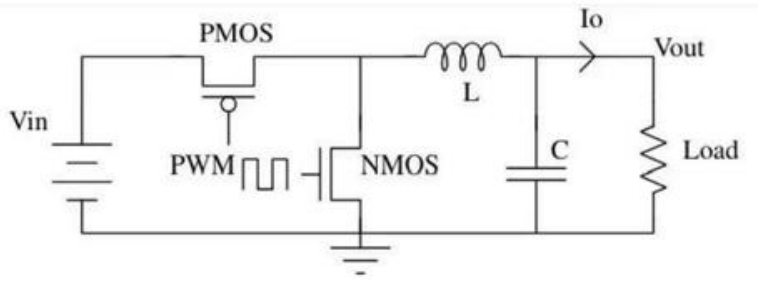

Fig 1: Buck Convertor

Discontinuous Conduction Mode (DCM)

In Discontinuous Conduction Mode, the current through the Inductor becomes zero for a fraction of the Switching period. This can be achieved at light load conditions, using a zero crossing detector for Inductor current and turning off the Power moset when the Inductor current becomes zero or by replacing the NMOS with a Diode.

Continuous Conduction Mode (CCM)

In Continuous Conduction Mode, the Inductor conducts throughout the switching period. The operating principle for CCM is described in Fig. 3. In each cycle, the circuit operates in two states namely ON and OFF states. In On state, the PMOS is conducting and the NMOS is off. The voltage across the Inductor in this state is give by

VL = Vin − Vout.

In off state, the NMOS is conducting and the PMOS is off. The voltage across the inductor in this state is given by

VL = −Vo.

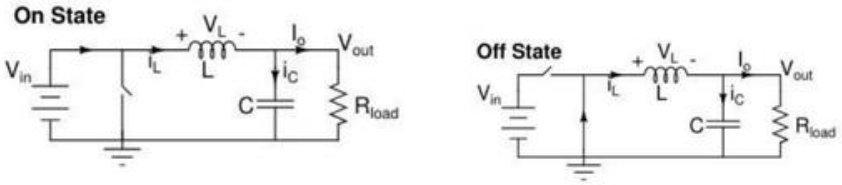

Fig 2: ON and OFF states of Buck convertor

The current through the Inductor (IL) is related to the voltage across it (VL) as

$$V = L\frac{dIL}{dt} \Longrightarrow \int_0^T dI_L = \frac{1}{L}\int_0^T V_L\, dt$$

$$\int_0^T dI_L = 0 \Longrightarrow \frac{1}{L}\int_0^T V_L\, dt = 0.$$

In steady state i.e., when all the external conditions such as input voltage or Load does not change, all the quantities such as Inductor current, output voltage etc. repeat themselves in

every cycle. In other words, the circuit behaves the same in each cycle. Hence, in steady state, the total change in Inductor current over one cycle is zero.

$$\int_0^T V_L\,dt = \int_0^{T_1} V_L\,dt + \int_{T_1}^T V_L\,dt = (V_{in} + V_{out})T_{on} + (-V_{out})T_{off} = 0$$

$$V_{out} = \frac{T_{on}}{T_{on}+T_{0ff}} V_{in}$$

The Duty cycle (D) of a rectangular signal is defined as the ratio of Ton and Time period of the signal.

$$D = \frac{T_{on}}{T_{on}+T_{0ff}}$$

Hence, The output and input voltages of a Buck converter are related as

$$V_{out} = \frac{T_{on}}{T_{on}+T_{0ff}} V_{in} = DV_{in}$$

Since $0 \le D \le 1$, $V_{out} \le V_{in}$

Inductor Ripple Current: Fig. 1.3 shows the voltage and current through the Inductor and Capacitor as a function of time.The peak to peak Inductor Ripple current(ΔI_L) is given by

$$\Delta I_L = \int_0^T di_L = \frac{1}{L}\int_0^{T_1} V_L\,dt = \frac{1}{L}\int_{T_1}^T V_L\,dt = \frac{V_{in}-V_{out}}{L} T_{on}$$

This is called Inductor Volt-Second balance. Now,

The maximum and minimum current through the Inductor are given by

$$\Delta I_L(max) = I_o + \frac{\Delta I_L}{2} \quad \Delta I_L(min) = I_o - \frac{\Delta I_L}{2}$$

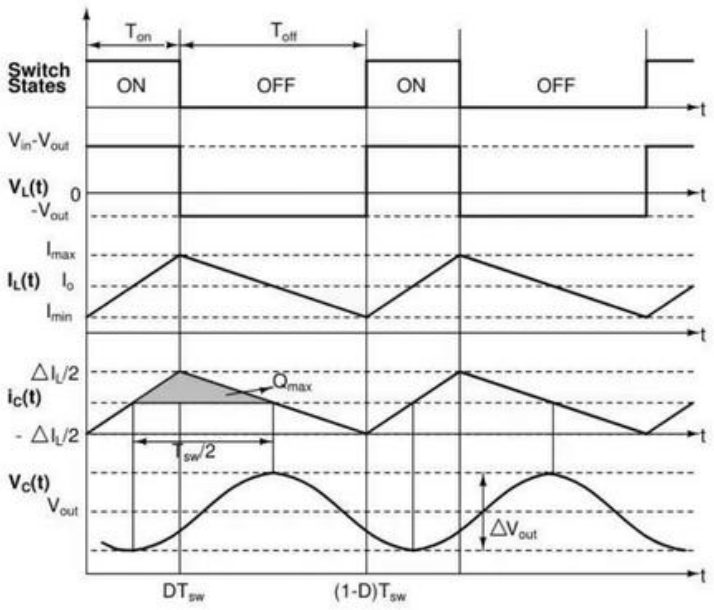

Fig 3: waveform operating in Continuous conduction mode

The Inductor current is divided into Load current and the current through the Capacitor (ic). Hence, the Capacitor (C) carries the ripple current through the Inductor (L). The Voltage across the

Capacitor (VC) is related to its current (ic) as

$$i_c = C\frac{dV_c}{dt} \Longrightarrow \int dV_c = \frac{1}{C}\int i_c\, dt = \frac{Q}{C}$$

where, Q is the charge stored in the Capacitor. Hence, the Output Voltage Ripple (ΔVout) is given by the maximum charge stored in the Capacitor during a cycle divided by the Capacitance (C).

$$Q_{max} = \int \frac{T}{2} i_c\, dt = \frac{1}{2}\frac{T}{2}\frac{\Delta I_L}{2} = \frac{\Delta I_L}{8F_m} = \frac{V_{in}\, D(1-D)}{8F^2L}$$

$$\Delta V_{out} = \frac{Q_{max}}{C} = \frac{V_{in}\, D(1-D)}{8F^2LC}$$

The Output Voltage ripple of the Buck converter as a function of Duty Cycle (D). We can see that the Output Voltage ripple is minimum at D = 0 and D = 1 and maximum ripple occurs at a Duty Cycle of ½.

2.2 MODELING OF BUCK CONTROLLER

2.2.1 VOLTAGE CONTROL METHOD

The voltage control method, also known as voltage-mode control (VMC), is a conventional technique used to regulate the output of DC-DC converters such as buck converters. In this approach, the output voltage is continuously monitored and compared with a reference voltage. The resulting error signal is processed by a compensator—typically a type II or type III error amplifier—which shapes the loop response and provides a control voltage. This control voltage is then compared with a periodic ramp or sawtooth waveform to generate the Pulse Width Modulation (PWM) signal that drives the switching transistor. The duty cycle of the PWM signal is modulated based on the magnitude of the error signal, thus adjusting the energy delivered to the load and regulating the output voltage.

The Voltage Control method is one of the most common configurations to implement in Buck Controller IC. The central mechanism of control lies in modulating the duty cycle of the power switch based on real-time feedback of the output voltage. A voltage divider network with a gain factor β is used to scale down the output voltage and generate the feedback signal, denoted as Vf. Under ideal, disturbance-free conditions, this feedback voltage equals the DC reference voltage Vref , signifying a balanced steady-state operation. The deviation from this ideal condition results in an error voltage, Ve, calculated as the difference between Vf and Vref. This error signal is processed by a high-gain error amplifier which determines the open-loop gain characteristics and significantly influences the stability, bandwidth, and transient response of the overall system. The error amplifier output is further shaped by a compensator block, which is essential for achieving the desired frequency response characteristics and maintaining a stable closed-loop operation.

However, the voltage control method has significant limitations, especially in high-performance or rapidly changing load environments. One of the primary drawbacks is **slower transient response**. Since the controller only responds to changes in output voltage, there is an inherent delay in reacting to disturbances such as sudden changes in load or input voltage. This delay can result in output voltage overshoot or undershoot, potentially affecting sensitive downstream circuitry. Additionally, voltage-mode control is more susceptible to **input voltage fluctuations**, as the input is not part of the feedback loop. This can degrade regulation quality, especially when the input supply is noisy or poorly regulated.

Due to these limitations, voltage-mode control is gradually being replaced in modern power management ICs by **current-mode control**, which offers superior dynamic response, improved input disturbance rejection, and better support for load sharing. While voltage-mode control remains useful for basic applications, its shortcomings in terms of speed, robustness, and adaptability make it less favorable in today's performance-driven electronics.

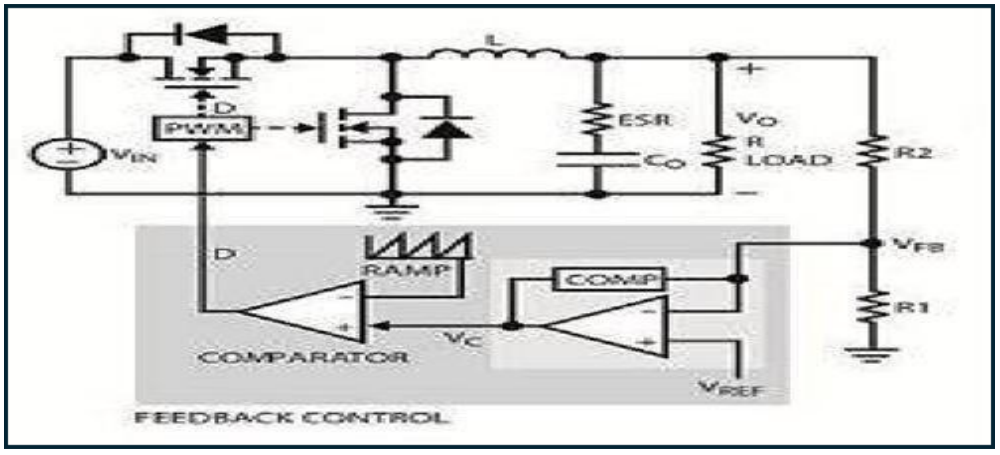

Fig 4: Voltage Control method

2.2.2 CURRENT CONTROL METHOD

Current Programmed Mode (CPM), also known as peak current-mode control, is an advanced technique for regulating the output of a buck converter by directly controlling the peak current through the switching transistor. Unlike voltage-mode control, where the duty cycle is explicitly controlled based on the output voltage error, CPM uses the inductor current as the primary feedback parameter. This approach improves dynamic performance, enhances system stability, and offers better protection mechanisms during transient conditions. The key advantage lies in its ability to react more quickly to changes in load or input conditions due to its inherently faster control loop.

In CPM, as depicted in the accompanying diagram, the switch current is(t)i_s(t)is(t) is continuously monitored and compared to a reference derived from the output voltage error. The output voltage V(t) is compared with a reference voltage Vref using a compensator, which generates a control voltage. This voltage is then used to set a current threshold, which is compared against the sensed switch current Is through an analog comparator. Once the sensed current equals the control threshold, the comparator resets the SR latch, turning off the transistor for the remainder of the switching period. This effectively modulates the duty cycle in real-time, based on current dynamics rather than just voltage, improving response speed and simplifying the design of the output filter.

However, CPM is not without its challenges. One prominent issue is sub-harmonic oscillation, which arises particularly when the duty cycle exceeds 50%. This type of instability occurs because the ripple current in the inductor fails to return to its initial value before the start of the next switching cycle, leading to alternating wide and narrow pulses at the switching node. This oscillatory behavior—known as sub-harmonic oscillation—can severely degrade performance and must be mitigated through slope compensation. By adding an artificial compensating ramp to the control signal with a slope equal to or greater than the inductor current's natural down-slope, the system effectively damps the oscillation within a single cycle, restoring stability even at higher duty cycles.

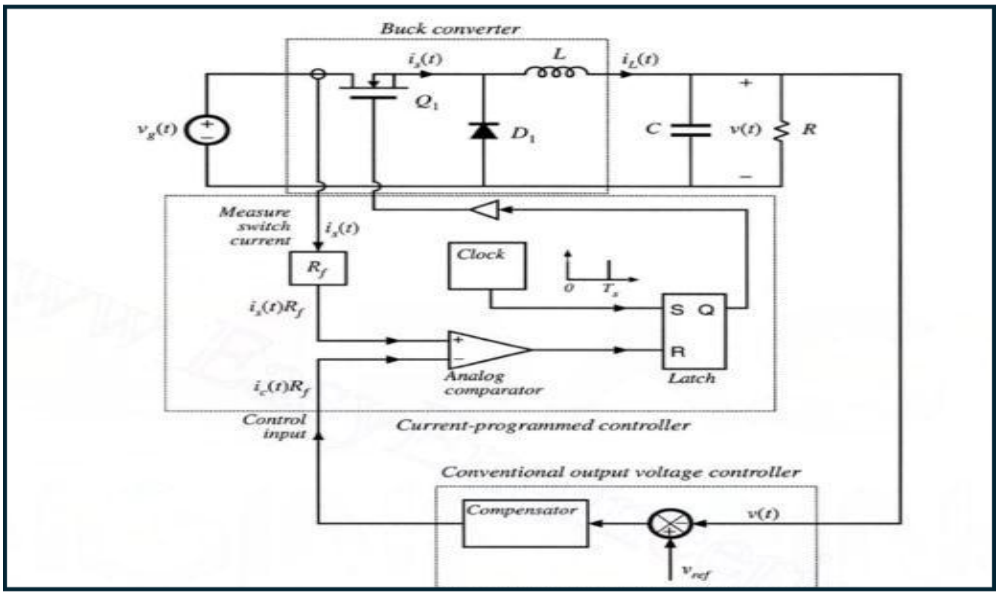

Fig 5: Current control method

Compared to voltage-mode control, CPM offers multiple advantages. Secondly, CPM naturally rejects input voltage perturbations due to its direct regulation of current. Thirdly, it simplifies the design of power stages, particularly in applications requiring parallel converters or current sharing. While voltage control is simpler and sufficient in slow or low-precision applications, it tends to lag in response and is more sensitive to input voltage fluctuations and filter component variations. Therefore, in performance-critical applications like processor power supplies, battery-operated devices, and dynamic load environments, CPM stands out as a more robust and reliable control strategy.

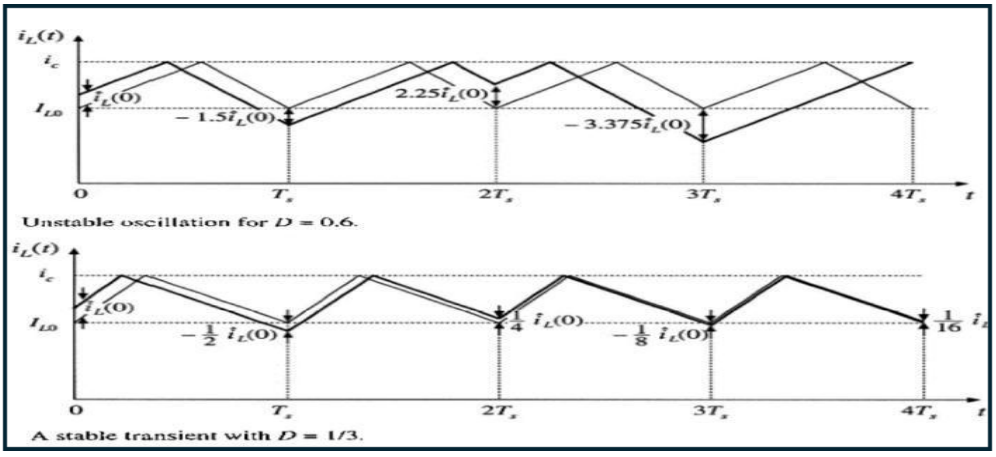

Fig 6: Sub-Harmonics when D>0.5

The compensator is a critical analog control component designed to ensure sufficient phase margin and gain crossover frequency for the loop gain, which in turn guarantees robust system performance against dynamic load and line conditions. Typically, the compensator integrates an error integrator, which enhances low-frequency gain to minimize steady-state error, while simultaneously introducing phase boost around the crossover frequency to improve phase margin. The output of the compensator, Vc, is compared with a high-frequency sawtooth or ramp waveform of frequency Fs by the PWM modulator. This comparison yields a PWM signal whose duty cycle is directly proportional to the amplitude of Vc. The switch, governed by this PWM signal, regulates the energy transferred to the output stage and hence controls the output voltage. At higher frequencies, the compensator is designed to roll off the gain, thereby limiting its influence on the closed-loop gain and suppressing noise amplification. In this thesis, a rigorous compensator design methodology is presented, capable of tailoring the loop response to meet stringent performance specifications in terms of bandwidth, stability, and dynamic regulation for DC-DC power conversion systems.

CHAPTER 3

METHODOLOGY

3.1 INTRODUCTION

Table 1. Required characteristics from Buck Controller designed

S.no	Parameter	Value
1	Input Voltage	1.9 -1.7 V
2	Output Voltage	1.2 V
3	Switching Frequency (Fsw)	1 Mhz
4	Oscillation Voltage (Vosc)	3.3V
5	Inductor(L)	160uH
6	Capacitor (C)	2uF
7	Ripple Voltage (V)	2 mV
8	Inductor Current (Il)	15 mA
9	Load Current (I)	1.5– 2.5 A

3.1.1 CONVERTER DESIGN

Required characteristics from Buck Controller designed**.**

Calculation of Inductor, Capacitor and Critical Resistance Values for a given Input Voltage and Output Ripple Voltage

Consider a buck convertor system with the following parameters:

Input voltage: Vg

Duty cycle: D

Sampling time: Ts

Change in output voltage: ΔVo

Change in inductor current: ΔIL

Inductance: L

Capacitance: C

In the proposed design, the switching frequency (fs) is 1MHz. So,

$$\text{Ts} = \frac{1}{f} = \frac{1}{1*10^6}\text{ s}, \quad \text{D} = \frac{3.3}{12} = 0.275$$

The ripple current can be expressed as ΔI_L = Imax – Imin

$$\Delta I_L = \frac{V_s - V_{out}}{f*L}(\alpha)$$

$$\alpha = \text{Duty cycle} = \frac{T_{on}}{T}$$

$$T_{on} = \text{D} * T_s = (0.275 * 1*10^6) = 275\text{Khz}$$

$$\alpha = \frac{275*10^3}{1*10^6} = 0.275$$

$$\Delta I_L = 0.0149 = 15\text{mA (approx.)}$$

The ripple voltage can be expressed as ΔVo = Vmax-Vmin

$$\Delta V_o = \frac{V_{in}\, D(1-D)}{8*f^2*LC}$$

$$= \frac{12*0.275*(1-0.275)}{8*(1*10^{6^2})*LC} = 0.93\text{ mV}$$

$$\Delta V_o = 2\text{mV(approx..)}$$

$$L = \frac{v_0(v_s - v_0)}{f\Delta I_L V_s}$$

$$= \frac{(3{\cdot}3)(12-33)}{(1\times10^6)(15\times10^{-3})(12)}$$

$$L = 160\mu H$$

$$C = \frac{v_{in}\, D\,(1-D)}{8F^2 L\Delta V_{out}}$$

$$= \frac{(12)*0.275(1-0.275)}{8*(1\times10^6)^2(2\times10^{-3})(160*10^{-6})} = 0.93\mu F$$

$$\text{C} = 2\mu F\ (approx)$$

3.2 OPAMP DESIGN

The two-stage CMOS operational amplifier (op-amp) is a widely used topology in analog integrated circuit design, particularly for applications requiring high gain, wide output swing, and sufficient frequency stability. The primary motivation behind a two-stage architecture is to achieve higher open-loop gain, typically in the range of 60 dB to 100 dB, while maintaining reasonable performance across load conditions and operating frequencies. This architecture consists of a differential amplifier (first stage) followed by a common-source gain stage (second stage).

In the first stage, a differential pair processes the input signals, ensuring high common-mode rejection ratio (CMRR) and enabling precise amplification of small differential inputs. The output of the differential stage is then fed into the second stage, an inverting amplifier that boosts the overall gain of the op-amp. This configuration helps achieve the desired gain for applications like signal amplification, filtering, and analog computation.

However, the two-stage configuration introduces additional poles and potentially right-half-plane (RHP) zeros, which can degrade stability and dynamic performance if not properly compensated. To ensure stability under closed-loop feedback, frequency compensation is crucial. The most commonly employed technique is Miller compensation, which involves connecting a compensation capacitor (Cc) between the output of the second stage and the intermediate node between the two stages. This introduces a dominant low-frequency pole and pushes the non-dominant poles to higher frequencies, enhancing phase margin and ensuring stable operation.

An inherent consequence of Miller compensation is the introduction of a right-half-plane zero, which adversely affects phase margin and limits the achievable gain-bandwidth product (GBW). To suppress this zero, designers often insert a series resistor with the compensation capacitor, or adopt advanced topologies like active compensation, cascode stages, or feed-forward techniques. A common alternative involves adding a capacitor between the low-impedance node of the first stage and the output of the second stage, thereby achieving

compensation without introducing a harmful feed-forward path that compromises phase margin.

A major challenge in designing two-stage op-amps lies in balancing gain, bandwidth, power consumption, and output swing. A high GBW requires large bias currents, while a high DC gain demands high output impedance and sufficient transconductance from both stages. Simultaneously optimizing these parameters is non-trivial. Stability is further complicated by load capacitance at the op-amp output. Studies have shown that increasing the load capacitance up to 10pF can improve Power Supply Rejection Ratio (PSRR), but beyond that, it can compromise phase margin if not compensated correctly.

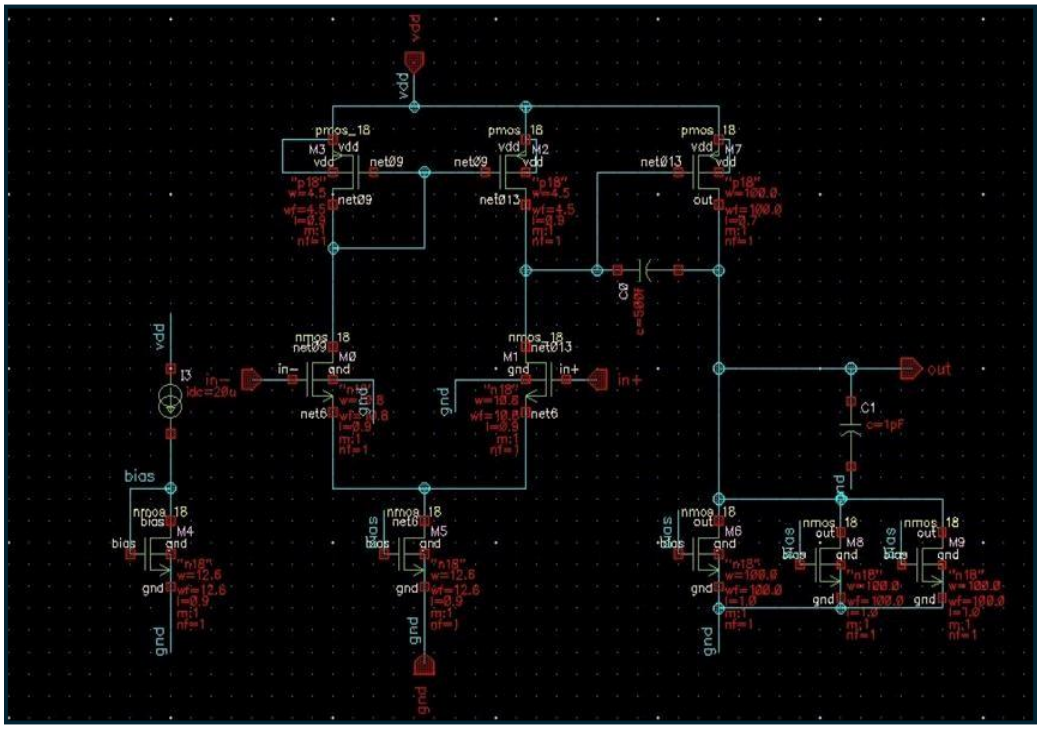

Fig 7: Op-amp Design

3.3 BANDGAP REFERENCE (BGR)

The Bandgap Reference (BGR) is a fundamental analog circuit used to generate a stable, temperature-independent reference voltage, typically around 1.2V, which is close to the bandgap energy of silicon at 0 K.

The core principle behind the BGR circuit is temperature compensation. Semiconductor devices like bipolar junction transistors (BJTs) or CMOS transistors exhibit temperature-dependent characteristics. To cancel out these variations, the BGR combines two types of temperature-dependent voltages:

CTAT (Complementary-To-Absolute-Temperature) Voltage: The base-emitter voltage VBE of a bipolar transistor exhibits a negative temperature coefficient, typically around -2 mV/°C. This means as the temperature increases, VBE decreases. This behavior is CTAT and forms one part of the reference voltage equation.

PTAT (Proportional-To-Absolute-Temperature) Voltage: A PTAT voltage is generated using the difference in VBE between two BJTs operated at different current densities.

By adding a CTAT voltage and a scaled PTAT voltage, the result can be made temperature independent at a specific operating point. The reference voltage VREF in a classic BGR is thus:

Here, KKK is a scaling factor typically implemented using resistor ratios in the circuit. By adjusting this factor, the negative temperature drift of VBE is exactly canceled out by the positive drift of the PTAT voltage, resulting in a flat temperature response.

A well-designed BGR circuits can maintain temperature stability within a few parts per million per degree Celsius (ppm/°C), which is adequate for most precision analog applications.

I have implemented the Bipolar BGR which utilizes BJTs or parasitic BJTs in CMOS processes to derive.

Advanced BGR circuits may also include curvature-correction techniques to address the non-linear temperature dependencies beyond first-order cancellation, further enhancing precision.

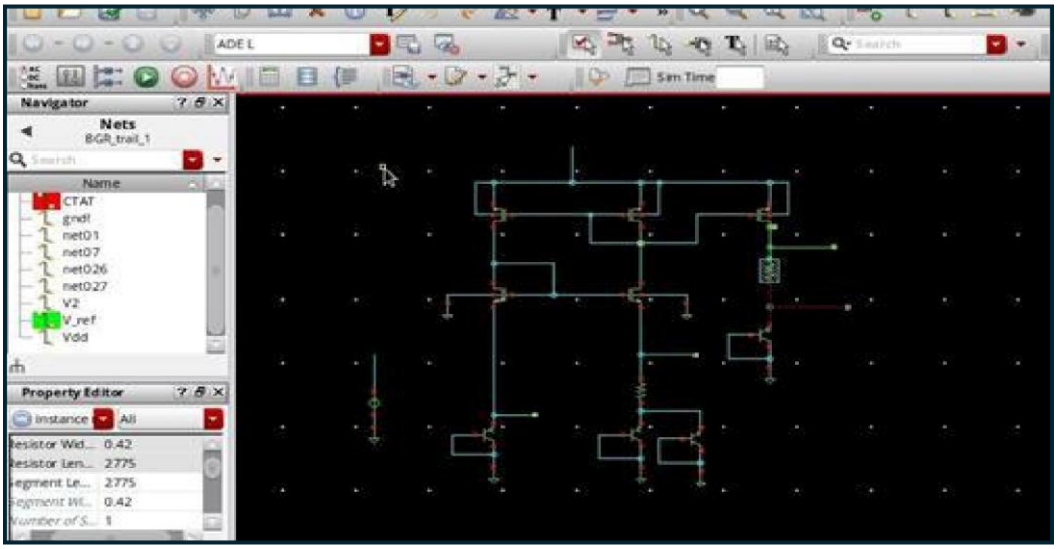

Fig 8: BGR Design

3.4 RAMP GENERATOR

A ramp generator circuit for generating sawtooth waveforms based on a clock signal may include an operational amplifier, a first switched capacitor device within a first feedback path of the operational amplifier, and a first plurality of switch devices within the first feedback path, whereby upon actuation of the first plurality of switches, the first switched capacitor generates first ramp waveforms during first alternate clock periods of the clock signal.

The circuit may also include a second switched capacitor device within a second feedback path of the operational amplifier, and a second plurality of switch devices within the second feedback path, whereby upon actuation of the second plurality of switches, the second switched capacitor generates second ramp waveforms during second alternate clock periods of the clock signal. The first alternate clock periods of the clock are followed by an adjacent one of the second alternate clock periods of the clock.

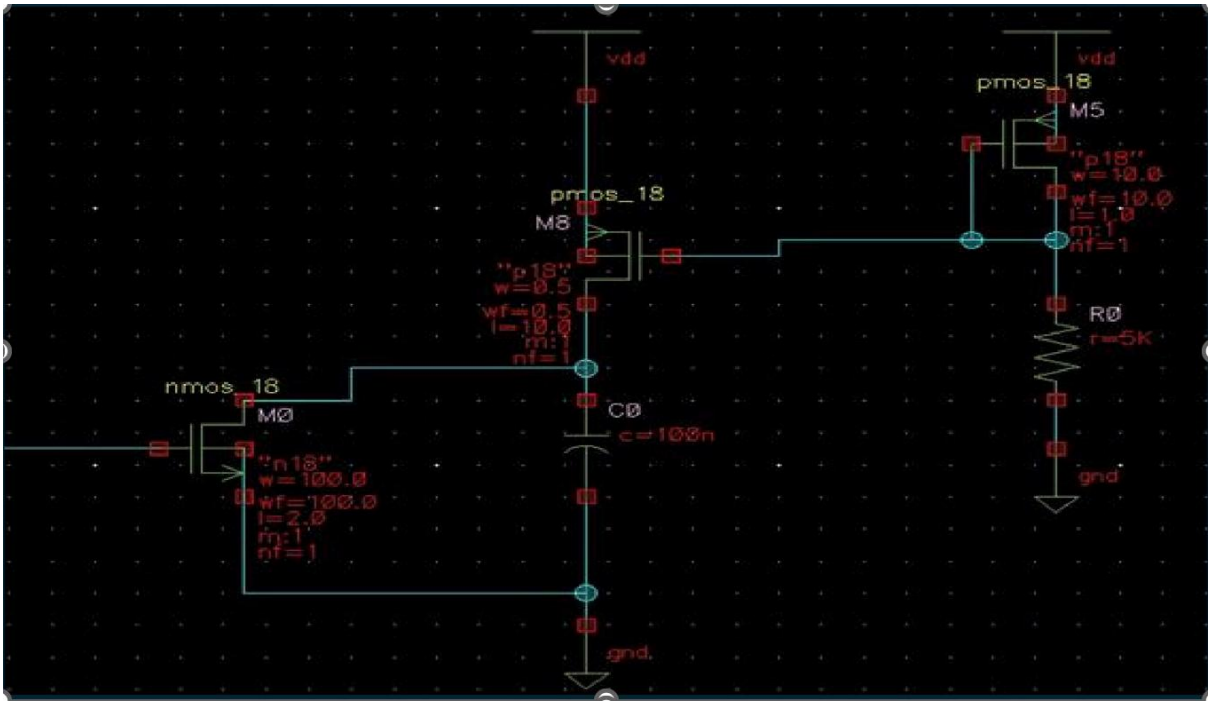

Fig 9: Capacitor charge reset circuit

The circuit also requires to create short pulses from the clock pulse of duty cycle 50% to make sure the distance between each sawtooth is small. This is done by creating a delay driver and comparing the clock with the delayed clock through a AND gate. This generates short pulses which is enough to short the capacitor to 0.

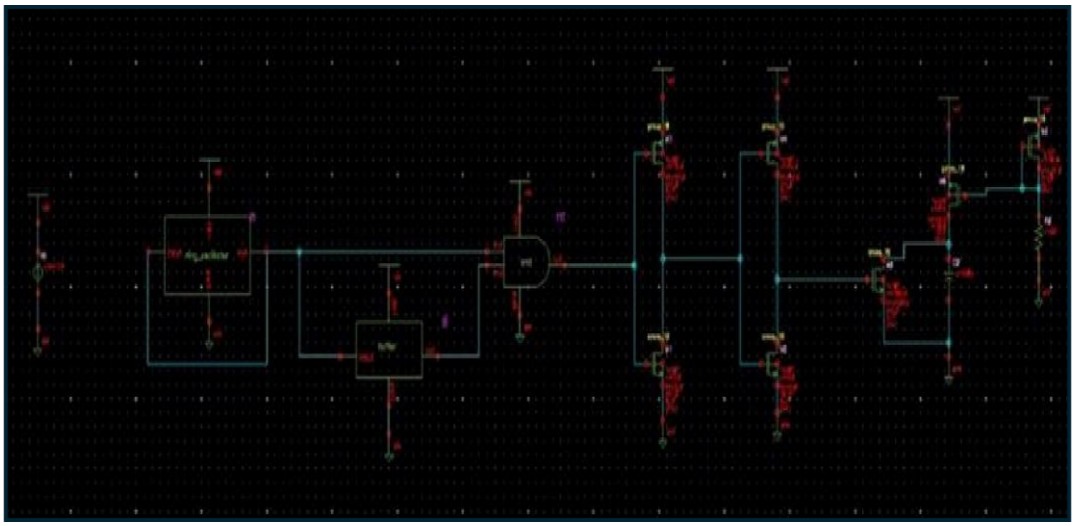

Fig 10: Pulse generator along with sawtooth generator

3.5 RING OSILLATOR

A device which consists of odd number of inverting amplifier stages with a feedback to the input is the ring oscillator and generally used in PLL devices. Odd number of stages gives the inverted output when the input voltage is given at once to the first stage, the oscillation starts. The most important factor in ring oscillator is gate delay because in devices fabricated with MOSFET, gate cannot switch immediately. The gate capacitance needs to be charged before current flows between drain and source so that every inverter takes time to give output.

Therefore increase in the number of stages of ring oscillator increase the gate delay. Odd number of inverter stages used to give the effect of single inverter amplifier with a negative feedback gain of greater than 1 so that the output will be in opposite direction to the input and it will be amplified with an amount more than the input. Amplified, inverted output is then propagated to the input with delay where it is amplified and inverted again. Propagation delay in ring oscillator is defined as the time difference between input and output.

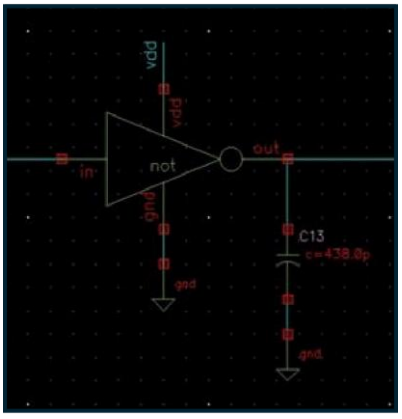

Fig 11: Single inverter level

Calculation:

Number of stages (n) =19

Frequency (f) = 1 MHz

3.6 LOW DROPOUT REGULATOR

A Low Dropout Regulator (LDO) is a linear voltage regulator designed to maintain a constant output voltage even when the input voltage is only slightly higher than the output voltage. In this design, the LDO is configured to convert an input voltage of 1.8V to a regulated output voltage of 1.2V, supplying a load current of up to 20mA. The circuit also includes a current protection mechanism that uses feedback to prevent damage during overcurrent or short-circuit conditions.

Basic LDO Operation:

The core components of an LDO regulator include:

Pass transistor (typically PMOS): Acts as a variable resistor, regulating current flow from input to output.

Error amplifier: Compares the feedback voltage with a reference voltage (Vref).

Voltage reference: A stable reference (e.g., 1.2V) against which the output is compared.

Feedback network: A resistor divider from the output provides a scaled version of the output voltage to the error amplifier.

The LDO operates by adjusting the gate of the pass transistor based on the error amplifier's output. If the output voltage drops, the error amplifier increases the gate voltage to pass more current, raising the output back to the desired level. Conversely, if the output rises, the gate is pulled down to reduce current flow.

Current Limiting via Feedback:

To protect the circuit from excessive current, especially during conditions like a short circuit, a current protection mechanism is integrated into the feedback loop. This protection works as follows:

A current sensing circuit, usually a small sense resistor or mirrored current branch, monitors the output current.

When the load current exceeds 20mA, the sensed current generates a voltage that is fed into a comparator or part of the error amplifier.

The comparator detects when the sensed current crosses a set threshold (corresponding to 20mA) and alters the feedback path.

Instead of maintaining the output at 1.2V, the error amplifier now reduces the gate voltage of the PMOS, causing the pass transistor to limit current flow.

This lowers the output voltage deliberately, reducing the power delivered to the load. This behavior protects the pass device and the downstream circuit by effectively reducing the output current during fault conditions.

This foldback current limiting approach is particularly effective. It not only limits the current but also ensures that under short-circuit conditions, the power dissipated in the LDO is reduced, protecting it from thermal stress.

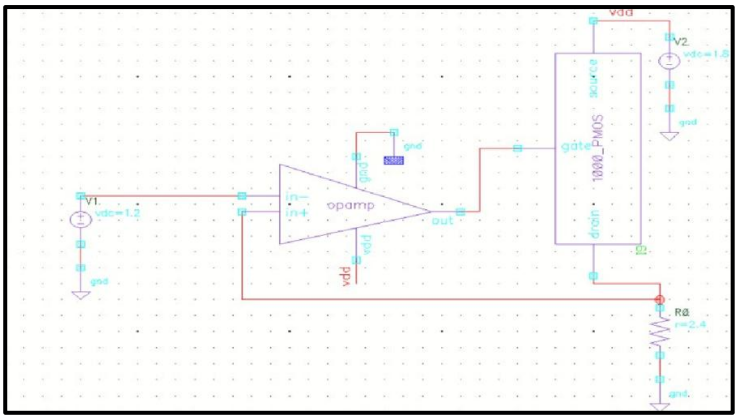

Fig 12: LDO basic design

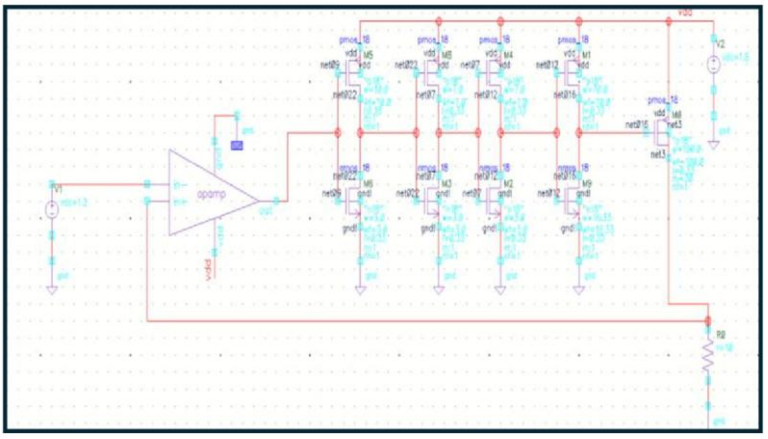

Fig 13: LDO Design with driver

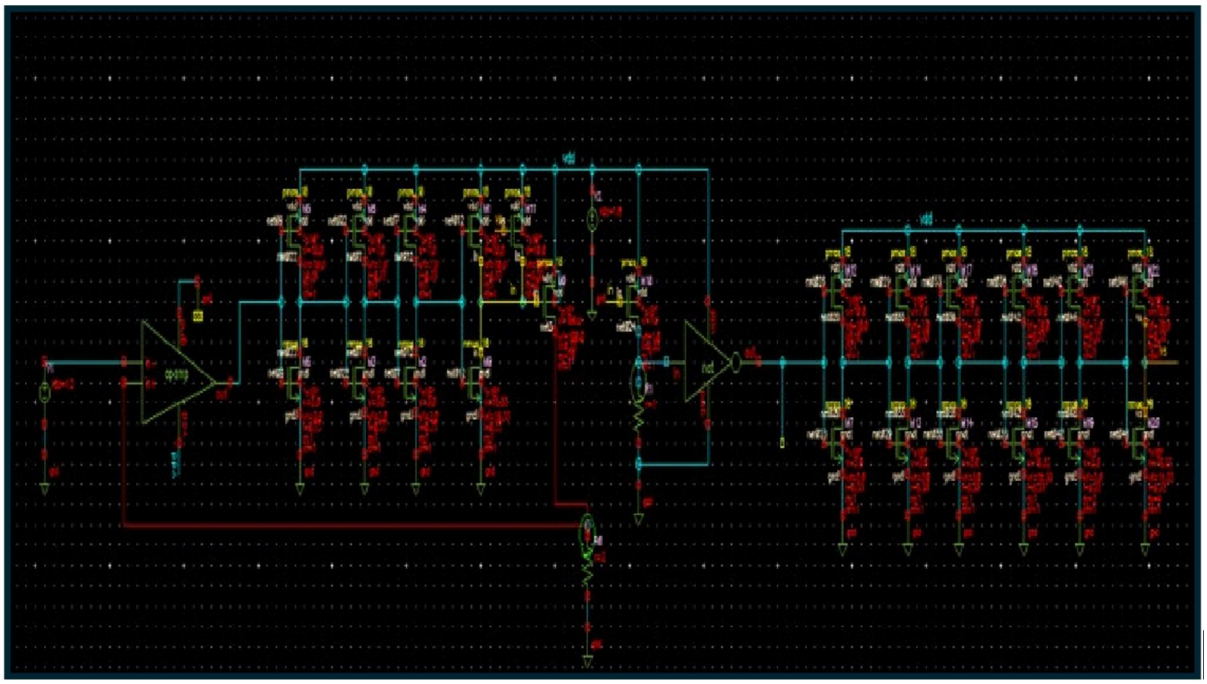

Fig 14: LDO Design with current limiting circuit

CHAPTER 4
RESULTS AND DISCUSSION

This chapter presents the experimental results of the proposed Deep Q-Learning (DQL) based traffic signal control system and compares its performance against traditional fixed-time and density-based round-robin controllers. The evaluation focuses on key metrics such as average queue length, vehicle waiting time, and reward optimization, using data extracted from SUMO simulations.

4.1 WORKING OF EACH MODULE DESIGNED

4.1.1 OPAMP

Specification	**Parameter**
Technology	SCL Pdk (180nm)
Supply Voltage	1.8V
Operating free air- temperature	-40 ℃, 27 ℃ and 127 ℃
Input bias current	20 mA
Input Common mode Range	0.7 V to 1.3 V
Open loop gain	60 dB
Input common mode Range	2 mV
Unity Gain Bandwidth	3.2 Mhz
Phase Margin	60 degrees

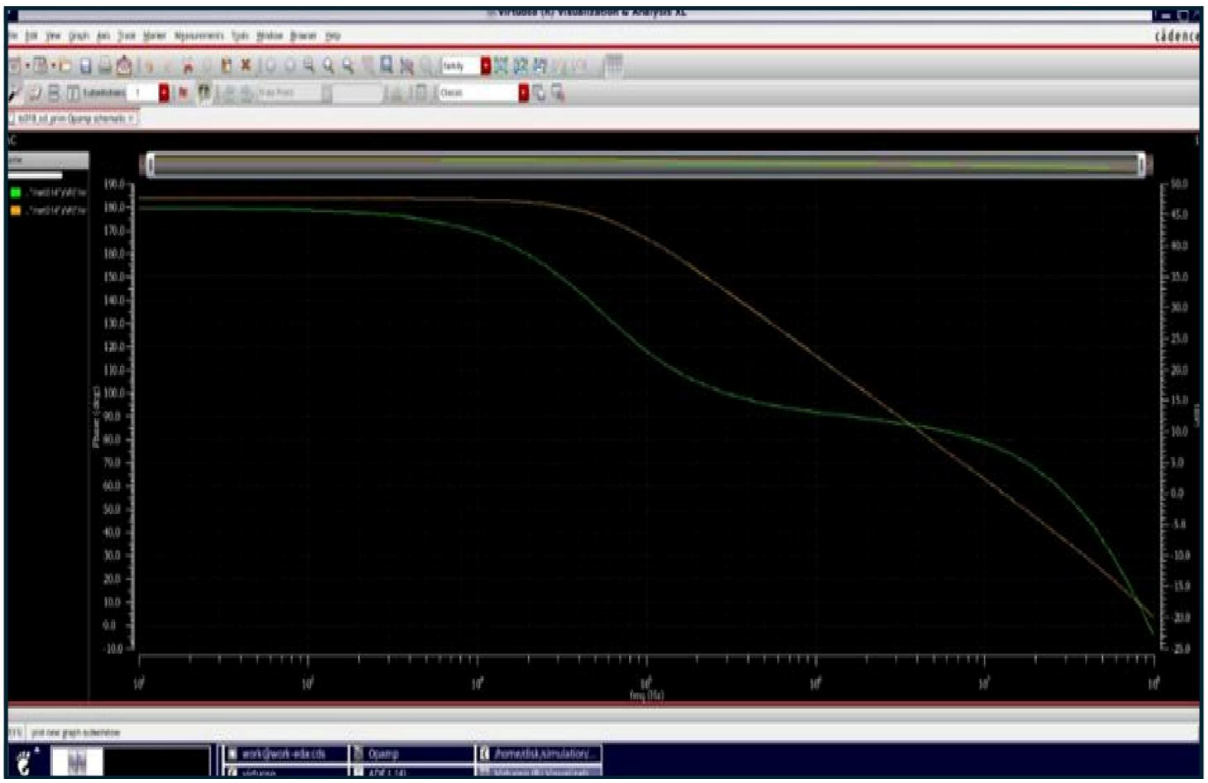

Fig 15: Frequency Analysis of Gain at Common Voltage 0.8 V

Phase gain of 60dB and 60dB gain obtained with common mode voltage 0.8V. We are also able to verify 3.2 Mhz unity gain bandwidth

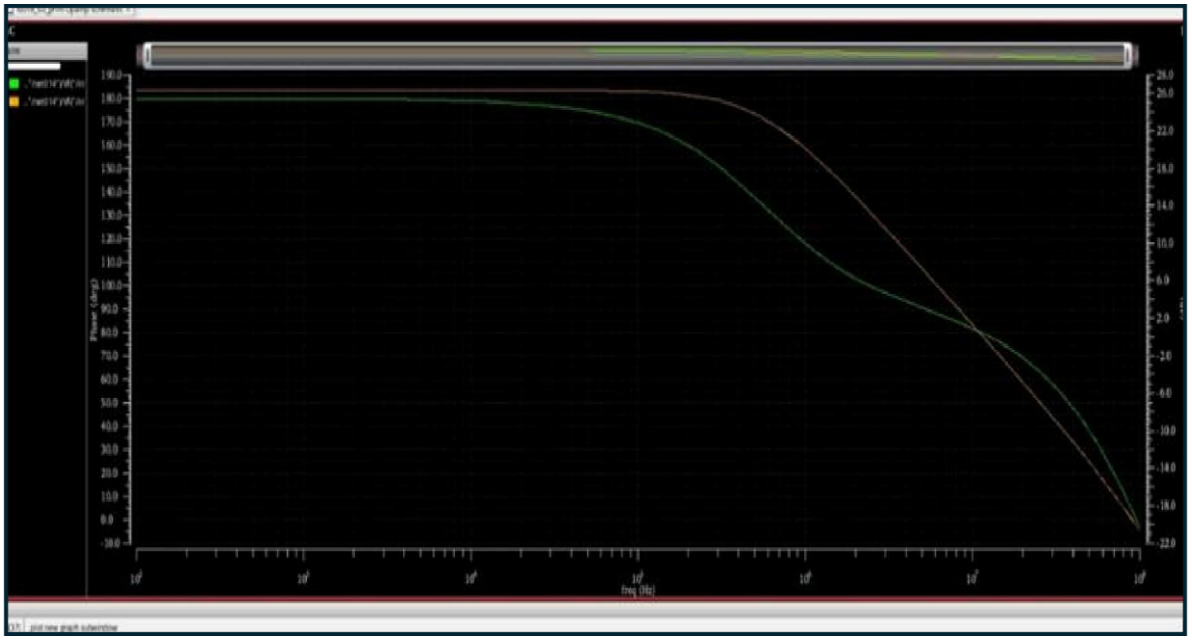

Fig 16: Frequency analysis of Gain at Common Mode voltage 1.2V

Phase gain of 70 dB and 30dB gain obtained with common mode voltage of 1.2V. Able to observe 900Khz unity gain bandwidth

Thus the working of OPAMP designed with given spec is verified for both 0.8V and 1.2V bias voltage.

4.1.2 BANDGAP REFERANCE

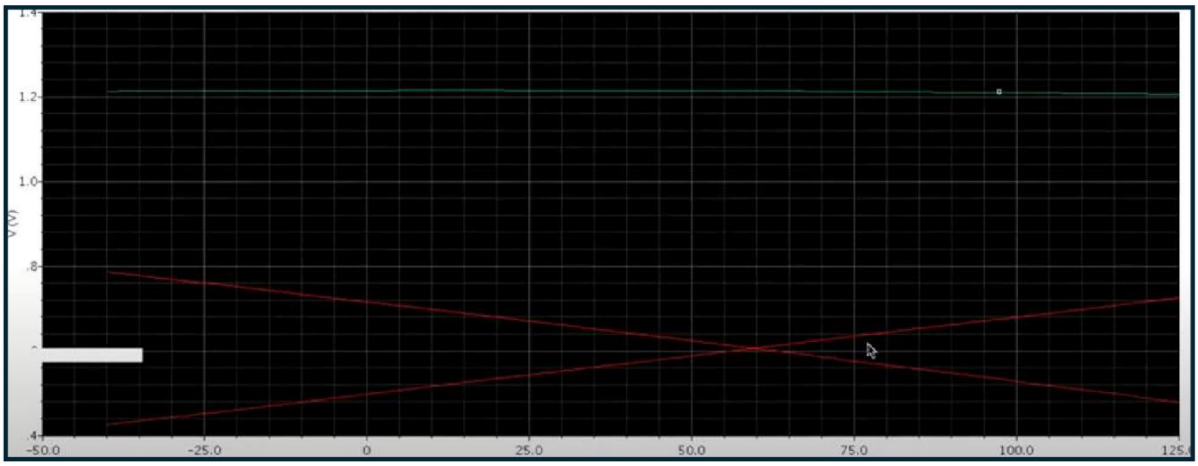

Fig 17 :BGR output with CTAT and PTAT Curves

The CTAT is seen to be reducing with temperature. This slope is at +0.027 V/C

The PTAT is matched with the amplification factor to match the slope of the CTAT. The PTAT is seen to be increasing with temperature.

Thus we amplify CTAT to match PTAT and on adding them, the slopes are seen to be cancelled and thus a constant output voltage of 1.2 V is seen.

On varying the circuit voltage from -50 to 125 ℃ we can observe that BGR outputs constant reference voltage 1.2 V. Thus required output is verified

4.1.3 RAMP GENERATOR

The output sawtooth waveform starts bending after 0.8V, as the capacitor charging characteristics is seen.

This circuit can output a waveform for the required compensatory Ramp function to cancel the sub-harmonic oscillations, which is of very small order every cycle and only grows as time moves

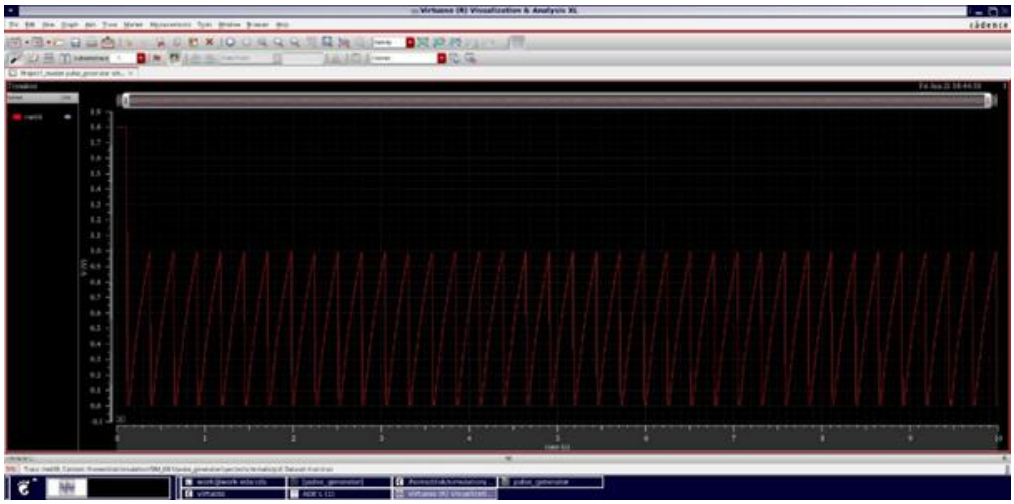

Fig 18: Ramp Generator output

4.1.4 RING OSCILLATOR

The clock of 1 Mhz is successfully generated using the Ring Oscillator. This helps us generate the clock pulses inside the chip other than from outside the chip.

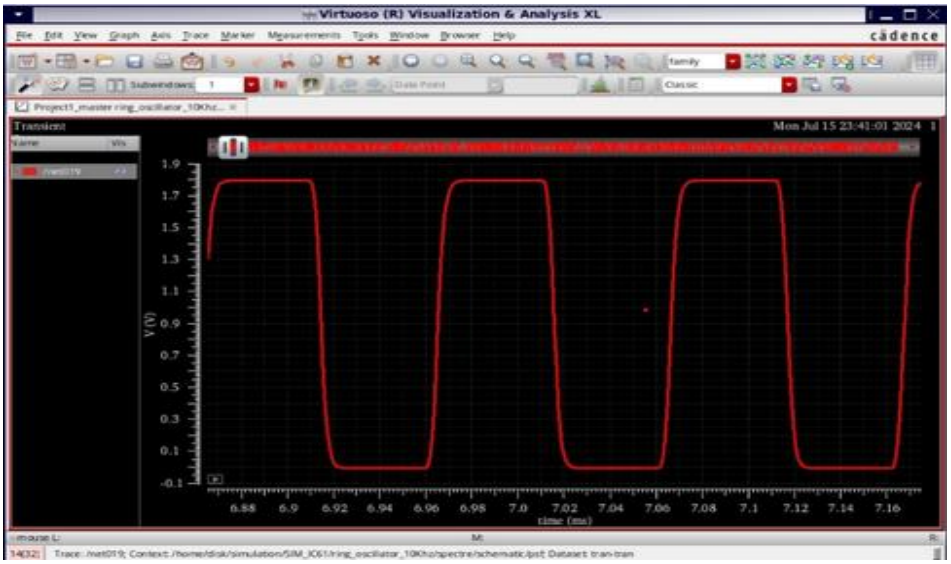

Fig 19: 1 Mhz Ring Oscillator Output

4.1.5 LOW DROUPOUT

Table 3. LDO Specifications

Specification	**Parameter**
Technology	SCL Pdk (180nm)
Supply Voltage	1.8V
Operating free air- temperature	-40 ℃, 27 ℃ and 127 ℃
Reference voltage	1.2 V
Output Voltage	1.2 V
Maximum load	500 mA
Cutoff Resistance	24 Ω

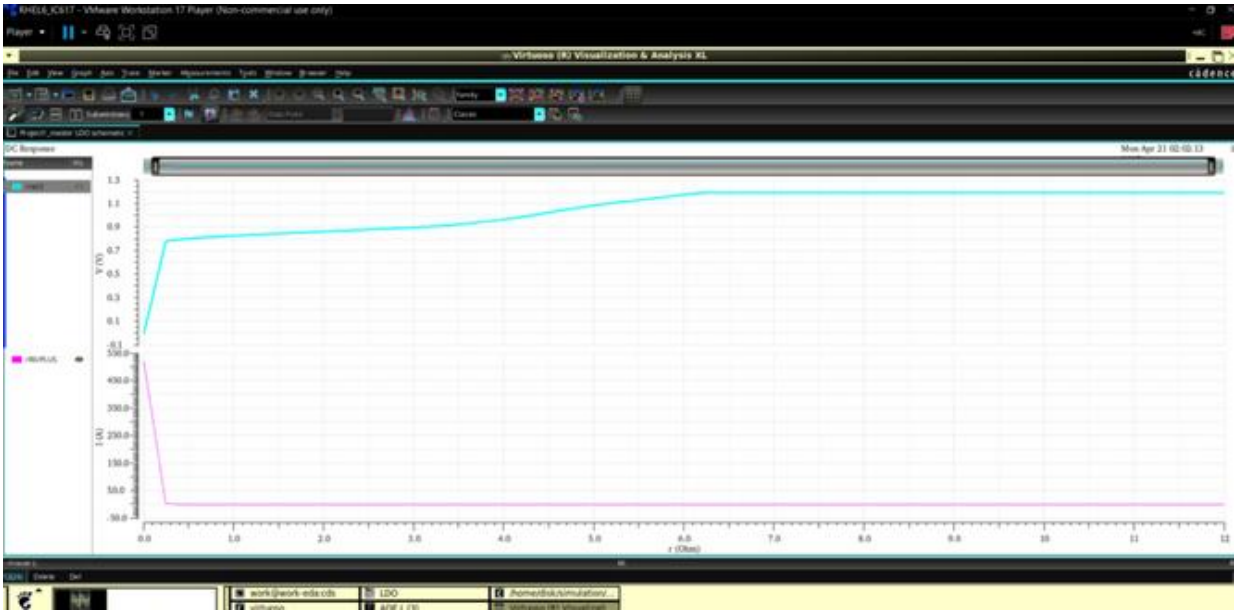

Fig 20: LDO without current protection circuit

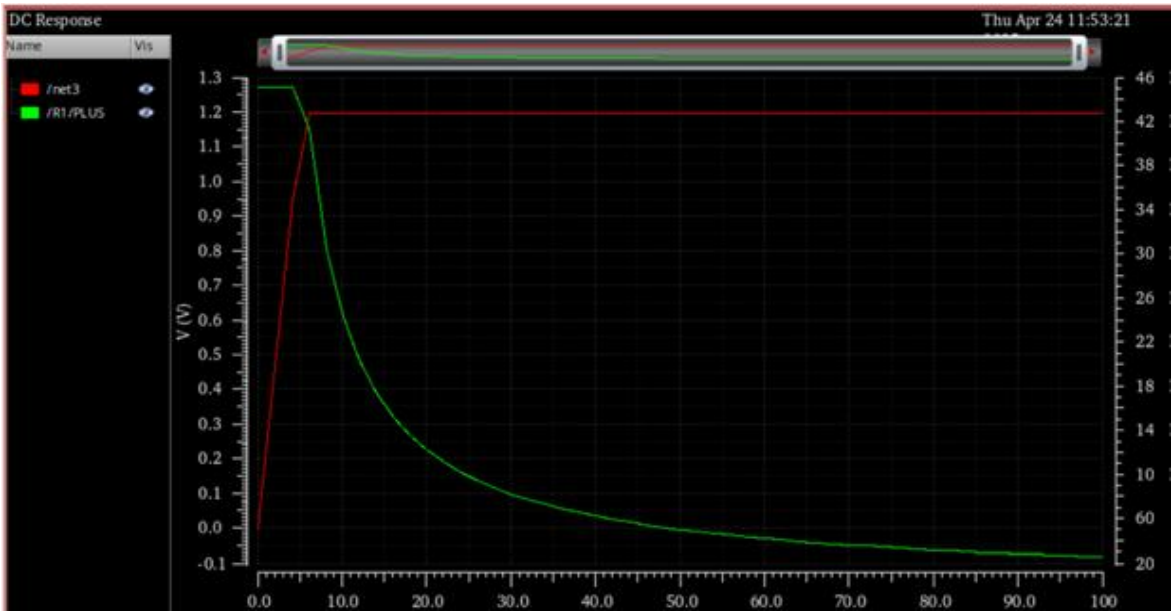

Fig 21: LDO with current protection circuit

The current protection implemented LDO, has a the output platued once the load exceeds 46mA, thus successful current protection circuit is implemented.

4.1.6 POWER MOSFET

Below table describes the specifications of the Power MOSFET designed

Specification	**Parameter**
Technology	SCL PDK (180nm)
Supply Voltage	1.8V
Operating free air- temperature	-40 ℃, 27 ℃ and 127 ℃
Ron	0.0049Ω
Roff	7.5 MΩ
Maximum load	500 mA

It has been verified that the R off the MOSFET exponentially increase with linear increase in Vgs. This ensures that the system doesn't leak much current during off condition.

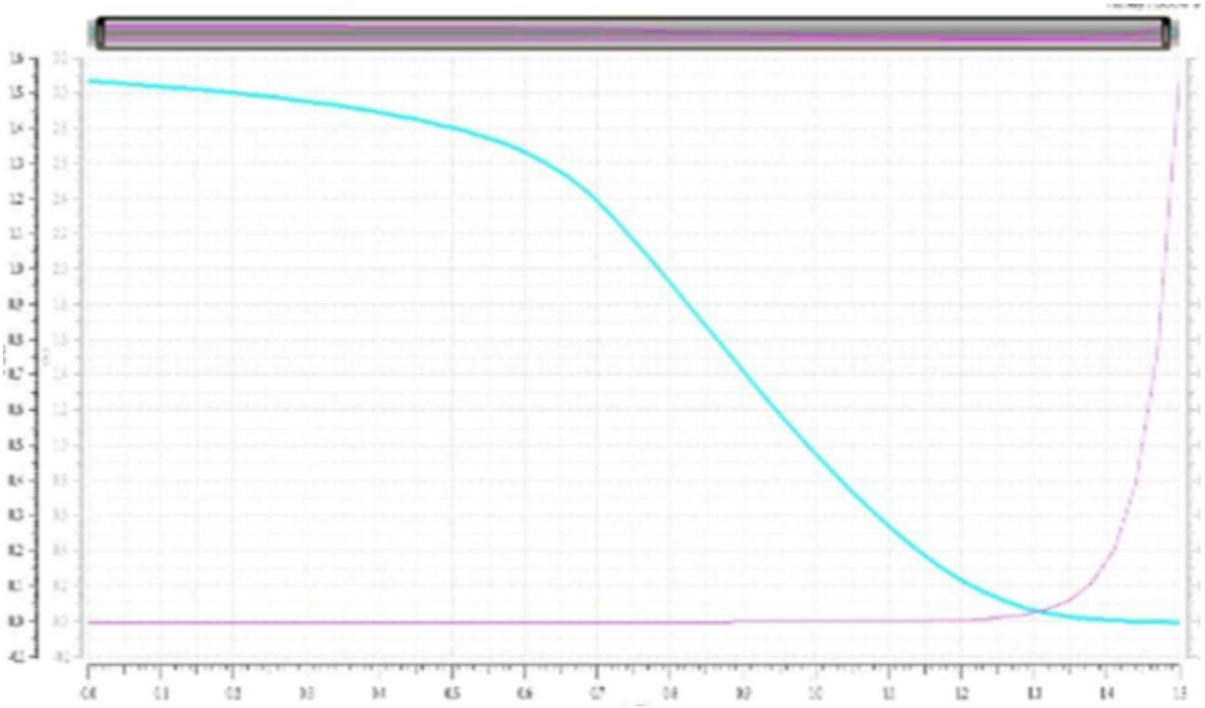

Fig 21: Current and Resistance plots of MOSFET with Gate Voltage

4.2 LIMITATIONS

Simulation Constraints: The current design does not simulate the breakdown of components due to heat or large loads, which can lead to inaccurate performance predictions under extreme conditions.

PDK Constraints: The Process Design Kit (PDK) provided by SCL India is not optimized for the latest MOSFETs and other components, resulting in potential errors and inconsistent behavior during simulations.

Software Limitations: The unavailability of genuine Cadence software has led to several challenges, including the inability to save outputs and perform comprehensive analyses.

CHAPTER 5

SUMMARY AND CONCLUSION

5.1 SUMMARY

The required buck controller components have been designed, verified, and further optimized for integration with the buck controller IC. Key achievements include:

· **Designing a BGR:** Successfully designed a Bandgap Reference (BGR) using SCL MOSFETs, accounting for their inconsistent behavior.

· **Current Protection Circuit:** Developed a current protection circuit for the Low Dropout (LDO) converter, safeguarding the circuit from overcurrent during accidental short-circuit conditions.

· **OPAMP Design:** Designed an operational amplifier (OPAMP) with 60dB gain and 60° phase margin, ensuring stable operation across all frequencies.

· **Clock Generation:** Generated a 1MHz clock using a ring oscillator, effectively integrating the clock within the circuit.

· **Sawtooth Waveform Generation:** Produced a sawtooth waveform using the available clock frequency to prevent sub-harmonic oscillations and maintain system stability.

· **Power MOSFET Design:** Designed a Power MOSFET to meet the required specifications and load conditions.

Thus have designed all the modules required for the Controller system and thus created a strong foundation for the development of the closed loop controller system.

5.2 CONCLUSION

In this thesis, a comprehensive design and implementation of a current-mode controlled DC-DC buck converter has been presented. The controller, designed for an input range of 1.9V to 1.7V, successfully regulates the output voltage to 1.2V with a switching frequency of 1MHz. The system’s performance, characterized by an output ripple voltage of 2mV and a transient response time of 0.6ms, demonstrates the effectiveness of the proposed design.

The methodology involved a detailed stability analysis, compensator design, and extensive simulations using Cadence Virtuoso. The derived transfer function of the compensator and

the closed-loop system ensured robust performance under varying input voltages and load conditions. The use of an on-chip current sensor for feedback, combined with output voltage feedback control, provided precise regulation and stability.

Furthermore, the individual components of the controller were meticulously modeled using CMOS technology and verified through simulations, confirming their functionality and reliability. The results indicate that the designed controller meets the desired specifications and can be effectively utilized in various engineering applications, including automotive, aeromodelling, and renewable energy systems.

Overall, this work contributes to the advancement of DC-DC buck converter technology by providing a reliable and efficient controller design, paving the way for future research and development in this field.

5.3 SCOPE FOR FUTURE WORK

Enhanced Efficiency: Future work can focus on optimizing the efficiency of the buck converter, particularly under variable dead band generator in the driver circuit, which reduces the power consumption by avoiding direct shorting of Vdd and Ground

Integration with Renewable Energy Systems: Given the increasing emphasis on renewable energy, integrating the buck converter with solar panels and other renewable sources can be explored. This includes developing algorithms for maximum power point tracking (MPPT) to enhance the overall system efficiency.

Multi-Phase Converters: Investigating the design and implementation of multi-phase buck converters can provide higher current capabilities and improved performance for high-power applications.

By addressing these areas, the current-mode controlled DC-DC buck converter can be further refined and adapted to meet the evolving demands of various engineering fields, ensuring its relevance and applicability in future technological advancements.

5.4 REFERENCES

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